Low Noise BiCMOS Front-end Amplifier in the DMILL Technology

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Abstract

Bipolar transistors become interesting devices for low noise front-end amplifier when the requirement of high speed has to be combined with low power dissipation. This paper presents a low noise front-end design using bipolar technology. This design has been proposed for the MSGC front-end electronics of the CMS tracker to shorten the effective signal length leading to a reduced pile-up probability from tracks belonging to different bunch crossings. It could equally well be used for Silicon detectors.

The detailed simulation of the circuit and the measured performance of several prototype circuits are described. At a power consumption of 1.4 mW/channel, a peaking time of 25 ns, a gain of 90 mV/MIP with a non-linearity less than 5% over ±6 MIPS dynamical range and a low noise performance (Equivalent Noise Charge *ENC*) of 1000 electrons rms were obtained for a 12 pF detector capacitance.

The radiation hardness of DMILL bipolar transistors has been a crucial issue in the past. Results of an irradiation with a high intensity pion beam are presented in this paper.

1. INTRODUCTION

In the CMS inner tracker will be several million channels of MSGC detectors. The readout requires high-density front-end electronics with an acceptable signal to noise performance, a speed sufficient to enable an event timing at the level of about two bunch crossing and a power consumption limited to a few mW per channel.

In order to reach this goal, the circuit solutions developed in low power specification should cope with the additional constraints of low noise, large bandwidth and high impedance input loads. Indeed, noise-power-speed conflicts exist. The requirement of low power suggests a choice of low currents, which produce low transistor transconductance and therefore low speed and high noise. Bipolar technology offers nowadays devices with excellent characteristics and is best suited for low power and fast electronics because of the highest transconductance to bias current ratio of *BJT*s. Another potential advantage of using bipolar transistors is a better noise matching compared to *CMOS* device.

A *BiCMOS* front-end electronic circuit has been developed. This paper presents the design concept and experimental results.

2. FRONT-END TOPOLOGY

Figure 1 shows the topology of the front-end circuit. A folded cascode topology is chosen for the preamplifier stage. The input transistor is a bipolar *NPN* transistor. The cascode transistor is a *PMOS* transistor because of *PNP* transistors is not available in the DMILL process. For all current sinks and current sources, *CMOS* transistors are used due to their better performances. The feedback loop consists of a capacitance of 100 fF and a resistance of 350 KΩ. The time constant of the feedback loop is short enough so the signal after the preamplifier does not require any differentiation.

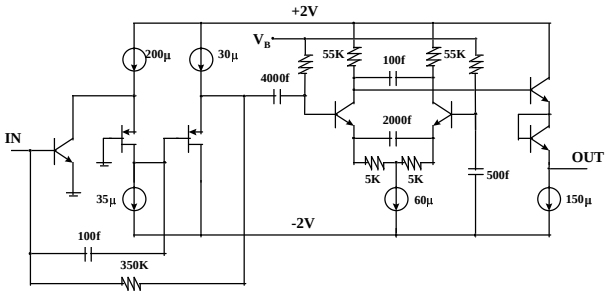

Fig. 1 Front-end topology

The second stage is constituted by a differential pair. It is used as an active filter to eliminate noise outside the useful bandwidth. The preamplifier and shaper together perform a semi-Gaussian shaping.

3. LOW NOISE OPTIMISATION

The noise performance of the front-end circuit is essentially defined by the equivalent input voltage noise and by the shot noise of the base current of the input transistor. [1]

$$d\ v_{eq}^2 = 4kT(\gamma\ r_B + \frac{1}{2g_m})\ df = 4kT(\gamma\ r_B + \frac{kT}{2qI_c})df$$

$$d\ i_{eq}^2 = \left[2q\left(I_B + \frac{I_c}{|\beta(j\omega)|^2} + I_D \right) + \frac{4kT}{R_f} \right] df$$

where $g_m = \frac{I_c}{V_{th}} = \frac{qI_c}{kT}$

$$\gamma = \frac{C_{Det} + C_f}{C_{Det} + C_f + C_{in}} = \frac{C_{Det} + C_f}{C_T}$$

I_D is the leakage current delivered by a detector; r_B is the base resistance of the input *NPN* transistor; C_f and R_f are respectively the feedback capacitor and feedback resistor of the preamplifier.

Consider that the preamplifier-shaper together performs a first order semi-Gaussian shaping, the relative contributions of the above two noise sources depend on the shaping time τ_o of the preamplifier-shaper and total input capacitance C_T as shown below:

$$ENC_{total}^2 = \frac{1.57e^2}{4\pi\ q^2}\frac{C_T^2}{\tau_o}4kT\left(\gamma\ r_B + \frac{kT}{2qI_c}\right) + \frac{1.57e^2}{4\pi\ q^2}\tau_o\left[2q\left(\frac{I_c}{\beta} + I_D\right) + \frac{4kT}{R_f}\right]$$

To minimise the contribution of the equivalent input voltage noise; the base-spreading resistance of the input transistor has to be reduced. A large dimension should be used for the input transistor. But from radiation consideration [2] [3], a larger input transistor will significantly increase the shot noise of the base current due to the decrease of the current gain β; β is more degraded when the current density is low. The size of the input transistor has then to be optimised by a trade off between the two noise source contributions: the series noise source of the base spreading resistance and the parallel noise source due to the base current. According to a preliminary analysis [4], and due to only a few emitter area choices available in the DMILL technology, a transistor emitter area of L_e x W_e = 20 x 1.2 µm^2 (L_e: emitter length, W_e: emitter width) is chosen for the input transistor. The base spreading resistance for the chosen geometry is around 150Ω.

The optimum collector current of the input bipolar transistor to minimise noise is:

$$I_{C_{OPT}} = \sqrt{\beta}\frac{C_T \mathrm{v}_{th}}{\tau_o}$$

For a required peaking time of 25 ns and a 10 pF detector capacitance ($C_T \cong$ 11pF), the optimum current is 150 µA ($I_{C_{OPT}} = 195\mu A$ for a 12 pF detector capacitance) and if a faster shaping is required, a higher current can be used. Figure 2 represents the noise performance from simulation versus collector current for two values of emitter length.

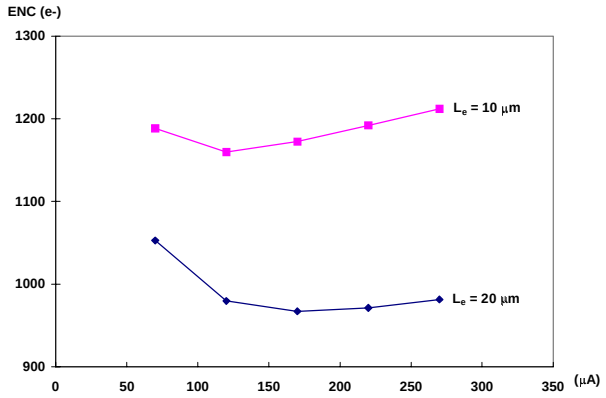

Fig 2. *ENC* vs collector current of input transistor

The feedback resistance in the input stage is used both for biasing the input bipolar transistor and for determining the effective gain of the preamplifier. In order to reduce the thermal noise contribution of this feedback resistance, a reasonable high value is chosen.

$$Noise\ Degradation_{r_B,R_f} = \sqrt{1 + \gamma\ \frac{r_B I_{C_{OPT}}}{\mathrm{v}_{th}} + \frac{\mathrm{v}_{th}}{\frac{R_f I_{C_{OPT}}}{\beta}}} - 1$$

The noise contribution due to the feedback resistance can be derived from the above equation and is less than 4%.

4. SENSITIVITY OF THE NOISE TO DETECTOR CAPACITANCE

The usual way to express the performance of a charge amplifier as a linear function of the detector capacitance as shown in the following equation is a good approximation only if the series noise is the dominating component.

$$ENC = ENC_o + k\ C_D$$

In the case of the bipolar front-end, this expression has little meaning if the parallel noise component is significant. An evaluation has been performed to compare these two different noise components. The total *ENC* can be represented by the following equation as:

$$ENC = \sqrt{ENC_s^{\ 2} + ENC_p^{\ 2}}$$

where ENC_s and ENC_p are the *ENC* coming from the series noise and parallel noise respectively. Taking into

account these two noises added in quadrature, the series noise is the dominant component in our design before irradiation. It is then interesting to quantify the *ENC* as a linear function of the detector capacitance C_{Det}.

From the Eldo simulation results, an *ENC* of about of 830 electrons rms was obtained at the detector capacitance equal to 10 pF. The sensitivity of the noise to the detector capacitance around its nominal value of 10pF is 42 e^- rms/pF. Figure 3 represents *ENC* as function of detector capacitance from simulation results.

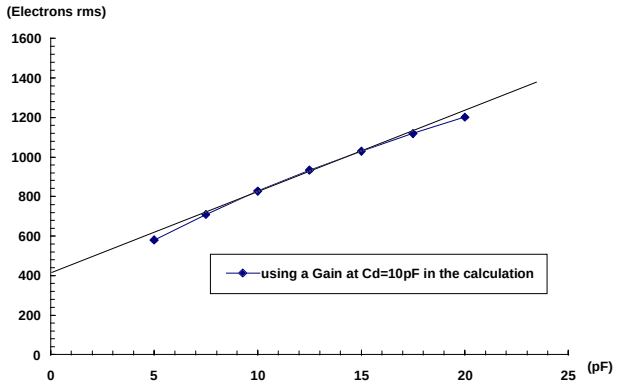

Figure 3. *ENC* versus detector capacitance

5. EXPERIMENTAL RESULTS

Figure 4 shows the output pulse shape over ± 6 MIPs (24000 e^-/MIP) dynamic range. The output pulse shape is very close to that of an ideal semi-Gaussian curve. The undershoot is less than 5%. Figure 5 represents the output peak amplitude (in mV) with an average gain of 90 mV/silicon MIP over ± 6 MIPs dynamic range. The non-linearity is less than 3% in ± 5 MIPs range. Figure 6 shows the peaking time for an input range from -6 up to +6 MIPs. A variation of ±1 ns has been obtained.

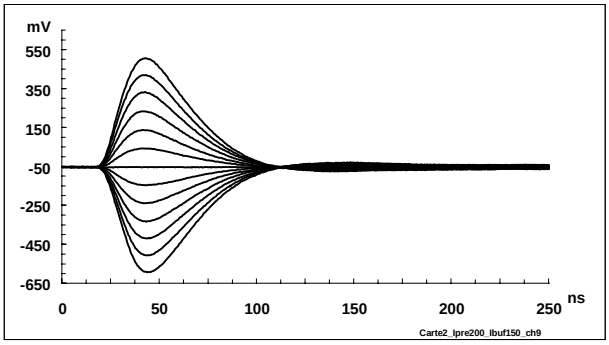

Fig. 4. Measured output pulse shapes over ± 6 MIP

The power consumption of the BiCMOS front-end is 1.42 mW/channel. The detailed power distribution is as follows: 580 µW for the preamplifier, 240 µW for the shaper and 600 µW for the emitter follower. The power consumption is similar to that of the APVD which is 1.46 mW/channel. Power consumption in the emitter follower depends on the total pipeline capacitance of channel. The 600 µW of power consumption in the emitter follower is calculated for a load capacitor of 3 pF. This value of the total pipeline capacitance per channel is considered as the worst case.

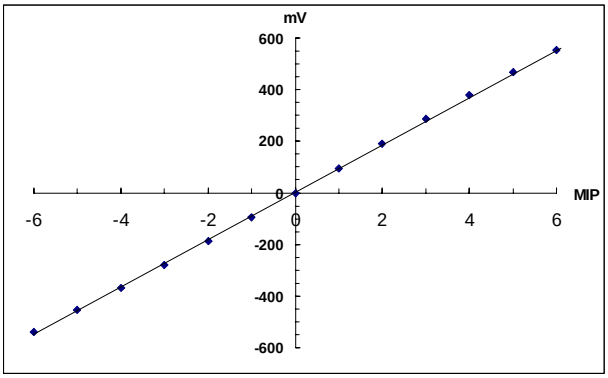

Fig. 5. Output linearity

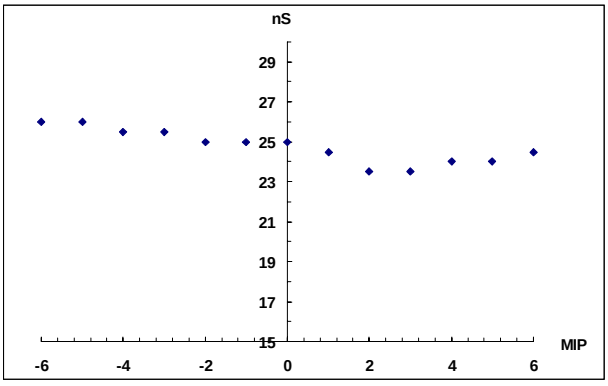

Fig. 6. Measured peaking time

Figure 7 represents a measurement of the *ENC* versus detector capacitance.

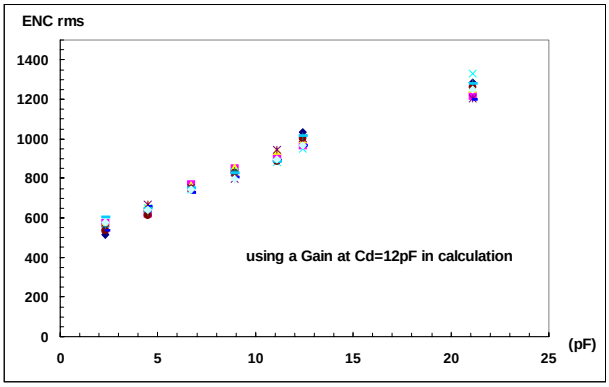

Fig. 7. Measured *ENC* versus detector capacitance

Note that the gain of the amplifier will slightly change when the detector capacitance changes. A constant gain at 12 pF is employed for the *ENC* calculation. This means the *ENC* values are smaller than indicated in the curve when the detector capacitance smaller than 12 pF and the

values are greater than indicated in the curve when the detector capacitance larger than 12 pF. The real *ENC* at 23.5 pF is around 1450 electrons rms. Taking into account the above correction, the average values of the measured noise figure in *ENC* can be represented as below:

$$ENC = 450\ e^- + 45\ e^-/\ pF$$

The measured and simulated *ENC* values versus the detector capacitance show a very good agreement.

Figures 8 shows the measured noise performance in *ENC* versus the input transistor collector current. It can be seen that the optimum collector current for a 12 pF detector capacitor is around 200 µA. This value is very closed to that of the theoretical analysis.

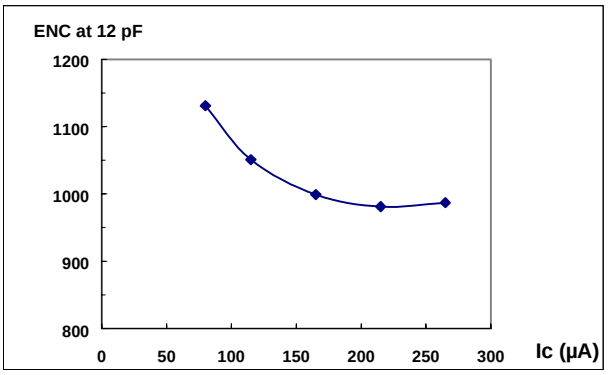

Fig. 8. Measured *ENC* vs. collector current of input transistor (C_{Det} = 12 pF)

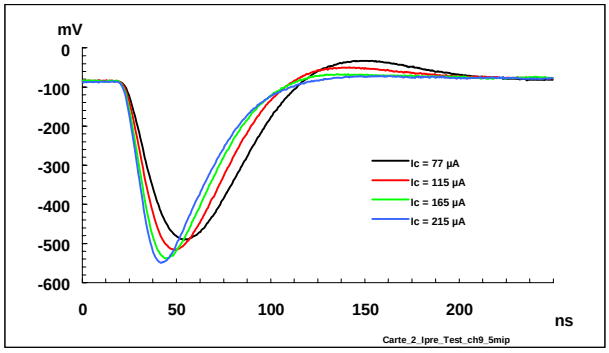

Fig. 9. Output waveforms as function of input transistor collector current (C_{Det} = 12 pF)

Figure 9 shows measured output waveforms of the front-end amplifier as function of the input transistor collector current for a detector capacitance of 12 pF (Using the 12 pF is only for the measurement convenience).

Figure 10 shows the peaking time versus the input transistor collector current for the same detector capacitance. Higher collector current is biased, quicker the peaking time is.

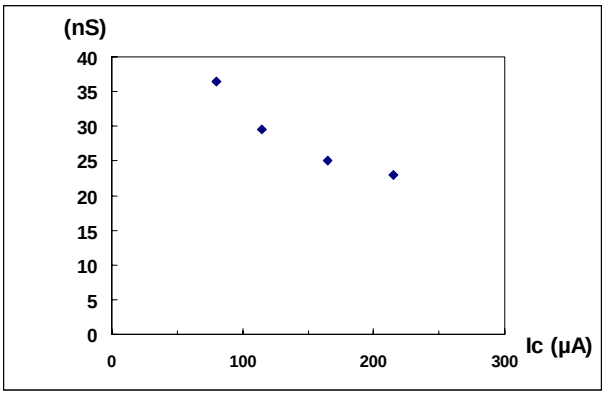

Fig. 10. Peaking time vs. collector current of input transistor (C_{Det} = 12 pF)

6. IRRADIATION

The radiation hardness of DMILL bipolar transistors has been a crucial issue in the past. To verify the circuit's performances, the circuit was irradiated using a high intensity pion beam with an integrated flux of 1.0 x 10^{14}/cm^2 which is roughly equivalent to 10 years LHC experience. For a same collector current bias (I_c = 120 µA), variations of peaking time (6%), output pulse shape and its amplitude (15%) are relatively small after irradiation because these circuit responses depend less on β.

As expected, the β is a parameter which has a very large variation before and after irradiation [5]. For example, the β of the input transistor has been changed from the nominal value of 200 down to 30 for a collector current biased between 100 and 140 µA. The current gain β is a function of collector current. From the simulation curve of current gain β versus collector current for the input transistor *NPN* (L_e x W_e = 20 x 1.2 µm^2) shown in figure 11, it can be seen that the collector current biased at around 120 µA is just a limit to have a correct performance. A higher collector current should give a better performance.

A weakness in circuit architecture has also been noted with respect to the feedback resistor in the preamplifier. In fact, leakage currents of the bipolar transistor I_{SC} and I_{SE} increase after irradiation, these lead to a DC bias variation via the feedback resistor R_f. In the worst case, the preamplifier is blocked. A feedback transistor can be used to replace that feedback resistor if a single power supply is employed (0 to 4 V). If so, a higher collector

current bias can be used to compensate delay of peaking time and reduce of output wave amplitude. The contribution of the parallel noise can also be reduced if a higher collector current bias is employed.

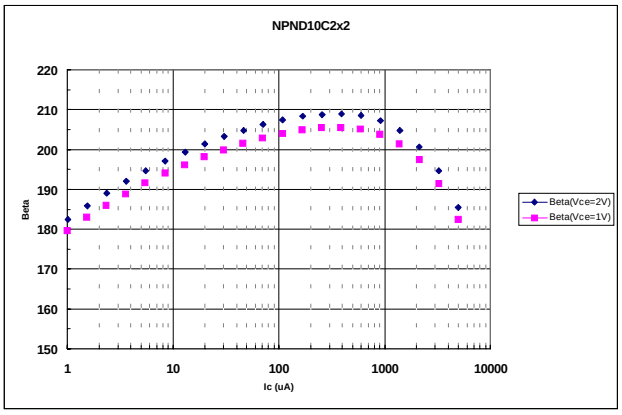

Fig. 11. Transistor current gain β vs. collector current (L_e x W_e = 20 x 1.2 µm^2)

The *ENC* at 12 pF after irradiation is estimated around 350 electrons more than the *ENC* at the same detector capacitor before irradiation. This increase is essentially due to the degradation of the current gain β. In this case, the shot noise source of the base current of the input transistor is as important as the series voltage noise generated essentially by the base resistor. It is possible to reduce the degradation of β by increasing the collector current as explained above.

CONCLUSION

In this paper, a low noise, low power consumption BiCMOS front-end using the radiation hard SOI DMILL process has been presented. An *ENC* noise of 450 electrons at 0 pF with a noise slope of 45 electrons/pF has been obtained for a peaking time of 25 ns, a gain of 90 mV/MIP. The irradiation measurement using a high intensity pion beam with an integration flux of 1.0 x 10^{14}/cm^2 has been performed. With a modification of the feedback device in the preamplifier, the characteristic of the designed front-end circuit will be suitable for use at CMS experiences.

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