Single Event Upset Studies on the APV6 Front End Readout Chip

J Fulcher[*]*, G Hall, M Raymond*
Imperial College, London, UK
D Bisello, A Paccagnella, I Stavitski, J Wyss, A Kaminski
Padova University, Padova, Italy
M French, L Jones
Rutherford Appleton Laboratory, Didcot, UK

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Abstract

The microstrip tracker for the CMS experiment at the LHC will be read out using radiation hard APV chips. During high luminosity running of the LHC the tracker will be exposed to particle fluxes up to 10^6 cm^{-2} s^{-1}. This high rate of particles introduces a concern that the APV could occasionally suffer from Single Event Upset (SEU). In order to evaluate the expected upset rate the APV was run under controlled conditions in a heavy ion beam. The upset cross-sections of the main digital parts of the chip have been measured at two values of incident Linear Energy Transfer (LET). A theoretical prediction of both threshold LET and cross-section is presented along with the experimental measurements.

1. INTRODUCTION

The high radiation environment of the LHC demands that the electronics in the central regions of the CMS detector must be designed to withstand large doses of ionizing radiation. One result of such high rates is to introduce susceptibility to Single Event Effects (SEEs). There are many different SEEs; the one we are interested in is Single Event Upset (SEU), which affects the memory elements of digital circuits.

The CMS collaboration has adopted a readout system based around the APV chip series, a mixed mode amplifier buffer chip with programmable digital control logic. During the research and design phases of the APV chip, much care has been taken to assure a high degree of total dose radiation tolerance. There are two versions of the chip; the APV6, fabricated in the Harris AVLSI-RA Bulk CMOS process [1] and the APVD, fabricated in the DMILL process [2]. Both of these have feature sizes of order 1.2 microns. Extensive testing has been carried out on representative test structures from various processing runs, and the degree of radiation tolerance of these processes has been thoroughly investigated [3]. However, the susceptibility of the APV to SEU is not well known, nor is there much relevant data for comparable types of complex mixed analogue digital chips. A new version of the APV will be fabricated in a 0.25μm technology [4]; therefore future tests will perform a full investigation of the sensitivity of both processes.

With a view to calculating a prediction of the upset rate in the final system, a first evaluation of the SEU sensitivity of the bulk CMOS process has been carried out by placing the APV6 in a beam of heavy ions, at the Tandem accelerator, INFN Legnaro, Italy.

1.1 The APV6

The APV6 front-end chips consist of 128 channels, each of which is made up of a pulse amplifier and shaper that feeds a 160 deep analogue pipeline capable of storing input pulses for up to 4 μs. On an external T1 trigger the data is retrieved from the pipeline and then output, via a 128 : 1 multiplexer. The output stream consists of a set of analogue levels retrieved from all 128 channels and a digital header. This header comprises an error flag and an eight-bit address that indicates which one of the 160 pipeline locations had been marked for readout by the trigger pointer. Control of the various chip operation modes and bias settings is achieved via a standard I^2C serial bus link.

The vulnerable parts of the chip are the digital circuits. In the APV these comprise the digital pointers of the pipeline, the FIFO address memory, the I2C control logic and data registers and other main control logic. In the first evaluation of the SEU vulnerability, upset cross-sections have been measured for the pipeline logic and FIFO combination, and the I2C data registers. The remaining control logic was masked from the beam.

2. THEORY

2.1 The SEU phenomenon

SEU is a non-destructive phenomenon, which affects both dynamic and static memory registers that temporarily store logic states. It manifests itself as a soft error appearing in a device and is caused by the deposition of charge by an ionizing particle.

Depending on the state of the cell, a sufficient injection of charge at points 1 or 2, in Figure 2.1, will cause the state of the cell to invert.

[*] Corresponding author, email jr.fulcher@ic.ac.uk

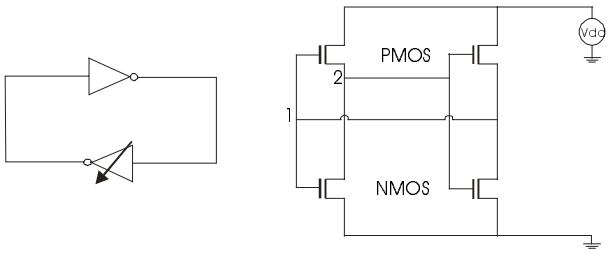


Figure 2.1 Schematic representation of a memory cell composed of two cross coupled inverters, and its circuit description .

In the APV soft errors could cause a variety of undesirable effects, some of which would result in temporary malfunction and possible loss of data. In the event of such errors the APV can be reset and after a latency (~ 3 μs), normal operation would resume.

For an upset to occur two basic criteria must be met. The incident particle must provide a high enough LET[1] (Linear Energy Transfer) in order to free electrons and create a charge deposit larger than the critical charge Q_{crit}, which is the minimum charge required to cause the circuit to invert logic state. The particle must also strike close enough to the sensitive part of the circuit, represented by the arrow in figure 2.1, so that charge can be collected fast enough. The sensitive volume of one memory element is defined as being that volume in which the incident particle must strike to cause an upset, which can be approximated by the drain implant volume of the 'off' NMOS transistor and that of the source of the 'off' PMOS transistor. The combination of these two volumes makes the total sensitive volume. In actual fact the true sensitive volume is larger, the reason for which is explained in section 2.4.

2.2 Upset cross-section

The cross-section, σ, for SEU's is defined at normal incidence as:

$$\sigma = \frac{N_{events}}{\Phi}\left[cm^2\right] \qquad [2.2.1]$$

Where Φ is the total incident particle fluence, and N_{events} is the number of events (SEU) counted during the test. Figure 2.1 shows a typical cross-section curve. In the case of heavy ion irradiation these curves typically represent σ of the device as a function of LET of the incident ions.

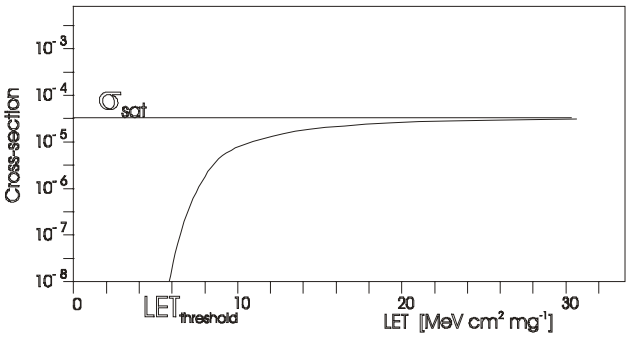


Figure 2.1 A typical cross-section curve.

$LET_{threshold}$ is the minimum LET for which upsets can occur and σ_{sat} is the saturating cross-section for high values of LET. These two defining features of the device behavior can then be used to reconstruct the curve analytically, which enables an interpolated prediction of the upset rate for other forms of radiation. In the case of the CMS tracker, the required calculations are complicated since the incident particles are typically of single charge and therefore only cause large enough ionization by virtue of interactions with silicon lattice sites. Monte-Carlo simulations are required and have been developed at CERN [5].

2.3 Predicting the threshold LET

The critical charge Q_{crit} is estimated by assuming that, in order to cause an upset, the voltage at nodes 1 or 2 in figure 2.1 must be changed by at least half of the difference between logic 0 and logic 1. In the APV logic 0 is at –2V and logic 1 is at 2V, which gives us a required upset voltage of 2V.

The capacitance of these nodes is 30fF (15fF for each transistor gate), Q_{crit} is given by :

$$Q_{crit} = 2V \times 30\,fF = 60\,fC \qquad [2.3.1]$$

Using 3.6 eV per electron, the critical energy required is given by:

$$E_{crit} = \frac{Q_{crit}}{e} \times 3.6 = 1350 \text{ keV} \qquad [2.3.2]$$

We can convert this value into a measure of LET, since the depth of the sensitive volume is small enough to allow us to approximate to the surface LET of the incident particle. The depth, z, is given by that of the epitaxial layer of the device, which is roughly 2 μm. $LET_{threshold}$ specific to the APV6 is given by:

$$LET_{threshold} = \frac{E_{crit}}{z\rho} = 2.9 MeV cm^2 mg^{-1} \qquad [2.2.3]$$

This represents a conservative estimate of the expected threshold LET.

[1] LET is a measure of a particle's rate of energy transfer in a particular material and is given by $LET = \frac{dE}{dx}.\frac{1}{\rho}$, where ρ is the density of that material. All values of LET in this paper refer to energy transfer in silicon.

2.4 Predicting the upset cross-section

The total number of sensitive nodes in the pipeline logic is 960. The surface area of each node is 12×10^{-8} cm^2. Therefore, the total sensitive cross-sectional area of the pipeline logic is:

$$\sigma_{pipeline} = 115\times10^{-6} cm^2 \qquad [2.4.1]$$

For the I2C registers there are 128 sensitive nodes, hence:

$$\sigma_{I2C} = 154\times10^{-7} cm^2 \qquad [2.4.2]$$

These values represent the total physical cross-section of the sensitive volumes in the circuits. In reality the saturated cross-section will be larger than this, since high LET particles striking near the edge of the sensitive volume can create charge clouds.

3. TESTING THE APV6

3.1 Preparation

Before setting up the system in the beam area a preparatory system was set up in the lab at IC. The system reflected all the requirements of the final system, including long cables to run between the beam area and the barracks, vacuum prepared interface cards and cables. The system was tested fully, making data taking runs as if in the beam. The data from these control runs were stored to be accessed for comparison at a later date.

3.2 Hardware

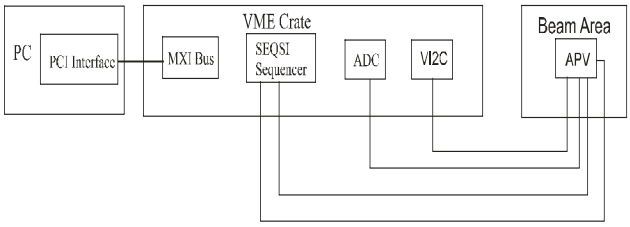


Figure 3.1 Schematic representation of the hardware

The test beam setup was effectively identical to the APV readout chain in the lab. Main control was performed by a PC running LabVIEW, which communicated with the VME crate via a PCI VME interface. The trigger sequence for the APV was provided by a SEQSI sequencer, and control of the APV performed by a VI2C slow control interface. The output from the APV was digitized by a flash ADC.

3.3 Software

The control and data acquisition was carried out by custom designed software developed in LabVIEW. The main tasks were to provide resets and triggers, via the SEQSI, to capture the digitised APV output data frame, via the ADC, to perform rudimentary on-line analysis and to save data to disk. The on-line counting of events was necessary for fine-tuning of the sensitive time in order to ensure that event counting was non-saturated (see section 3.6). Other on-line information included an overall count of upsets and a total sensitive elapsed time counter. The software also included I2C control for testing the APV static registers.

3.4 Masking APV sections

One of the requirements of the system was the ability to mask off sections of the APV. The masks were made from copper plates approximately 1mm thick, to provide an adjustable aperture. This enabled us to select the parts of the chip to test. It was also possible to reduce the upset rate by reducing the exposed area of these parts.

3.5 Seeing upsets

One part of the chip where it was possible to detect upsets, and probably the most useful to test, is the combination of the pipeline logic and FIFO. In the event of an upset there are two possible outcomes: either the error bit in the output data frame is set, or the pipeline address in the output data frame is corrupt. The most likely cause of a corrupted address is an upset changing the pipeline column address stored in the FIFO. The error bit is set if an upset in the pointer logic causes the latency of the trigger pointer to change. Only a small proportion of upsets produce both outcomes simultaneously.

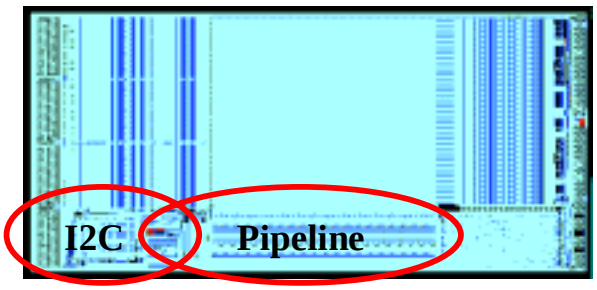


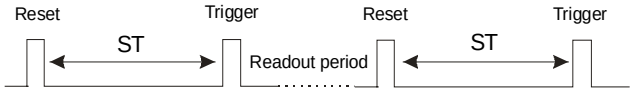
Figure 3.2 Location of tested circuits.

One can also test for events in the I2C registers by writing defined values, reading out the values after a set period of time, and comparing them with initial values. In this case it is possible to detect the individual cells which have been upset.

When measuring upsets in such a chip one has to be careful that upsets do not interfere with chip operation. This can be achieved by exposing only the parts of the chip shown in figure 3.2, masking off the vital control logic and running the chip for short time periods, to ensure only a small number of upsets during each. It is important that the average number of upsets per time interval is less than one (see section 3.6). The running time per measurement, when the chip is sensitive to upsets, is defined as the sensitive time (ST). When measuring the upset rate, following each ST there is a readout period, this is repeated many times to make a

good measurement. For the pipeline a typical run consists of 100,000 STs, and for the I2C, 100.

Figure 3.3 shows the definition of $T_{sensitive}$ the total sensitive time for one run for the pipeline logic.



$$T_{sensitive} = N_{triggers} \cdot ST$$

Figure 3.3 definition of ST for the pipeline logic

3.6 Non-saturated measurements of events in the pipeline logic

One important issue is undercounting of events in the pipeline logic. Only one error can be detected within each sensitive time interval, as more than one error still only produce symptoms consistent with one error. If we lose events by undercounting then the measured upset rates begin to saturate, hence one must ensure that the number of events is less than half the number of sensitive time intervals. In order to achieve this condition one can adjust the length of the sensitive time interval, adjust the upset rate by changing the beam flux (this method is crude and unreliable) or use masking to change the exposed area of the chip.

3.7 The TANDEM Van der Graaf accelerator

The TANDEM is located at the INFN laboratory in Legnaro. Table 3.1 shows the ions that were available for this test and their corresponding LET in silicon.

The TANDEM is capable of producing many more ion species, those in table 3.1 being chosen specifically for this test to cover a useful range of LET values.

Ion	Li	C	O	F	Si	Ni	Ag
LET (MeV.cm^2.mg^{-1})	0.38	1.5	2.9	3.8	8.7	28.7	54.9
Energy (MeV)	55	92	106	116	153	214	259

Table 3.1 Available ions for APV6 test

The typical beam flux was in the range 1x10^4–1x10^7 cm^{-2} s^{-1}. For each ion this value was set to a constant. Due to problems during the experiment there was only enough time to test the APV6 under two ion beams: Oxygen, which had a typical flux of 2x10^6 cm^{-2} s^{-1} and Silicon, which had a flux of 2x10^5 cm^{-2} s^{-1}. The chip was mounted inside a vacuum chamber, which was held at a pressure of 10^{-6} mbar.

4 RESULTS AND CONCLUSIONS

Measurements were made for the SEU cross-section of both the pipeline and I2C logic at two values of LET using Oxygen and Silicon ions. For Oxygen a large number of readings with high fluence were made and no upsets were observed. Thus it can be deduced that the threshold for both pipeline and I2C logic is above 2.9 MeV.cm^2.mg^{-1}. Silicon, on the other hand, produced a significant upset rate, giving the following results.

4.1 Error distribution

In order to be confident that events observed were caused by the ion beam, the distribution of these events with time was measured. For random processes the distribution should be described by Poisson statistics.

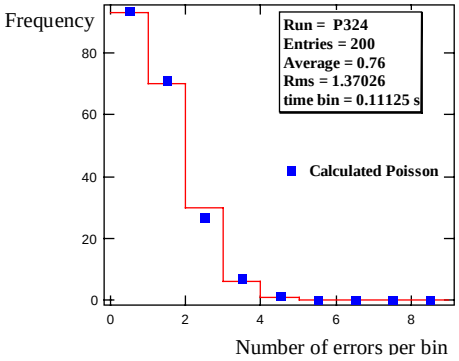


Figure 4.1 SEU distribution for pipeline logic

Figure 4.1 shows a typical distribution of 200 SEUs observed in the pipeline logic. All data showed a good fit with Poisson statistics.

4.2 Pipeline cross-section

These data represent errors in the pipeline logic only, which are identified as having caused the error bit to be set in the APV6 data header. All of the results that follow were made with a ratio of SEUs to number of sensitive time intervals ~ 1/1000. Under these conditions one would expect the upset cross-section to show no dependence on the sensitive time.

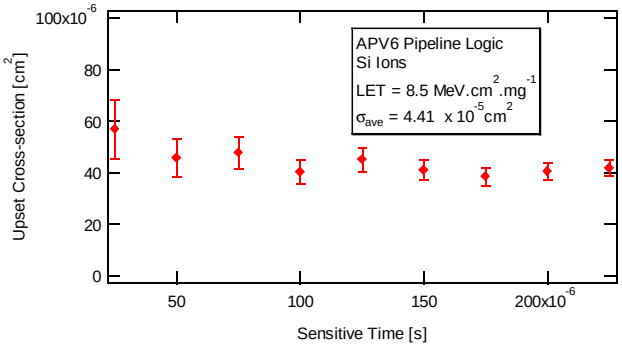


Figure 4.2 Variation of cross-section with sensitive time

Figure 4.2 confirms this expectation within an acceptable statistical variation, with the average cross-section of (4.4 ± 0.2) x 10^{-5} cm^2.

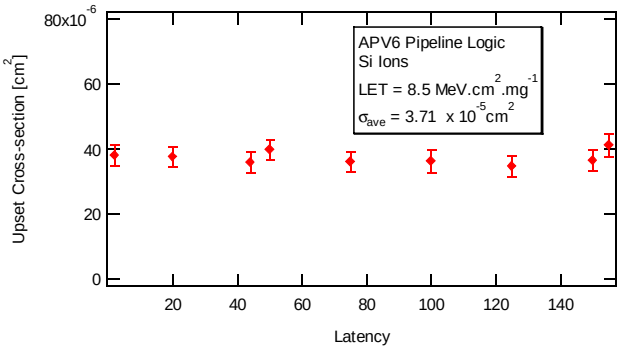


Figure 4.3 Variation of cross-section with latency

A similar test was made by varying the latency of the trigger pointer. Again one would expect to see no variation in the cross-section, and figure 4.3 shows that the measured value varies very little, with an average of $(3.7 \pm 0.1) \times 10^{-5}$ cm^2.

If one assumes the cross-section to be constant at one value of LET, the average of all measurements for the cross-section of the pipeline logic can be taken as a first estimate, this gives $(4.1 \pm 0.1) \times 10^{-5}$ cm^2.

4.3 I2C registers cross-section

Similar measurements made for the upset cross-section in the I2C registers again show consistent results with variation in the sensitive time. Figure 4.4 shows the average cross-section to be about $(1.5 \pm 0.9) \times 10^{-5}$ cm^2.

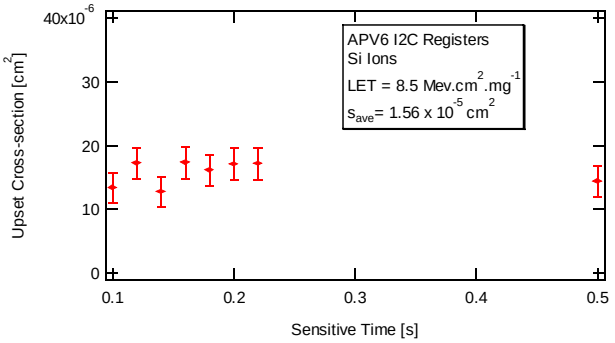


Figure 4.4 Variation of cross-section with sensitive time

4.4 Discussion and future measurements

With only two measurements of cross-section it is impossible to draw a curve of cross-section against LET. Figure 4.5 shows a possible range in which the curve could lie, illustrating the uncertainties that still remain.

It is clear that more points are needed in order to make an accurate measurement of the saturated cross-section, and the threshold LET. From figure 4.5 the threshold lies between 2.9 and 8.5 MeV cm^2 mg^{-1}.

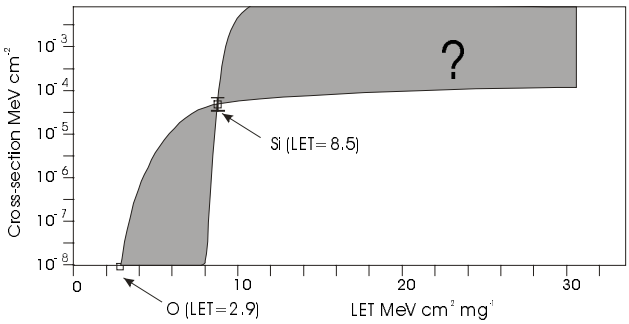


Figure 4.5 Possible range for the cross-section curve

Table 4.1 shows a comparison between the predictions in section 2 and the measurements above.

	Prediction	Measured
Threshold LET (MeV.cm^2.mg^{-1})	2.9	2.9 – 8.5
Cross-section I2C (cm^2)	1.5×10^{-5}	$1.5 \pm 0.9 \times 10^{-5}$
Cross-section Pipeline (cm^2)	1.2×10^{-5}	$4.1 \pm 0.1 \times 10^{-5}$

Table 4.1

Tests to complete the measurements are planned for later this year. This will then enable extrapolation to CMS to be made and a prediction for the expected upset rate in the tracker. We also intend to test the APV25S0, the new version of the chip fabricated in a 0.25 micron process.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

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