DEVELOPMENT OF AN OCTAL CMOS ASD FOR THE ATLAS MUON DETECTOR

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Abstract

Development of a CMOS amplifier/shaper/ discriminator for the ATLAS Muon detector is presented. The first phase of this work has resulted in a simplified 4-channel device (ASD-lite) fabricated in HP 0.5μm n-well CMOS operating at 3.3 volts. Highly accurate DC models resulted in performance which closely matches SPICE predictions. On-chip crosstalk, a parameter not easily simulated, is measured to be below 0.5%. Results of chip measurements and on-chamber tests will be presented. This device will be used for early testing of ATLAS MDT (Monitored Drift Tube) modules. Further work on the final octal MDT-ASD, which will be fully programmable and include Wilkinson leading edge charge measurement, will be presented.

Front End Requirements

The Muon spectrometer aims for a P_T resolution of 10% for 1TeV muons. This translates into a single wire resolution requirement of <80μm. The average drift velocity is about 20μm/ns, which implies a systematic timing error for an individual tube of about 500ps.

The planned gas gain is low, about $2 \cdot 10^4$, to avoid aging problems. The expected signal (collected charge) is roughly 1500 electrons (0.25fC) per primary electron, so good position resolution requires a low noise front-end.

A specified preamp peaking time of 15ns is a good compromise in terms of resolution and stability [1]. The channel to channel crosstalk is specified to be less than 1%. The high count rates of up to 400kHz/wire together with the long electron drift times require either a bipolar shaping scheme or active baseline restoration to avoid resolution deterioration due to baseline fluctuations.

At the time of the TDR[2] the baseline MDT gas was $Ar/N_2/CH_4$ 91/4/5 (3 bars absolute) which is very linear and has a maximum drift time of 500ns. The choice for the ASD shaping scheme was unipolar shaping with active baseline restoration[3] for the following two reasons. First, it allows the measurement of the signal trailing edge[4 5], which has a fixed latency with respect to the bunch crossing, with an accuracy of about 20ns. Second, it avoids multiple threshold crossings per muon track, which would increase the hit rate and therefore the readout occupancy.

Aging problems with all MDT gases containing hydrocarbons caused a change of the baseline gas to Ar/CO_2 93/7 (3 bars absolute) which has a maximum drift time of 800ns and is very nonlinear[6]. The long drift time and the non-linearity degrade the trailing edge resolution to about 80ns and cause multiple threshold crossings even for a unipolar shaping scheme[7]. We therefore have adopted a bipolar shaping scheme since it does not require an active BLR and also does not require programmable filter time constants. To avoid multiple hits from multiple threshold crossings for a single signal we introduce a fixed dead time equal to the maximum drift time. It was shown that the overall increase in dead time does not cause a degradation of the pattern recognition efficiency[8].

An ADC will measure the signal charge in a 20ns gate following the threshold crossing time. The charge is then encoded into a pulse width in the usual Wilkinson technique. This information allows a resolution improvement by performing a time slewing correction. Additionally, it is useful for diagnostics and monitoring purposes and might also be used for dE/dx identification of slow moving heavy particles like heavy muon SUSY partners.

Two modes of operation will be provided. In one mode the ASD output gives the time over threshold information, i.e. signal leading and trailing edge timing. The other mode measures leading edge time and charge and is considered the default operating mode.

Readout System Packaging

The ATLAS MDT system consists of about 350,000 pressurized drift tubes of 3cm diameter, with lengths from 1.5 to 6m. The MDTs are read out by an ASD at one end, and the other end is terminated in the characteristic impedance of the tube (380Ω). The preamp input impedance is a relatively low ~100Ω to maximize collected charge. To minimize cost, the MDT signals are carried on two-layer "hedgehog boards" to a mezzanine board, which contains 24 readout channels: 3 Octal ASDs, a single 24-channel TDC, and associated control circuitry.

A single MDT chamber may have as many as 432 drift tubes or 18 hedgehog/mezzanine board

sets. Data are read out of each TDC individually via a 40Mbit/sec serial link to a single CSM (Chamber Service Module) which multiplexes the (up to) 18 serial links into a single optical fiber for transmission to the ATLAS DAQ. A daisy-chain JTAG bus permits downloading of parameters to ASDs and TDCs and triggering of test/calibration pulse injection.

Each superlayer (3 or 4 layers of individual tubes) is entirely enclosed in a faraday cage shield at both ends. All AC signals entering or leaving the shield are low-level differential signals (LVDS). All DC signals are filtered at the shield entry point.

Each complete MDT chamber is electrically isolated from the support structure, and all services (gas, electrical, etc) are also electrically isolated or floating at the source. The MDT chambers will be individually grounded in a controlled way to a single common ground point.

ASD Overview

The chip is fabricated in HP 0.5μm CMOS operating at 3.3V. The analog structure of each channel of the ASD is shown in Figure 1.

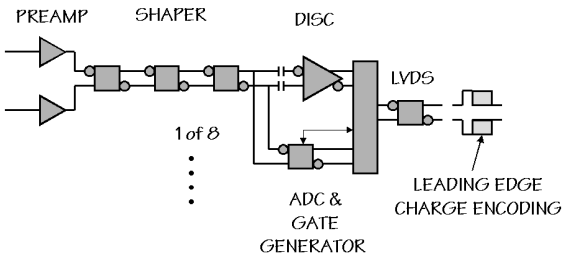

Figure 1: ASD block diagram

It is a fully differential structure with a pair of identical preamplifiers at the input[9], a shaper stage, followed by a discriminator leading edge charge integrator to be described later. The second preamp provides DC balance, common mode pickup rejection and improved power supply rejection.

Some important specifications are:

- Input impedance : $Z_{IN} = 120\Omega$
- ENC = 5000e rms or ~3.5 primary electrons
- Shaper peaking time = 15ns
- Sensitivity at shaper output :
  3mV/primary electron (gas gain $2 \cdot 10^4$)
  or 12mV/fC referred to delta function into terminated MDT
- Linear range ~1.5V or 500 primary electrons
- Nominal threshold setting : ~60mV or 20 primary electrons (~ 6 σ_{noise})

SPICE simulation using bsim3V3 models supplied by MOSIS closely match the measured chip parameters.

Preamp

Each preamp is an unfolded n-channel cascode structure, shown in Figure 2, with large input FET M1 of W/L = 2400μm/0.9μm running at 1mA drain current. Current is determined by the p-channel cascode current source, M3/M4. Impedance at the hi-Z node is set by R1. Bias voltages are provided by a bias network (not shown) which is common to all preamps on the chip, but bypassed externally to ground with large capacitors. This insures minimal crosstalk through the bias network (<0.25% measured).

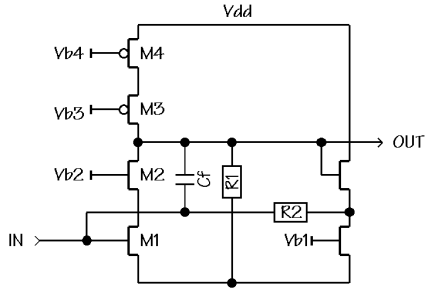

Figure 2: Cascode n-channel preamp

Input impedance at low frequencies is determined by open loop gain ($g_m \cdot R1$) and feedback resistor R2. At high frequencies, it is determined by g_{m1} and feedback and stray capacitance. Resistors and capacitors are chosen so that both are equal to 120Ω in spice simulation. Owing to the accuracy of the bsim3V3 models, measured DC and dynamic pulse input impedance are very close to this value

Since the MDT is terminated at its far end, the termination dominates the noise[10] with an additional 30% coming from the preamp.

Shaper

The shaper consists of three near identical differential amplifiers. The first serves only to provide gain and make the signal completely complementary. The basic differential amplifier is shown below in Figure 3.

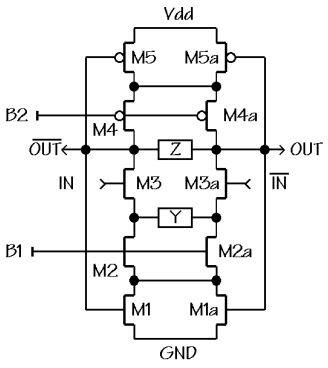

Figure 3: Basic differential amplifier

The basic transconductance element is the transistor pair M3/M3a with transfer function given approximately by the product of the drain impedance Z, and the source admittance Y (modified somewhat by M3/M3a source impedance). Thus the network can be configured for a variety of desired transfer functions including gain in which both Z and Y are resistive elements, and bipolar shaping stages in which Z is resistive and Y is a series R-C. Bandwidth of each stage is dominated by the product of Z and the load capacitance, typically the gate capacitance of the subsequent stage as well as drain capacitance of M3, M3a, M4, M4a. Typically each stage adds approximately 3–4ns to the total peaking time and is consistent through multiple chip submissions.

The DC operating point is constrained by common mode feedback. This is formed by the upper and lower transistor pairs M5/M5a and M1/M1a operating in their diode region as voltage controlled resistors. Typically these pairs operate with V_{DS} of order 50mV and so very little of the 3.3V supply is given up to their operation. The value of the DC operating point is set by a simple bias network (not shown) controlling the B1/B2 nodes to be $V_{DD}/2$ or 1.65V. Both Monte Carlo simulations and chip measurements indicate that this value is quite process independent and is thus quite accurate, typically ±25mV. The common mode and differential bandwidths of this circuit are approximately the same. This insures, for example, that the output of the first differential amp after the preamp is almost completely complementary with very little common mode component. The stage has very low common mode gain and thus good rejection to substrate induced noise pickup throughout the shaper stage. Probe station measurements indicate that substrate noise coupling from the digital circuits after the discriminator, into the preamp shaper stages is at the few mV level at the shaper output and is considered negligible.

Wilkinson ADC

The Wilkinson ADC serves as a time slew correction and also provides diagnostics for monitoring chamber gas gain. It operates by creating a gate of approximately 20ns width at the leading edge of the signal, integrating charge onto a holding capacitor during the gate, and then running down the hold capacitor at constant current. The rundown current is chosen so that maximum rundown time is of order 100ns. The simplified circuit is shown below (Figure 4).

The Wilkinson cell is fully differential and uses the same differential transconductor as the shaper stage as floating current sources, both for the integration current source, as well as the rundown current sink.

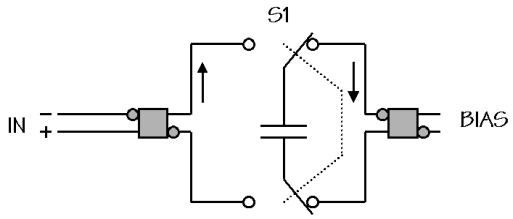

Figure 4: Wilkinson ADC

A simplified diagram of the logic for this cell, the gate generator, is shown in Figure 5.

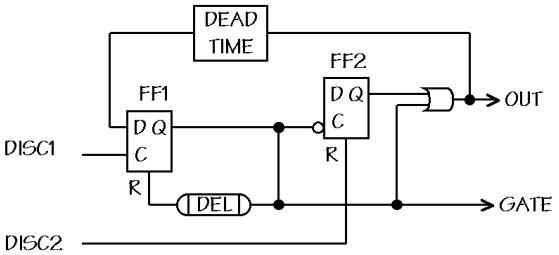

Figure 5 : Wilkinson gate generator

Both flip-flops are D–type with asynchronous reset. Disc1 and Disc2 refer to the main (timing) discriminator and a second discriminator, which is placed across the hold capacitor of the Wilkinson cell. The input flip-flop, FF1 is configured as a one-shot via the delay element marked DEL. On firing of Disc1, a fixed pulse is thus generated which gates current into the hold capacitor and causing Disc2 to go above threshold. At the trailing edge of the Gate, flip flop FF2 fires enabling the rundown. When the hold capacitor goes below threshold, FF2 resets and the Output pulse is terminated. The box labeled "Dead Time" contains delay elements and logic to preclude re-firing of FF1 both during the current cycle and for a fixed delay afterward. In the final version of the chip, this delay will be programmable over the entire drift time of the MDT, or up to ~1μs.

Unlike the logic for configuring the ASD, the gate generator logic runs during normal MDT operation and so must not induce substrate noise or crosstalk into the analog sections. To insure this, the logic sub-circuits are all fully differential and are bypassed on chip with respect to the power rails. Each logic transition is accompanied by a complement in very close proximity. The logic cells are therefore individually designed and are not standard cell logic.

Preliminary test results of the Wilkinson integrator (just received as of this writing) closely match SPICE predictions. Pulse width dependence on leading edge charge is as expected and substrate coupling from the logic cells is minimal.

Timing Discriminator

The Discriminator is implemented as a differential amplifier with gain of about 5 driving a comparator with hysteresis, as shown in Figure 6. The shaper output is AC-coupled to the diff-amp input, and the discriminator threshold is applied there as an external DC voltage. The diff-amp is very similar to those used in the shaper and described above. The comparator will be described in more detail here.

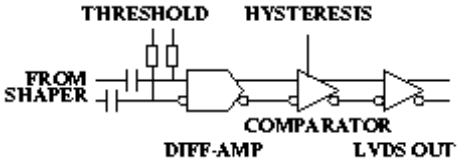

Figure 6: Timing discriminator block diagram

The comparator is a high-gain differential amplifier with symmetrical current-mirror loads. The main differential pair (M1, M2) is biased at 400μA. Two current-mirror loops provide a differential output. The voltage gain is about 500 with no hysteresis. A simplified schematic is shown in Figure 7.

Hysteresis is provided by (M1A, M2A) which unbalance the static current through the main differential pair by a variable external current, shifting the effective discriminator threshold by up to 100mV. Positive feedback from two inverters reverses the threshold offset polarity when the discriminator fires.

The bias currents for the main differential pair and the hysteresis pair are provided via current mirrors. The main bias current is set at about 400μA using a poly resistor; the hysteresis is controled by an external current.

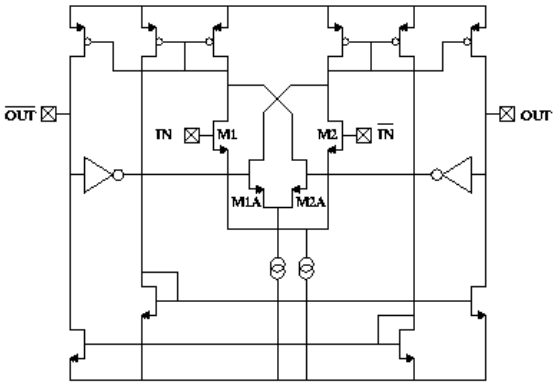

Figure 7: Comparator schematic

LVDS Output

This cell[11], shown in Figure 8, provides a low-level logic output with a nominal swing of 200mV differential into 100Ω centered at 1.2V. This corresponds to the "reduced range link" described in IEEE 1596.3 (the LVDS standard). The circuit is designed to be compatible with a specific receiver (the AMT TDC) and should also be compatible with commercial LVDS receivers. No claim is made that it complies fully with the standard for an LVDS transmitter.

Differential drive is provided directly from the discriminator outputs to two moderately sized inverters. These inverters drive the output stage, which is essentially a pair of current-starved inverters (M1/M2) and M3/M4), with their output current limited by transistor pairs operating in their resistive region (M5-M8). Common-mode feedback from the outputs to the current-limiting FETs sets the common-mode output voltage.

The DC characteristics are set entirely by transistor sizes and are thus subject to process variations. Observations on a small number of fabricated devices largely agree with Monte Carlo SPICE simulations and are compatible with the intended TDC receivers.

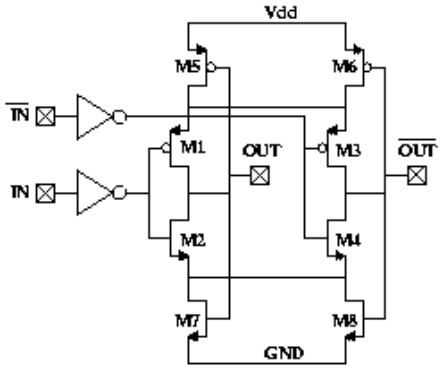

Figure 8: LVDS output schematic

Crosstalk and Substrate Noise

Early prototype multi-channel ASD chips showed significant crosstalk of a few percent. This crosstalk was diagnosed as caused by noise coupled to the chip substrate, and subsequently "broadcast" throughout the device. Several remedial measures were taken in subsequent prototypes, and the crosstalk is now below measurable levels (less than 0.5%).

Two distinct types of crosstalk were observed: "Analog" crosstalk – differentiated, proportional to input charge, affecting only neighboring channels and "Digital" crosstalk –in response to discriminator firing, essentially independent of distance from source. A chip fabricated with HP 0.5μm process consists of a heavily-doped silicon substrate about 500μm thick with resistance of about 1Ω/□, overlaid by a lightly-doped epitaxial layer about 6 μm thick with a much higher resistance of 33kΩ/□, with the active circuitry

above this. According to the literature[12] the substrate in this type of device can be treated as a single circuit node for analysis purposes, and can couple signals between widely separated subcircuits. In our original prototypes no particular care was taken to prevent this.

Remedial measures included the following: A balanced, differential circuit topology was adopted throughout the design, both to reduce susceptibility of sensitive subcircuits and to reduce radiated noise. The LVDS output driver switches by far the largest currents in the device, and was found to radiate substantial noise. Series resistors were added to degenerate the power supply connections to this subcircuit. Diffused guard rings (with closely spaced contacts) were added around all circuits (digital and analog). For the digital circuits, the guard rings were always placed within 8μm (the thickness of the epitaxial layer) of active transistor area. Guard ring connections were brought out to separate bonding pads, though it was not found necessary to isolate them outside the IC package. Separate bonding pads were provided for digital power, analog power and bias circuit bypass capacitors.

Many remedial measures were taken and the measured crosstalk was consequently minimized. It was not practical to measure the effectiveness of each modification individually.

Programmability

Many features of the MDT-ASD will be programmable. They fall into three broad categories and are summarized in Table 1. The adjustments are sent to the ASD as a serial bit-stream using JTAG or a similar protocol.

Operating Point	Testing, Cal.	Failure/Malfunc.
Timing Disc. Threshold	Pulse Injection (8 levels)	Dead Time Adjustment
Timing Disc. Hysteresis	Output Boundary Scan	TOT output mode
ADC range		Channel disable

Table 1. ASD programmable features

The data are converted to physical quantities by custom Digital-to-Analog Converter cells (DACs). According to the requirements, two types of DACs are used: Resistor chain voltage output converters (VDAC) and switchable scaled-transistor current mirrors (CDAC). Figure 9 shows the schematic of an 8-bit VDAC. The converter is implemented using a two-stage scheme (2×16-resistor chains). The range is applied to the RN (negative) and RP (positive) terminals. The 4 MSBs [b7:b4] switch the specified segment of the total range to the second chain, which puts out the selected voltage to the DACOUT terminal according to the LSBs [b3:b0]. Resistor chain DACs are inherently monotonic and exhibit good linearity, depending mainly on transistor and resistor matching of the fabrication process. For the used 0.5μm minimum feature size process, the final layout of the cell has the dimensions 280μm × 250μm. A DAC of this type is used to set the threshold of the main timing discriminator within a range of 0 to 4 times the nominal value (60mV) with a resolution of 1mV.

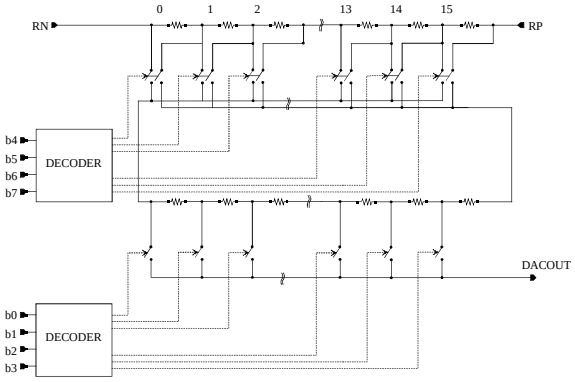

Figure 9. 8-bit Voltage DAC schematic

The CDACs supply their output currents directly to current mirrors in the respective cells. In order to meet the stringent requirements for the gate voltages of the mirror transistors, "bootstrap" references are used[13]. With the use of this reference circuit, a variation of less than ¼ LSB at full count for the output current of a 4-bit CDAC at a power supply change of 10% in both directions was achieved (Figure 10). The reference current varies −0.4% (for VDD − 10%) and +1.4% (for VDD + 10%).

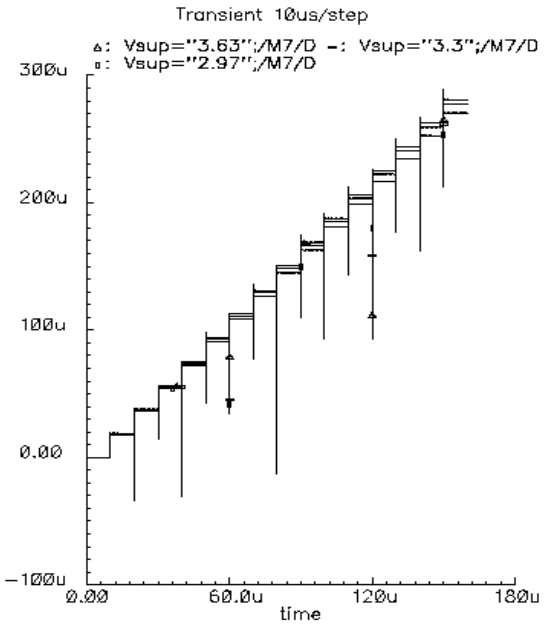

Figure 10. Simulation of a 4-bit CDAC at VDD nominal and ± 10%.

Converters of this type control the hysteresis of the main discriminator as well as gate width, run-down current and dead time of the Wilkinson ADC cell.

Test Results

The ASD Lite chip was extensively tested on an 8×3 tubes chamber prototype in a cosmic ray setup. The chip proved to be unconditionally stable on this setup.

Figure 11 and Figure 12 show the analog output signal and the discriminator signal for a cosmic muon (ASD lite). Note that this is a signal from a single muon track. The 'spiky' structure is due to charge deposit fluctuations along the track.

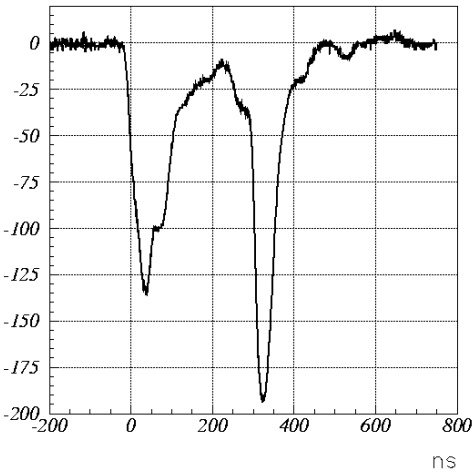

Figure 11: Analog signal from a cosmic ray muon (ASD Lite)

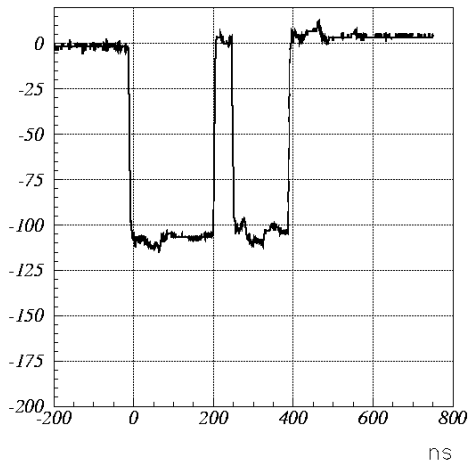

Figure 12: Discriminator output for the above signal

A prime issue is chip protection against high voltage discharges close to the preamp input. It was verified that, with an appropriate input protection circuit on the Mezzanine card, the chip could survive multiple full chamber discharges.

The overall channel to channel crosstalk was measured to be <0.7%.

Figure 13 and Figure 14 show a TDC spectrum from cosmic muons and an ADC spectrum from a radioactive source, which was obtained by integrating the analog output pulse from the scope trace (DSO).

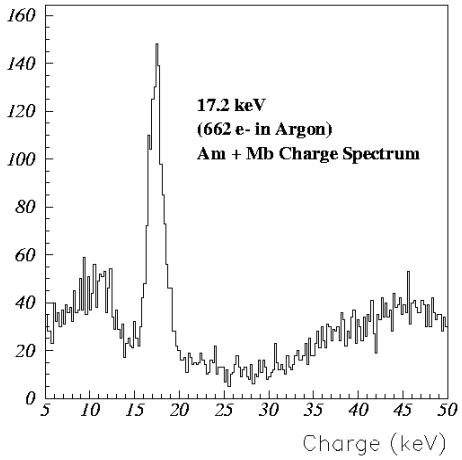

Figure 13: ADC spectrum from a radioactive source

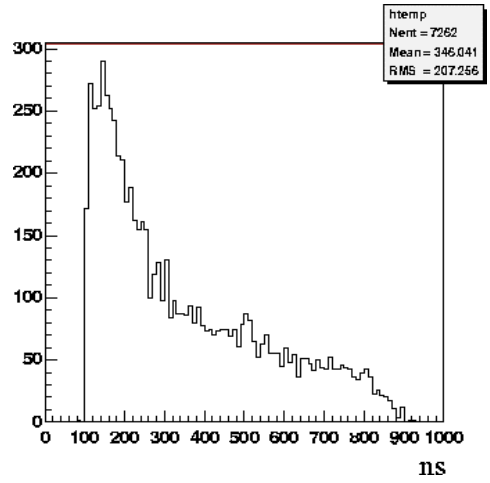

Figure 14: TDC spectrum from cosmic muons

Conclusions and Future Plans

A four-channel all-CMOS ASD has been designed, fabricated and tested extensively on ATLAS MDT detectors. A fully-programmable eight-channel ASD is under development. Roughly 50,000 packaged ASDs will be produced, starting in 2001, for the ATLAS experiment.

References

[1] W. Riegler, "MDT resolution simulation, Fronted electronics requirements" ATLAS note ATL-MUON-97-137 (1997) CERN

[2] ATLAS Muon Spectrometer Technical Design Report, CERN/LHCC/97-22, ATLAS TDR 10, (1997)

[3] W. Riegler "Front end electronics of the ATLAS precision muon drift chambers" 3rd Workshop on Electronics for LHC Experiments, London, England, 22-26 Sep 1997

[4] C. Blocker et al, “Signal Processing and Front End Electronics for the ATLAS Muon Detector” Proceedings, 1st Workshop on Electronics for LHC Experiments

[5] J. Shank, J. Oliver, T. Mann “Trailing Edge Timing Studies with Prototype ATLAS Muon Drift Tubes”, Proceedings 1st Workshop on Electronics for LHC Experiments.

[6] M. Aleksa, W. Riegler "Non-Linear MDT Drift Gases like Ar/CO2 as MDT drift gases" ATLAS note ATL-MUON-98-268 1998 CERN

[7] W. Riegler, M. Aleksa "Bipolar versus unipolar shaping of MDT signals" ATLAS note ATL-MUON-99-003 (1999) CERN

[8] M. Virchaux, J.F. Laporte, Reconstruction Efficiency and Dead Time” Unpublished internal Muon document

[9] F.M. Newcomer, S. Tedja, R. Van Berg, J. Van der Spiegel, H.H. Williams, IEEE Nuc. Sci. NS-40 (4) 1993

[10] C. Blocker, J. Huth, J. Oliver “Noise Considerations for the ATLAS Muon Detector” ATLAS Muon Note Muon-No-080 (1995)

[11] The authors gratefully acknowledge conversations with O. Milgrome who suggested this topology.

[12] N. Verghese, T. Schmerbeck, D. Allstot, “Simulation Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits”, Kluwer, 1998.

[13] P. Allen, D. Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 1996