

used on a wide variety of commercial off-the-shelf VME carrier boards. The FED-PMC is thereby able to benefit naturally from the constant improvement in carrier processing performance. With an appropriate interface card it can also be plugged directly on to the PCI bus of a PC or workstation.

The PMC implementation provides a cost effective solution for instrumenting detectors in test beam and laboratory setups. Software drivers are provided in order to hide the complexity of the card's functionality and enable users to install and operate FED-PMC's in a "plug and play" fashion.



Figure 2: Photograph showing both sides of the FED-PMC (Mk2 version).

2.2 Functionality

A diagram indicating the basic functional units of the FED-PMC is shown in Figure 3. The card has 8 electrical input channels which can be configured at assembly for either differential or single-ended inputs. Each channel utilises commercial ADCs [8] and is capable of digitising 9 bits² at clock speeds from between 2 and 40 MHz.

The data is stored in contiguous blocks inside a Dual Ported Memory (DPM). The DPM is implemented as 4 x 64K x 18 bit synchronous memories [9] and is capable of buffering the raw data from approximately 250 APV frames. The data is read out (can be simultaneous with ADC capture) over the PCI bus via a 32 bit, 33 MHz commercial bridge interface [10]. A FIFO provides storage for event buffer pointers and event counter information.

² The ADCs are 10 bit, the LSB is not read out.

A CPLD implements the clock and trigger control. Trigger and clock (LVDS) signals can be brought in via the front panel or optionally through the PCI backplane. The fine adjustment of the clock phase with respect to the data can be set under software control in order to obtain the optimum sampling point at the ADC. For testing purposes triggers can be generated internally by software and the card can run from the internal PCI clock (33 MHz).

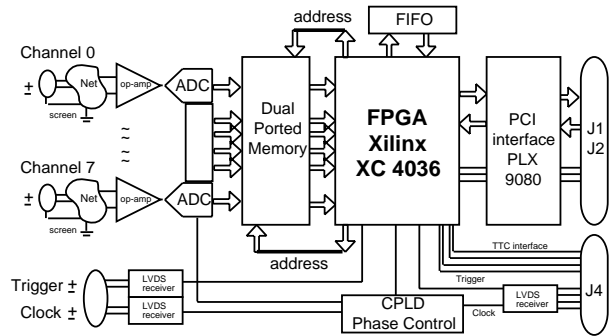


Figure 3: Block diagram of the FED-PMC.

2.3 Firmware

At the heart of the FED-PMC design is an FPGA [11]. This permits a large fraction of the card's functionality to be re-configurable in firmware and thereby maintains a flexible hardware architecture.

The basic firmware design configures the FED-PMC to provide raw data capture in a "digital scope" mode. VHDL blocks implement the following functions:

- Local data and address bus (slave)
- DPM interface
- Event buffer management
- FIFO and counters control
- Register interface
- Test functions

The flexibility of the FPGA based approach is demonstrated by the number of extensions to this core design which are in various stages of development for the microstrip tracker readout:

- APV Auto-Synchronisation mode : permits ADC data capture to be triggered on recognition of a header word which accompanies the APV data stream itself rather than on the external trigger.
- Data Generator mode : for exercising the interface to the higher levels of the DAQ using test patterns at high rate, (requires on-board DMA).
- Hit Finding mode : implementing pedestal and common mode subtraction with basic cluster finding³.

³ It should be noted that the original specification of the FED-PMC provided by the tracker detector groups did not require hit finding capabilities.

The precise algorithms employed depend on the type of microstrip detector being readout.

Core VHDL libraries are provided for those users wishing to develop their own FPGA designs.

During normal operation the FPGA is loaded on power up under software control from an on-board Flash memory. The memory can be reloaded with a new FPGA design via a local area network using the software tools provided. This permits FPGA design updates to be distributed from a central source and reloaded in situ. The FPGA can also be loaded directly from the network for testing of new designs without overwriting the Flash memory contents.

2.4 Software

The FPGA-based open hardware architecture, described in the previous section, is complemented by the design of the software architecture which forms an integral part of the delivered FED-PMC package. The software design follows a layered approach from the lowest-level drivers right up to a full graphical user interface.

A layered design (Figure 4) has several advantages for the end user:

- It abstracts the details of the hardware implementation. At the simplest level a handful of routine calls are required for card configuration and readout operation.

- It removes the need to rewrite code which has already been debugged in parallel with the hardware⁴.

- It permits upgrades to the firmware to be transparently implemented. The firmware contains a version identifier permitting the software to recognise the design currently installed and operate accordingly.

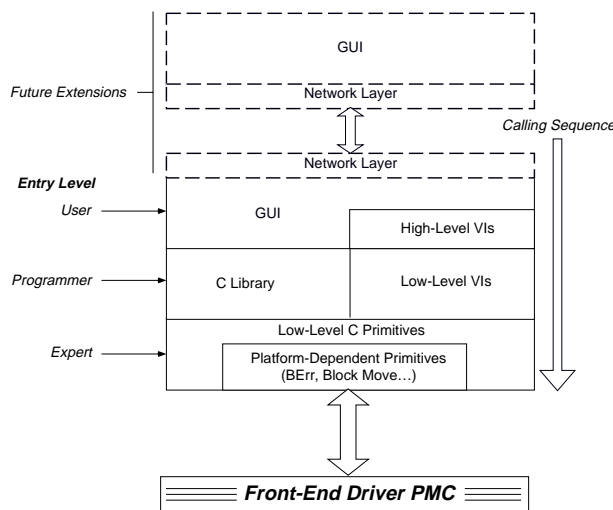


Figure 4: Layered Software Design.

⁴ If the end user chooses to implement their own firmware design they must of course produce the necessary software to operate it.

The software is implemented by a comprehensive library of (open source) C routines. A high-level graphical user interface implemented using LabView [12] has also been developed for the test bench at RAL.

2.5 Operating Environments

The FED-PMC has so far been operated in the following environments:

- CES RIO2 PowerPC Single Board Computer (SBC) running with either LynxOS or VxWorks operating systems.

- Motorola MVME2604 PowerPC SBC running LynxOS.

- VMETRO MIDAS-20 PMC carrier.

By using appropriate extender cards up to 6 FED-PMC's, providing a total of 48 ADC channels, can be operated from one SBC.

Each FED-PMC occupies a total of just over 1 MByte of PCI memory space.

3. FED-PMC STATUS

3.1 CMS Tracker Beam Tests

The first FED-PMC's (Mk1) were produced during summer 1998 and commissioned during tracker test beam running at the CERN PS in October 1998. A second version (Mk2) of the card was used extensively during further beam tests at CERN during May and August 1999. Several FED-PMC's were integrated into the test beam DAQ system in a matter of a few hours and operated successfully, and without further expert intervention, throughout the data taking period.

A total of 20 Mk2 cards have recently been distributed to the CMS microstrip tracker community. The card will also be used for prototyping tests of the CMS Pixel Vertex detector.

3.2 Applications outside CMS

The CMS FED-PMC is also being employed by groups working on readout prototypes for the RICH and tracker detectors of the LHCb experiment [13].

The suitability of the FED-PMC for a medical imaging application is currently under study at Imperial College London, UK.

4. ADDITIONAL INFORMATION

The software tools and source libraries together with further information on the FED-PMC can be found at http://hepnts1.rl.ac.uk/CMS_fed/Default.htm.

5. CONCLUSIONS

The challenge of providing a flexible, cost effective and easy to use ADC card for the prototyping requirements of the CMS tracker community has been met by the employment of the following standards :

- Hardware : PMC (PCI bus) running on commercial carriers

- Firmware : FPGA with VHDL libraries

- Software : C drivers with high level user interface

The FED-PMC has been used successfully for CMS microstrip tracker detector evaluation studies during beam tests at CERN.

The versatility of the design has been demonstrated by the employment of the FED-PMC in applications outside of CMS.

6. ACKNOWLEDGMENTS

The Mk1 FED-PMC was designed at RAL with the assistance of P. Burch.

The authors also wish to thank Dr. Gareth Noyes for his advice on software design and W. Beaumont for his assistance during the tracker beam tests at CERN.

7. REFERENCES

- [1] The Compact Muon Solenoid, Technical Proposal, CERN/LHCC 94-38.
- [2] The CMS Tracker Project, Technical Design Report, CERN/LHCC 98-6.
- [3] F.G.Sciacca et al., "Readout of Micro Strip Gas Chambers for the CMS Central Tracker with the APV6 Front-end Chip" *Fourth Workshop on Electronics for LHC Experiments*, CERN/LHCC/98-36.
- [4] L.L. Jones et al., "A 128 Channel Analogue Pipeline Chip for MSGC Read-out at LHC" *Fourth Workshop on Electronics for LHC Experiments*, CERN/LHCC/98-36.
- [5] B.G. Taylor, "Timing Trigger and Control distribution for LHC detectors" *First Workshop on Electronics for LHC Experiments*, CERN/LHCC/95-56.
- [6] R. Halsall et al., "Front End Readout Developments in the CMS Data Acquisition System" *Third Workshop on Electronics for LHC Experiments*, CERN/LHCC/97-60.
- [7] PCI Local Bus Specification, Revision 2.1, PCI Special Interest Group Draft Standard for Common Mezzanine Card Family CMC, IEEE P1386, Draft Standard for Physical/Environmental Layers for PCI Mezzanine Cards, IEEE P1386.1.
- [8] SPT7861 manufactured by Signal Processing Technologies, Inc., 4755 Forge Road, Colorado Springs, Colorado 80907, USA. <http://www.spt.com/datasheets/datasht1.html>
- [9] MCM69D618 manufactured by Motorola, Inc., <http://motorola.com/sps/>
- [10] PLX PCI9080 manufactured by PLX Technology, Inc., 390 Potrero Ave., Sunnyvale, CA 94086, USA. <http://www.plxtech.com/products/prodset.htm>
- [11] XC4036XL manufactured by Xilinx Technologies, Inc., 2100 Logic Drive, San Jose CA 95124-3400, USA. <http://www.xilinx.com/products/xc4000xl.htm>
- [12] LabView manufactured by National Instruments, Inc., 6504 Bridge Point Parkway, Austin, TX 78730-5039, USA.
- [13] LHCb, Technical Proposal, CERN/LHCC 98-4 LHCC/P4.