Trigger implementation in the KLOE experiment

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Abstract.

The KLOE detector at present under operation at the Frascati phi-factory DAΦNE is a general-purpose detector for the study of CP violation in the neutral kaon system.

The KLOE trigger uses signals from both the electromagnetic calorimeter and the central drift chamber.

Within 150 ns after an interaction the calorimeter and the drift chamber provide a set of signals which form the basis of the trigger decision.

The design of the modules providing the trigger decision for each sub-detector, the final trigger decision together with the modules for distribution and synchronization in the experiment is presented.

Particular emphasis will be given to the presentation of the use of modern design methodologies that could be also implemented for the realization of electronics for LHC experiments.

Outlook

The KLOE trigger uses signals from both the electromagnetic calorimeter and the central drift chamber.

The final trigger decision and the its distribution are performed by VME modules with two data acquisition interfaces: The VME one and a custom designed KLOE AUX-bus backplane.

VME is used for setting and calibration purposes, while the AUX-bus provides the interface the data acquisition system.

Monitoring of the data at each stage of triggering process is necessary for data consistency checks and to keep the entire system under control .

Actually this data allow the determination of all trigger efficiencies with the required precision togeteher with a detailed investigation of possible systematic effects due trigger system.

The modules of wich perform the trigger decisions for each subdetector contain counters, shift registers, status registers, and a fast data acquisition interface.

The trigger distribution system contains the logic for trigger handling and the logic for broadcasting the synchronization cycle, needed to check the properdistribution of the exact trigger number to all the front-end boards of KLOE.

All control and acquisition logic is implemented in FPGAs. In the design of the trigger modules HDL (Hardware Description Language) code for simulation was used, together with synthesis tools to target the function in FPGA devices. ECLinps logic and analog sum are used for fast part. The use of HDL permits the reuse of code for new design in different targets and an easy way to upgrade existing boards with new function, without PCB redesign.

The DAΦNE Φ Factory and the KLOE detector.

DAΦNE is high luminosity e+e-collider, built in Frascati, Italy. Its CM energy is set at the Φ meson resonance, 1020 MeV. About 35% of the Φ decays in $K_L K_S$ (K_L in $\pi\pi\pi$ and K_S in $\pi\pi$) while only a small fraction (about 0,3 %) are CP violating events (with K_L decaying in $\pi\pi$).

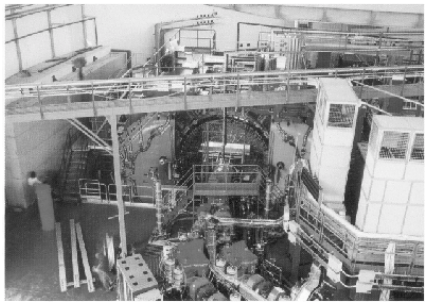

Fig 1. The KLOE detector inside DAΦNE.

The designed peak luminosity is 5 x 10^{32} cm^{-2} s^{-1} wich corresponds of Φ rate of about 2.5 kHz.
The Kloe experiment [1], currently on run at DAΦNE, has been optimized for the measurement of the CP violation parameter Re(ε'/ε) to a precision of 10^{-4} .
It consist of large helium tracking chamber for momentum measurement and a lead scintillating fiber elettromagnetic calorimeter with excellent timing performances. The entire detector operates inside 6 kGauss solenoidal field provided by superconducting magnet.

The KLOE Trigger.

The KLOE trigger [2],[3] strategy is based on local energy deposits in calorimeter sectors and multiplicity information from the drift chamber.

A two level scheme has been adopted in order to both produce an early trigger with good timing information to start the FEE operation and to exploid as much information as possible from the drift chamber, whose typical response time are in the microseconds scale.

Therefore after the arrival of a first level trigger, additional information is collected from the drift chamber, which is used, together with the calorimetric information, to start the DAQ system.

The trigger decsion can be vetoed at the first level in the case the event is identified as Bhabha scattering or at the second level in case of cosmic ray events.

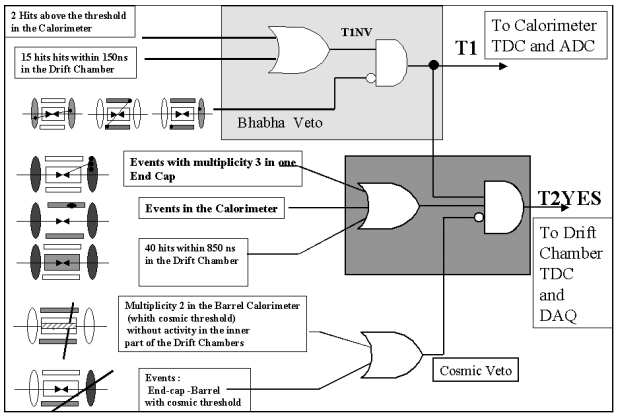

Fig 2. The KLOE trigger logic.

Trigger Control Signals.

In the following some definitions of the trigger signals and protocols are given:

- T0 is the time at which the real event occurs.
- T1 is the first level Trigger that has to be ready within 200 ns after T0. It is generated by the Trigger final decision board (TORTA), using the information coming from the Electro-Magnetic Calorimeter (E.M.C.), and from fastest hits in the Drift Chamber (D.C.) [2]
- T1sync is the T1 synchronized with the accelerator RF , and distributed by the Trigger Distributor board (TD) with a jitter less than 50 ps .
- T2Y is a signal, generated by the TORTA as a second level trigger, which takes into account the full information from the Drift Chamber and supplementary EMC information. It is ready and sent to the Trigger Supervisor (TS) in a range between 200-1500 ns after T1 **(**depending on wich subdetector is providing the validation**)**.
- T2 is generated by the TS with a constant delay of about 1.8 – 2 μs after T1 and distributed to the FEE if a T2Y from the TORTA was received. Its jitter needs to be less than 1ns.
- T1ACK is an acknowledge level which is asserted by the TS upon the receipt of a T1 signal from the TORTA. It is de-asserted at the end of a fixed time delay, independently on an eventual T2 generation, and if no BUSY condition is detected by the TS. T1ACK acts as a DISABLE signal to the TORTA. In case of a Golden Number Trigger, T1ACK remains asserted during the synchronization cycle.

The Trigger distributor.

Due to the very stringent timing requirements one of the most critical signals is T1sync, which is distributed to the ADCs and TDCs via the AUXbus backplane by using two differential lines [4].

Actually if a precision of 1ns is already an issue, 50 ps require a more sophisticated and cautious design of the line.

The Trigger Distributor (TD) distributes to the FEE the T1, directly received from the TORTA, after having synchronize it at 92,06 MHz, i.e 1/4 of the DAΦNE machine clock (368,25 MHz). The synchronized T1 is then fan-out, via a dedicated coaxial cable.

Laboratory mesasuraments give for tese module the following performances:

Max Temperature jitter <5 ps/°C
Max jitter for each channel ~7 ps
delay time for each channel ~ 14.2 ns

The Trigger Supervisor and FIOs crate.

The trigger supervisor (TS) [5] is a 9U VME board housed in a dedicated crate (Fig.3) with an custom backplane.

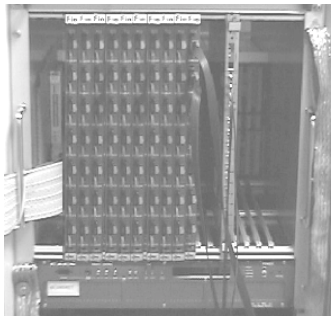

Fig 3. The Trigger supervisor and FIOs crate.

In the same VME crate are housed also 10 Fan In-Out (FIO) [5] modules, one for each readout chain , that distribute the trigger signals to the ROCK and the ROCKM boards, the controllers of the readout chain.

Every FIO module receives the T2 and the SYNCREQ signals from the TS via backplane, and redirects the BUSY and SYNCFAIL signals, coming from the ROCK (M)s to the TS, using dedicated backplane lines.

The TS main purpose is to provide an interface between the TORTA and the DAQ system. Its responsibility is to synchronize the distribution of the triggers with the event read-out and to block the validation of new triggers while the read-out system and the front-end electronics are busy.

During the synchronization cycle [4] the trigger supervisor and the FIOs check that in the entire system all the modules have the same trigger number. When a synch request is forwarded from the TS to the FIOs and from the FIOs to the respective chain, each ROCK module checks the trigger number inside the corrisponding crate, each FIO in the corresponding chain and finally the TS checks the status of all the FIOs.

The TORTA trigger box.

The Trigger ORganiser and Timing Analyser (TORTA) Board is the board that implements the trigger logic of trigger as shown in Fig2. As previously stated the T1 logic must be as fast as possible: therefore it is implemented on a ECLinps daughter card.

The use of a small daughter card gives a sufficient flexibility if a change of the T1 logic is needed. The rest of the logic is implemented in a 9U VME Auxbus board.

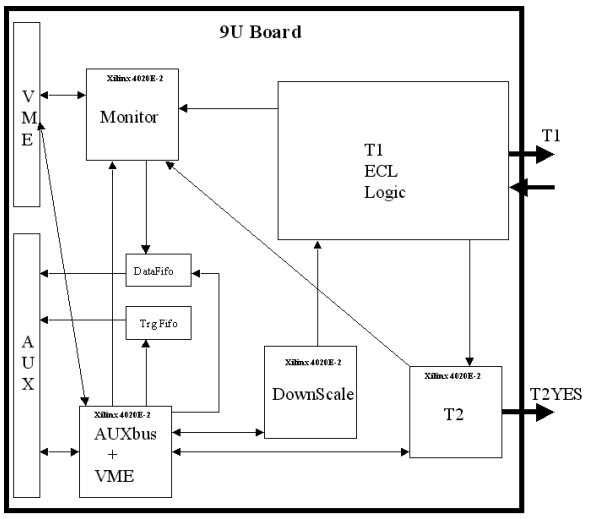

Fig 4. The TORTA block diagram

Four complex (~2000 flip-flops) Xilinx 4020EX are used.

The T2 Xilinx implements the T2 logic by setting registers to define the T2 configuration. The Monitor Xilinx implements a series of monitor registers to control dead time, arrival timing of critical signals and to latch the input patterns. The downscale Xilinx contains a set of counters to perform the downscaling of particular signals as the cosmic veto or bhabha vetos.

Finally the DAQ interface is implemented in the AuxBus VME Xilinx.

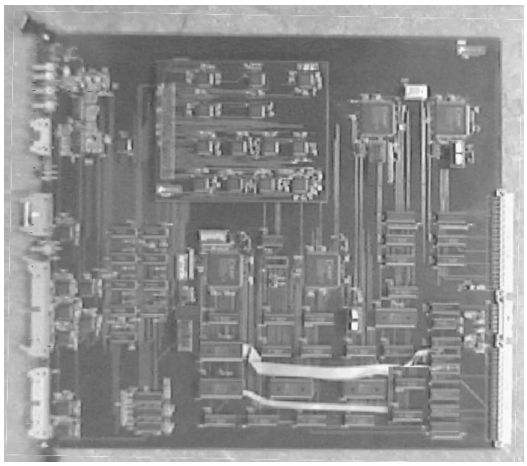

Fig 5. The TORTA Board.

The CAFFE Chamber trigger Box.

In the Chamber Activity Fast FEtch (CAFFE) board the first and second level drift chamber triggers are produced.

For trigger purposes signals coming form adiacent layers are grouped togheter, defining ten concentric “superlayer”.

This allows to avoid multiple counting spiralizing tracks of low energy particles produced in background events.

In the CAFFE the ten signals corresponding to the hit multiplicity of these superlayer are added.

The analog sum of layers 2-9 provides, after a discrimination to a proper threshold, the chamber level one trigger T1D.

The inner layer is used to produce the TCR signal used in the definition of the cosmic rays veto.

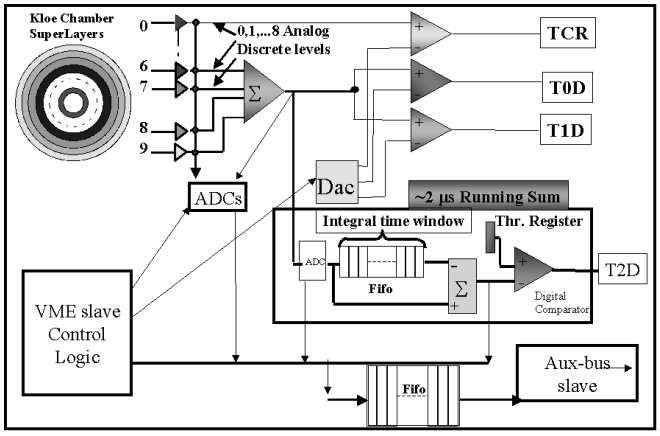

Fig 6. The CAFFE block diagram.

Moreover the analog sum of the 2-9 layers is digitally integrated with a running sum circuit implemented inside an FPGA.

After the receipt of the first level trigger, the number of hits in the chosen time interval is obtained by subtracting the values of two appropriate words in the register, corresponding to the integrated multiplicity just before the first level trigger and after 2 μs.

All the signals produced by the CAFFE are also digitized and are available for monitor purposes via either VME interface or during the KLOE acquisition via the Auxbus interface.
VME is used for setting of the the thresholds and for the definition of the integration time of the integrator.

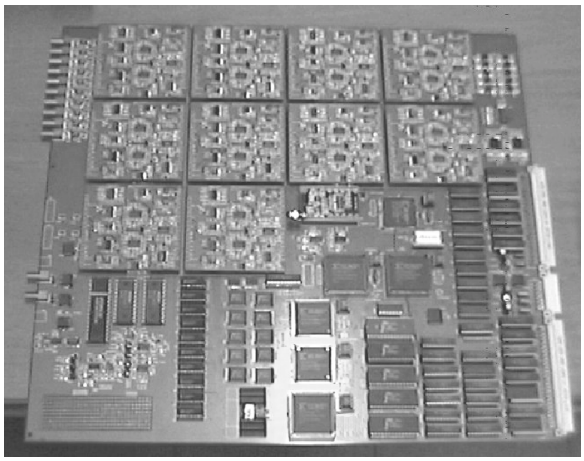

Fig 7. The CAFFE Board.

Conclusions

In the realization of these modules we started from the beginning using HDL (Hardware Description Language) and synthesis tools. In the meantime we observed from the very beginning the evolution of these tools from a source of new bugs to a mature tecnology. The use of FPGAs give to us enough flexibility giving an easy way to upgrade existing boards with new features when necessary.

All the described modules are steadly running since more two years.

Acknowledgements.

We are grateful to the INFN Bari CAE LAB in the person of Raffaele Liuzzi for the realization of the masters of supervisor TORTA and CAFFE and the CAE LAB of INFN LNF in the person of Domenico Riondino for the realization of the master of TD.

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