

Jet Determination in Lar- Calorimeters using a Heavily Interconnected System of FPGA's

B. Dulny, J.Fent, W. Haberer, C. Kiesling A. Osthoff

Max Planck Institut für Physik
Werner Heisenberg Institut
München, Germany

Abstract.

New fast and highly complex 'Field Programmable Gate Arrays' allow the design of sophisticated decision logic within the trigger latency time of detectors.

As an example we show the Jet Determination of the Hera-H1 detector at DESY Hamburg. It has to calculate all existing localized energy depositions (jets) in the calorimeter and deliver the result, sorted according to energy.

The system is implemented by a network of three times 440 high density FPGA's which have to deliver the results in less than 1 μ s. The computing power of the system is equivalent to 70 Billion operations per second.

1. The calorimeter trigger.

To understand the new system, it is necessary to give an survey of the environment in which it will be integrated.

The basic elements of the calorimeter trigger are built by about 700 projective, i.e. to the interaction region pointing, triggertowers.

These towers are the result of 40000 electromagnetic and hadronic channels which are readout and stored after the trigger decision.

The triggertowers are further summed to 512 so called Bigtowers (BT).

The electromagnetic and hadronic components of the BT-signals are digitized by 10 MHz Flash-ADC's and are summed to different topological and global quantities.

The electromagnetic and hadronic fractions are individually weighted in lookup tables. Further lookup tables and summing stages calculate different quantities as there are: total energy, transverse energy, missing energy etc.

The energy sums are discriminated by programmable thresholds, and the outputs are fed to the central trigger logic, where the decision for storing all the experiment data has to be made.

All this complex signal processing has to be accomplished in less than 1 μ s.

2. The FPGA - Jet-Trigger.

In the new proposed system, the summing over large calorimeter areas will be replaced by an intelligent algorithm identifying regions with signals well above the noise (jets).

The complicated scheme based on many thresholds at different levels can thus be replaced by an intuitive system where ideas popping up in a physics analysis can be easily implemented in the hardware.

All topological information will be available such, that physical correlations can be exploited to keep the trigger rate under control.

3. Design Principles.

The physical idea of the jet trigger is quite simple to formulate: It should find localized regions of energy depositions corresponding to a typical radius, together with the coordinates of the jet center.

In a trigger application a sequential algorithm is prohibitive because of timing limitations. A parallel hardwired solution is needed. The system is logically divided into four stages:

3.1 Preprocessor

Here, the analog pulses from the individual trigger towers, separated in electromagnetic (em) and hadronic (had) sections are sampled and digitized. The em and had sections are passed through look-up tables for thresholding and weighting and are subsequently added. The resulting 440 weighted towers are fed into the so-called bumpfinder.

3.2 Bumpfinder

The basic algorithm to find the jets is realized here. Each of the towers, formed in the previous stage, interrogates its nearest neighbors (known a priori by the fixed geometry of the towers) to determine whether any of them has more energy than the interrogating tower (called IT). If this is not the case the IT is a local energy maximum or „bump“. The jet energy is then formed by adding all the energies of the neighboring towers to the energy of the bump. Since this algorithm only interrogates the immediate neighborhood, it is suited for parallel execution: All the trigger towers determine their bump property independent of the others. The result of the bumpfinder is a list of jets, defined by energy and coordinates. A finite number of jets (maximum of 24) is fed into the next stage, the energy sorter.

3.3 Energy Sorter

Here a fixed number of jets (24) are sorted according to energy. Again the algorithm is carried out in a parallel manner, similar to the bump identification algorithm: Each jet compares itself with all the others and determines the number of jets with smaller or equal energy. The jet with the number 23 is the largest, the one with number 22 the next etc. In case of equality in the energies, a unique ordering based on the topological location of the bumps is forced. From the 24 possible bumps only the first 12 (highest energy) bumps are passed to the next stage.

3.4 Trigger Quantity Determination

The trigger element generator (TQD) houses the necessary logic to construct the trigger decision from the jets found. Typical actions of the TQD is to discriminate the individual jet energies, count jets above certain thresholds and determine topological correlations on the basis of position information of the jets. The TQD is designed in a very flexible and expandable way, since the optimal strategies of triggering will largely depend on the changing physics interests.

4. Hardware Realization.

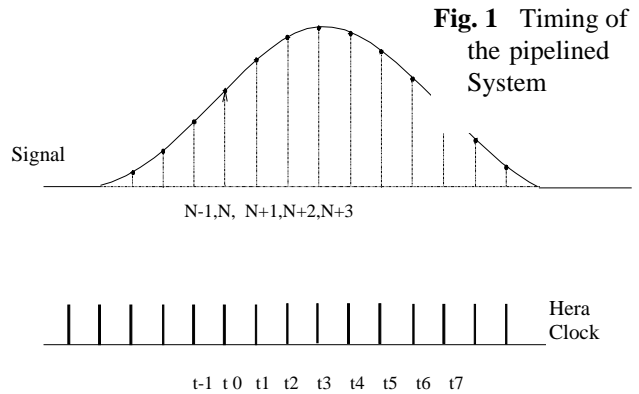
4.1 Design overview

The trigger towers have to be re-assembled to optimize their granularities depending on the position in the calorimeter. The re-assembly of the

signals is done in the ACS system (ADC, Calculation, Summing).

The Bump Finder Unit (BFU) processes these signals to find „bumps“ and their addresses. „Bumps“ are defined as the maxima of local energy depositions, including their immediate next neighbors. The BFU consists of eight boards, mapping eight octants of the calorimeter, arranged in cylindrical form. Each board delivers the fifteen possible „bumps“ to its Primary Sorting Unit (PSU). This unit selects, for each octant, the three bumps with the highest energies and transfers them to the central Secondary Sorting Unit

(SSU). Here the total of $3 * 8$ bumps are sorted by energy in decreasing order. The 12 largest bumps are sent to the Trigger Quantity Determination box (TQD), where the trigger elements will be generated.



- t0 sampling of signal, start of conversion for sample t0
- t1 digital output for sample t0 (5 internal clock cycles)
- t2,t3 processing of sample t0, transfer to BFU
- t4 output of Bump Finder Processor (BFU)
- t5 output of Primary Sorting Unit (3 Maxima/sector)
- t6 output of secondary Sorting Unit (12 Maxima in decreasing order at Trigger Quantity Distributor TQD)

Fig. 1 shows the timing of the pipelined system, in time units of particle crossings of the accelerator. Note that one unit is $0.1 \mu s$ and that only a total of 8 units are available for the digital part of the jet algorithm.

If one considers the sample N at unit 0, the digital value is obtained at unit 1. The ACS unit can complete its processing within one unit. With cable delay the BFU receives the data at unit 3. At unit 4 the output of the BFU is available and PSU and SSU finish their work until unit 6. In the remaining two units the final trigger elements are generated.

4.2 ADC-Calculation-Storage Unit (ACS)

The ACS cards convert the signals from the 568 EM-Trigger Towers and the 624 Had-Trigger Towers in 1192 8 Bit words, weight them,

calculate the EM- and Had-sum, send the resulting 440 Bytes to the BFU (Bump Finder Unit) and store simultaneously the data in circular buffers.

Except the AD- conversion, the logic is implemented in 440 FPGA's. (Altera 10K30).

4.3 Bump Finder Unit (BFU)

The current energy content in each input tower is compared with the eight or nine (depending on the local granularity) nearest neighbors (see fig2).

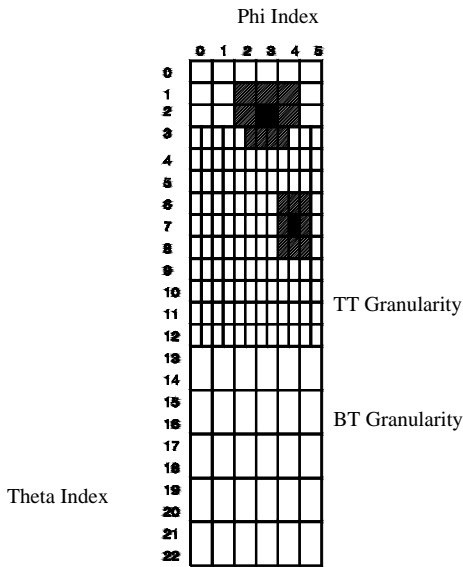


Fig. 2
Local granularity

This operation is done for all input towers in parallel. The towers which win, i.e. have the highest energy value compared to the neighbors, are bump centers. They sum the neighbor energies to their own energy and put the result onto the Three - State output bus, together with the address of the bump center.

The Input Towers are grouped to tower clusters. Only one member in a group can be a „bump“. Fig.3 shows one of the eight boards with Input Towers, Tower Clusters and the bus connections of a single Input Tower. Note that there are eight 8 Bit input busses from the neighbor towers, output address bus, 8 Bit output bus for the summed energy and a fanout of eight 8 Bit busses to the neighbor towers.

The bump energy (8 Bits) and the address within a cluster (2 Bits) are transferred to the PSU (Primary Sorting Unit). The evaluation of bump centers and the formation of the bump energies

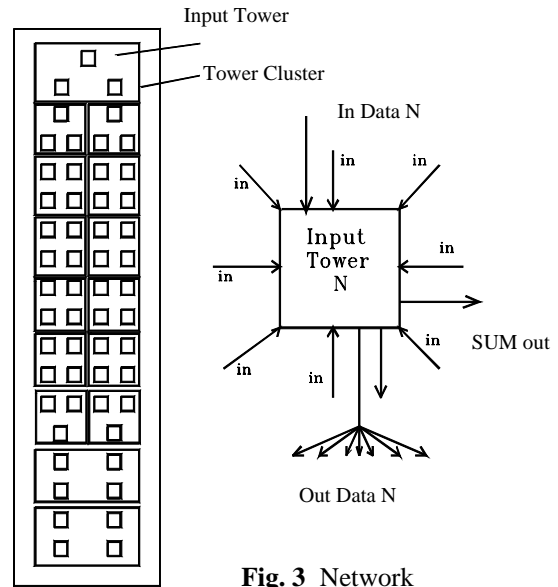


Fig. 3 Network of a single input tower

is done in large FPGA's (one for each Input Tower, 440 all together), which are all networked together. The total computing power of the BFU sums up to about 70 Billion calculations per second. Because of the high complexity of networking, it is necessary to arrange the system in form of a cylinder, just like the calorimeter itself. .

4.4 Primary Sorting Unit (PSU)

One of the eight identical sections in the cylinder contains 55 FPGA's with the BFU function. The fifteen bump energies (8 bits wide) and two address bits for every group are prepared for the Primary Sorting Unit (PSU). In the PSU the energies of each of the 15 bumps are compared with all others. The result is a coded position in the hierarchy of energies. After decoding, the three biggest bumps and their addresses are stored.. They are sent to the Secondary Sorting Unit (SSU) for the next sorting step. The PSU needs one time unit (0.1 μs) to process its function and is implemented in one large FPGA for each section.

4.5 Secondary Sorting Unit (SSU)

The 24 biggest bumps together with their addresses (3 maxima from each section), are collected in the PSU's for the whole calorimeter and are transferred to the SSU for the final sorting operation.

In the SSU the energies of each of the 24 bumps are compared with all others. If two bumps are

equal, the global position in the calorimeter is taken into account to force a strict ordering. Therefore the result of each comparison is an unambiguously coded number which gives the position in the hierarchy of energies. After decoding, the 24 energy bumps and their addresses are stored in decreasing order. The 12 largest energy bumps are distributed to a general bus system („jet container“), where trigger quantities can be calculated in the remaining time units. The Secondary Sorting Unit will be implemented in few large FPGA's (250 k gate equivalents) .

4.6 Trigger Quantity Determination (TQD).

The output of the third stage of the jet trigger is the list of 12 largest jets found, ordered by energy. In the forth and last stage of the trigger , this list is used to generate the trigger elements leading to an actual trigger. Since the „jet container“ is a bus system, an arbitrary number of modules may have access to it and trigger elements can be easily added if needed without disturbing the determination of the already implemented trigger elements in the jet trigger. The amount of complexity of trigger elements is limited by the two time units ($.2\mu$) which are left for the TQD.

5. Status of the Project

The project was started in the second half of 1997. The simulations for the different components (ADC Unit, Bump Finder and Primary and Secondary Sorting units) showed that the processing time can be kept in the available time units.

The logic synthesis of all FPGA's was successful. A first demonstrator model of the Bumpfinder for one octant showed its functionality.

6. Conclusions

The proposed level 1 jet trigger is the last missing piece of an ambitious upgrade program for the HERA H1 Liquid Argon Calorimeter. The physics idea of the trigger is to find the localized energy depositions in the calorimeter, order them by their energies and provide decisions in a very flexible way based on the multiplicity, energy and topological information of the jets.

The trigger will overcome the limitations of the present global trigger philosophy and will allow to select specific physics reactions with higher efficiency and higher background rejection.

The realization of this ambitious project is possible due to the fact that very complex and fast FPGA's came to the market and the second important fact is the availability of reliable design systems .

