A Low-Power, Radiation-Hard Gigabit Serializer for use in the CMS Electromagnetic Calorimeter

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***Abstract*—An integrated fiber-optic bit serializer and VCSEL (Vertical Cavity Surface Emitting Laser) driver has been constructed in radiation-hard complementary heterostructure GaAs FET (CHFET) technology. The serializer, which converts 20 parallel inputs into a high-speed serial output, consumes 60 mW at nominal supply voltage when operating at the Large Hadron Collider (LHC) word rate of 40 MHz (0.8-GB/s serial rate). The integrated driver directly drives a VCSEL and provides 10-mA switched current and 5 mA of prebias. The complete digital optical link thus consumes 90 mW.**

***Index Terms*—Optical communication, radiation effects.**

I. Introduction

MODERN high-luminosity particle physics experiments require a diverse and large number of electronic components operating in a harsh background radiation environment. In experiments at the Large Hadron Collider (LHC) being built at CERN in Geneva, maximum radiation levels will exceed 10^5 Gy (10 MRad) along with up to 10^{15} neutrons/cm^2 over the ten-year life of the experiments. These levels depend strongly on position and drop about four orders of magnitude at the outer radius of the particle detectors.

For several applications in such detectors, and in particular in the calorimeters, low-power gigabit/s digital fiber-optic links present attractive methods to transport the sensor data out of the high-radiation detector environment, to a shielded area for digital processing. In the Compact Muon Solenoid (CMS) experiment, the electromagnetic calorimeter (ECAL) [1] will consist of around 80 000 lead tungstate ($PbWO_4$) crystals arranged in a barrel and two endcaps. The scintillation light from the crystals is captured by a photodetector, amplified, and digitized. The digitizing electronics are located on the detector and must survive a total absorbed dose of up to 2×10^4 Gy along with a fluence of 5×10^{13} n/cm^2 over the lifetime of the detector.

Following the digitizing electronics, digital signal processing circuitry pipelines the data and performs a variety of numerical calculations for use in the experiment trigger. In order to avoid placing this large quantity of digital electronics in the detector radiation environment, fiber-optic links, one per crystal, will be used to transport the digitized data off the detector into a shielded environment. Such links must thus not only be sufficiently radiation hard, but also be low power as a large number of them are placed in an enclosed thermally regulated detector environment.

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II. Use of CHFET Technology

Faced with applications that require resistance to high levels of radiation (or no parameter drift at lower levels of radiation) typical solutions are SoI (silicon-on-insulator) CMOS or BiCMOS and bonded-wafer full complementary bipolar processes. SoI CMOS is a clear choice for low-power high-integration digital applications and less demanding analog ones. SoI BiCMOS can serve for higher speed at higher power, or improved analog applications. High-performance high-speed analog applications benefit from full complementary bipolar processes, at the expense of higher power consumption.

Complementary gallium arsenide (GaAs) is gaining increasing acceptance as a technology capable of achieving high speed and low power in harsh temperature and radiation environments. Such technology is thus ideally suited to high-speed digital fiber-optic data communications. With the realization of complementary heterostructure GaAs FET (CHFET) in 1985 by Honeywell, it became possible to produce circuits that combined the advantages of "CMOS-like" logic (low power and high complexity) with the advantages of GaAs (high speed, radiation hardness).

With the continuous decrease in feature size, digital circuits have become faster and capable of lower power operation. For CMOS logic, with negligible standby power, power consumption is given by $P = CV^2 f$, where C is the logic gate (and line) capacitance, V is the supply voltage, and f is the frequency of operation. Smaller feature sizes generally mean lower values of C and lower values of V. CHFET, which has low C, and operates at 1.3 V, thus has a clear power advantage over silicon.

CHFET transistors are well described by the five-parameter Statz model [2] for $V_{DS} \geq 2$ V. Logic circuits operate at 1.3 V, and typical threshold voltages are 0.2–0.3 V (both N- and P-CHFET's are enhancement-mode devices). Transistors used in logic cells have typical values of C_{GS} 5–20 fF. Although scaling is not quite linear with L, the transconductance, k', is around 200 μA/V^2 for NFET's and an order of magnitude lower for PFET's. In this paper, β refers to the transconductance parameter for a given transistor, and k' represents the simulation model parameter ($\beta = k'$ W/L).

Since radiation hardness is crucial, considerable effort has been invested in finding testing techniques that enable us to understand and model effects due to radiation. Components for use in the CMS ECAL are regularly tested in the OPTIS proton

beam at the Paul Scherrer Institute (Villigen, Switzerland). The OPTIS beam consists of 72-MeV protons with a flux of 1.25 $\times 10^9$ p/cm^2/s. These protons are roughly five times minimum ionizing and cause the equivalent displacement damage as two 1-MeV neutrons. This mixture thus simulates the radiation environment in the CMS ECAL where the electronics will be placed. CHFET (and other) components are generally irradiated to 10^{13} p/cm^2, which is equivalent to roughly 104 Gy and 2×10^{13} n/cm^2. Other authors [3] have performed ^{60}Co tests on CHFET to doses two orders of magnitude higher.

The variation of transistor parameters V_T and β as a function of proton dose for test transistors [$W = 60\ \mu \times L = 1.0\ \mu$] is shown in Fig. 1. As is seen, there is essentially no change in behavior with irradiation (here, up to 1.5×10^{13} p/cm^2). During the irradiation, V_{DS} and V_{GS} were continually varied, so that the transistors were not in a static bias configuration. The measured value of I_D as a function of V_{DS} and V_{GS} were used to extract Statz model parameters as a function of dose.

III. Circuit Architecture

Low-power operation is important in this application, as almost 100 000 transmitters will be located in the enclosed detector volume. The circuit architecture has been adapted for low-power operation and makes use of complementary logic for all operations except the high-speed serialization, where only NFET's are used.

In a conventional serializer, registered parallel N-bit input words are converted into a serial stream by a multiplexed-input shift register running at N times the word rate. Such a design requires high-speed flip-flops for the shift register and generally use a PLL-based clock synthesizer to generate the shift clock from the word clock. In the CHFET implementation, delayed copies of the word clock are produced with a DLL. These delayed copies are then used with combinatorial logic to create a serial data stream. Use of a DLL rather than a PLL is discussed in [4], and for this application the principle advantages are lower power and simpler loop design.

The basic delay structure employed is shown in Fig. 2, and consists of a chain of cross-coupled inverters operating at a fixed voltage V_{DLY}. Here, the PFET's are $W = 20\ \mu/L = 0.7\ \mu$ and the NFET's are $W = 10\ \mu/L = 0.6\ \mu$. The complete 20-b DLL was designed to operate at $f = 40$ MHz for $V_{DLY} = 1.3$ V and has an average measured sensitivity of $df/dV_{DLY} = 10$ MHz/150 mV.

Cross-coupled flip-flops, as shown in Fig. 3, are used to generate the DLL control voltage V_{DLY}. The clock as it exits the DLL chain ($\boldsymbol{V}$) is compared to the clock as it enters ($\boldsymbol{R}$), generating positive or negative current increments, which are stored on an integrating capacitor. The value of the capacitor then fixes the "jitter" per frame at

$$\sigma = \frac{d(1f)}{dV}\frac{I_{\mathrm{BIAS}}}{fC}$$

where f is the word rate and I_{BIAS} is the current switched in Fig. 3.

To convert the N-bit parallel input word into a serial stream using combinatorial logic, the individual data bits are successively enabled by the delayed copies of the clock (an example of the this technique may be found in [5]). Conceptually, if D_i is the ith data bit (where D_1 is the LSB and D_N is the MSB) and CK_i is the ith delayed copy of the clock, the serializer output, Z, is obtained by

$$Z = \sum_{i=1}^{N} Q_i,\ Q_i = D_i \cdot CK_i \cdot \overline{CK_{i+1}}.$$

In reality, such logic is prone to glitches at each bit transition, hence, the logic shown in Fig. 4 is used.

As shown in Fig. 4, a look-ahead technique is used to determine whether or not to switch off the VCSEL for the next bit. When $Q_i = D_i \cdot CK_i \cdot \overline{CK_{i+1}}$ and both $D_i = D_{i+1} = 1$, then a small glitch can appear between bits i and $i+1$ during the

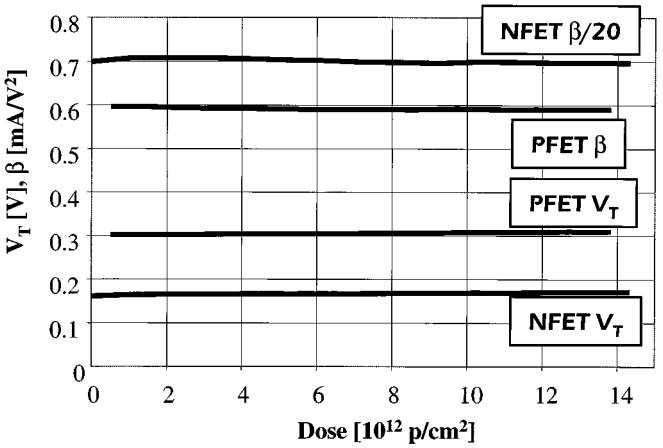

Fig. 1. CHFET parameters during irradiation.

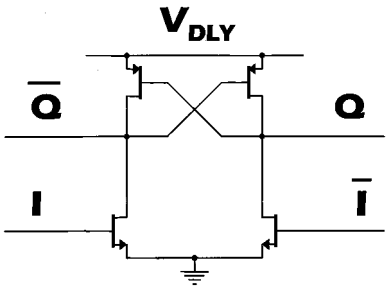

Fig. 2. Basic delay structure.

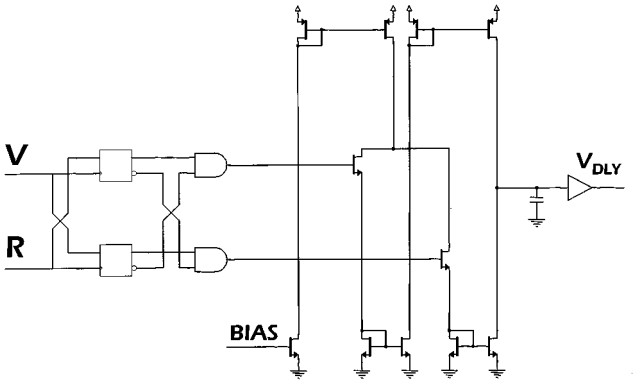

Fig. 3. DLL control.

transitions of $CK_i \cdot \overline{CK_{i+1}}$ and $CK_{i+1} \cdot \overline{CK_{i+2}}$. To prevent this

$$Q_i = D_i \cdot CK_i \cdot \left(\overline{CK_{i+1}} + D_{i+1} \cdot \overline{CK_{i+2}}\right).$$

The actual implementation of the logic described for Q_i makes use of feedback FET logic (FFL) [6]. An FFL inverter is shown in Fig. 5. As FFL makes use only of NFET's, it is inherently fast, but unlike the complementary logic, it has a static power consumption of up to 650 μW/cell. In the serializer, a single FFL cell (a multiplexed NOR, controlled by D_{i+1}) produces Q_i. Four-fold intermediate NOR's of the Q_i are formed, and the final output Z is the five-fold NOR of the intermediate terms.

In order to minimize power consumption, the VCSEL cathode is driven with a current output. An output stage is constructed with FFL inverters whose input is Z and whose output is connected to the gate of an NFET. This NFET has a grounded source, and its drain is connected to the VCSEL cathode, the anode being held at ± 2 V. Notice in Fig. 5 that M1–3 along with R form a current source, so that Z effectively switches those constant current sources through the VCSEL. An independent current mirror provides the prebias current of the VCSEL.

IV. Results

The circuit described above was submitted in November 1997, and the wafers were processed at Honeywell's CHFET facility in Plymouth, MN. The fabrication process has been described elsewhere [6]. A test chip consisting of individual transistors and test structures was submitted along with the serializer in order to be able to extract transistor parameters. The serializer, shown in Fig. 6, measures roughly 1.5 × 4 mm^2. The integrated VCSEL driver is on the right of the chip, and the DLL control and other analog circuits are on the left. The high-speed FFL core is contained in a strip in the center of the chip, surrounded on the top and bottom by cells containing the input flip-flops, delay elements, and additional logic.

During testing, the serializer drove an HFE-4080 VCSEL from Honeywell Microswitch connected to 30 m of 62.5/125-μ fiber. The signals were received by a Finisar 8510, whose output was connected to a digital oscilloscope. Transition waveforms at 800 Mb/s are shown in Fig. 7. The points represent the density plot from the oscilloscope, and the solid lines are overlaid simulation values.

The simulation values were obtained by using model information derived from measurements of the test chip described above. The test chip contained N and P transistors and a ring oscillator. Transistor parameters were extracted from several test chips, and the data were fit to a modified form of the Statz model (the parameter b was forced to zero, so the transistor is described by V_T, β, α, and λ). L–I–V data obtained with the HFE-4080 was used to create a simple model for simulation.

The circuit was tested under irradiation at the OPTIS proton beam at an ambient temperature of 25°C. Fig. 8 shows the evolution of the four components of the circuit's power consumption (operating at 40-MHz word rates) with proton dose. The line labeled 40-MHz logic represents the power consumption of the flip-flops and delay elements; analog (DLL) represents that of the input clock receiver and charge pump, NFET logic represents that of the FFL core, and VCSEL represents the total power consumption of the VCSEL with the driver. As seen, the power consumption remained stable, at less than 100 mW for the link. Individual bias currents and dc operating points were also monitored during irradiation and showed no change.

During irradiation, the only observed variable that showed any change was the DLL control voltage, VDLY, which showed a slight increase with dose, as shown in Fig. 9. This effect does not alter the operation of the serializer; it was simply the only observed effect caused by radiation.

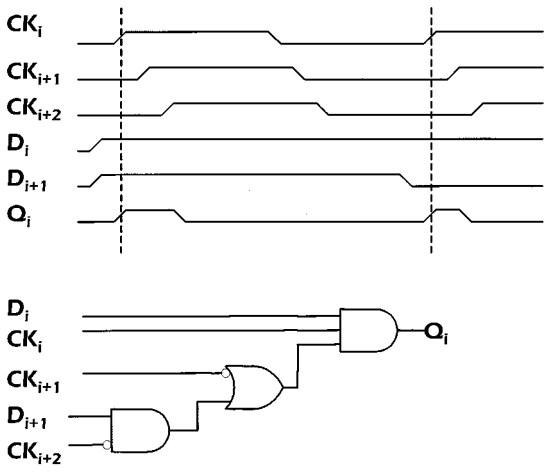

Fig. 4. Combinatorial logic.

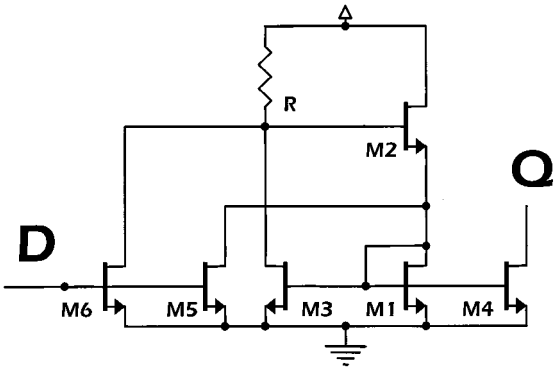

Fig. 5. FFL inverter.

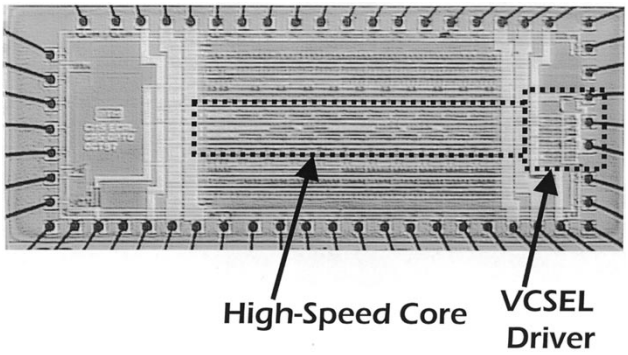

Fig. 6. Serializer photograph.

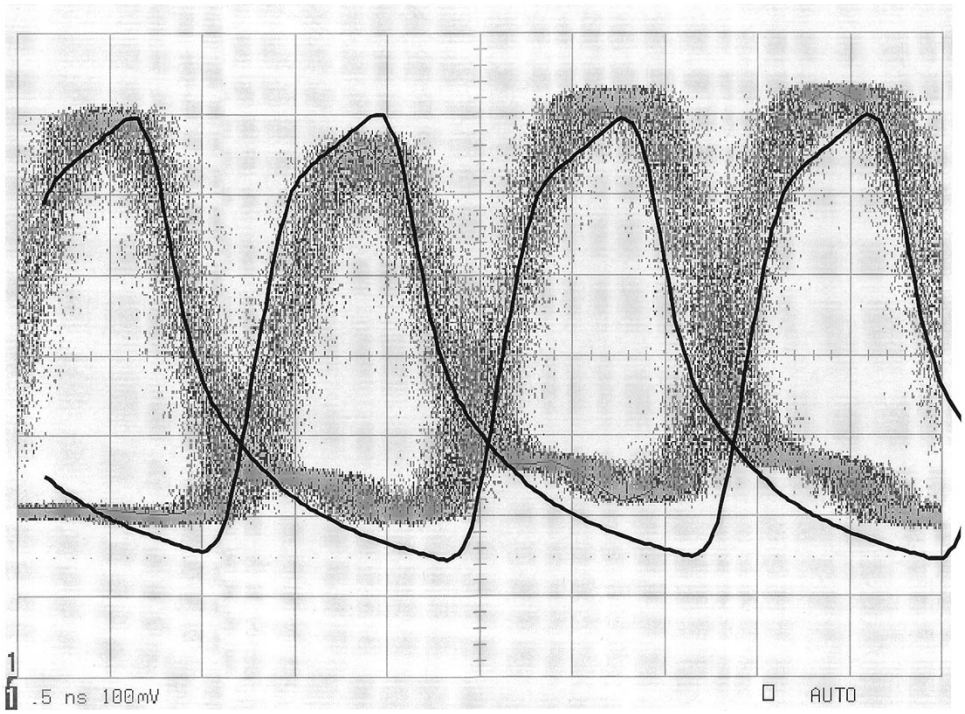

Fig. 7. Optically received transitions (measured and simulated).

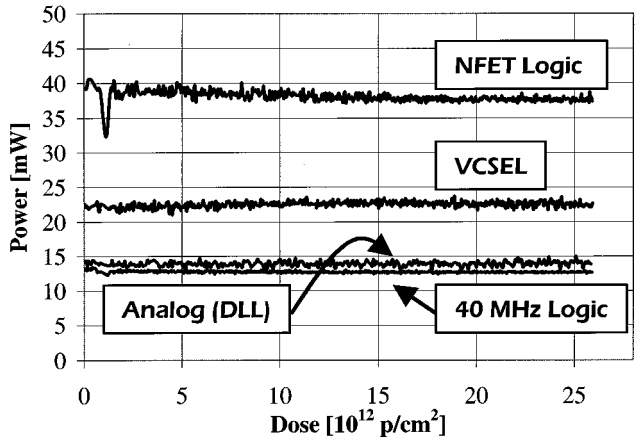

Fig. 8. Serializer power consumption with irradiation.

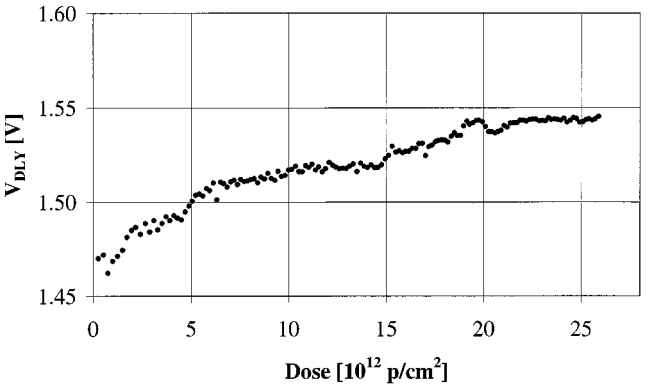

Fig. 9. Change in serializer DLL control voltage with irradiation.

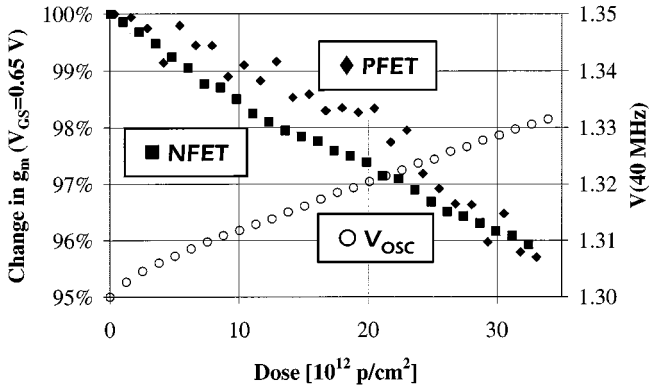

Fig. 10. Change in CHFET g_m and ring oscillator VDD with irradiation.

Individual transistors, from the same run as the serializer, were also irradiated, and showed minor effects in both N- and P-channel devices: Threshold voltages increased roughly 10 mV per 10^{13} p/cm^2 (under radiation, both N- and P-channel thresholds increase) and β dropped roughly 1% per 10^{13} p/cm^2. These two effects combine to give an effective g_m loss of around 1% per 10^{13} p/cm^2.

Fig. 10 shows the variation in g_m with dose, caused by the small V_T and β shift under irradiation. A ring oscillator was fabricated on the same test chip as the individual transistors, and also shown in Fig. 10, is the voltage ($V_{\rm OSC}$) required to keep the ring oscillator at a constant frequency as a function of dose. The ring oscillator structure is not identical to that of the DLL, however, it would appear that the small change in g_m explains the change in V_{DLY} observed in the DLL.

V. Conclusions and Future Plans

A high-speed serializer with integrated VCSEL driver has been fabricated in CHFET technology. The serializer, driver,

and VCSEL consume 90 mW when operating at 0.8 GB's, and demonstrate no degradation in performance at doses up to 2.5×10^{13} p/cm^2 (which is equivalent to 2.5×10^4 Gy along with 5×10^{13} 1-MeV n/cm^2). This meets the requirements of the CMS ECAL for speed, power consumption, and radiation hardness.

Single-event effects are a potential concern for this circuit either as random bit errors or losses of synchronization. As the high-speed clock is based on a DLL rather than a PLL, the circuit stores no information longer than one clock cycle. The large loop capacitor (shown in Fig. 3) is sized such that an erroneous decision by the control logic changes the reconstructed word clock timing by less than 10^{-3}. Radiation tests with the OPTIS proton beam, to look for single-event effects, have started, and their results will be reported in a subsequent paper.

An improved version of the serializer, including dc-line balance protocol, is in fabrication. Based on the good agreement between measurement and simulation (as shown in Fig. 7) care has been taken to improve the symmetry in the VCSEL light output. Two principle refinements were made. First, additional transistors were added to the basic DLL cell in order to compensate the difference in rise and fall times due to the difference in β_N and β_P. Second, a capacitive feedforward stage was added to the VCSEL driver to compensate the difference in turn-on and turn-off times in the VCSEL. The improved serializer, which along with an external VCSEL forms the transmitter of a digital optical link, will also consume less than 100 mW. The serializer, in addition to radiation hardness, thus also has a power consumption lower than corresponding commercially available parts.

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