THE ATLAS TILE CALORIMETER DIGITIZER

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Abstract

We describe a digitization and readout system built to serve 10800 PMT channels in the Atlas Tile calorimeter. Six or eight digitizer boards in each calorimeter module each receive six pairs of analog signals (high and low gain) to be digitized by 10-bit ADCs every 25 ns. Two custom designed gate arrays (CX-3161 from Chip Express) on each board each store data from three channels until validated by the first level trigger. Selected data are then formatted for subsequent read out. Clocks and control commands are distributed via the TTC system. The system is designed to achieve good fault and radiation tolerance. It was tested in test beam during summer 1999, and is intended for volume production in 2000.

1.1 INTRODUCTION

The Tile calorimeter (TileCal) [1] is divided into two barrel and two extended barrel parts. Each part is divided into 64 wedge-shaped modules (i.e. 256 modules in all). Each barrel module is read out by 45 PMTs, and each extended barrel module contains 31 PMTs.

The PMTs and the front end electronics are located inside "drawers" in the base of each module. Attached to each PMT base is a 3-in-1 board [2] which amplifies and shapes the PMT output. The shaper outputs are connected to the TileCal Digitizer system.

The digitizer system fits within a space 2.8 meters long and 10 cm wide, with sufficient clearance for two layers of circuit boards. Up to eight digitizer boards, each serving 6 channels, will fit into each module, along with a central readout interface. The drawers provide a well-shielded, water-cooled environment kept at a temperature of about 25 degrees centigrade. A power dissipation of about 70 Watts per module is allowed for the digitizer system.

The digitizer system samples incoming data every 25 ns. using 10-bit ADCs [3], and stores them in a fixed-length pipeline to await a first level accept. The level-1 latency is stipulated to be no longer than 2.5 μs. Each triggered event is recorded over an extended time frame, with a length programmable up to 16 samples. The time frames are stored in readout buffers (derandomizers) awaiting readout via the readout link interface.

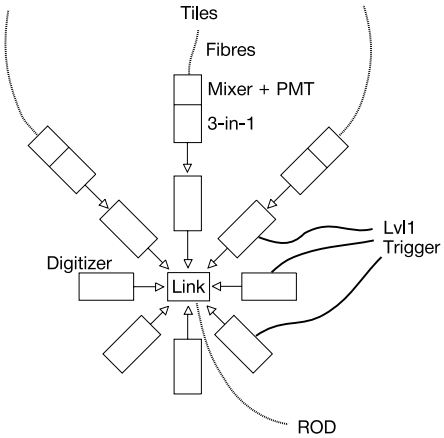

Fig. 1: Data flow of Tile Cal. electronics

The digitizer samples high and low gain signals in each channel, with a gain ratio of 64. A selection mechanism determines which gain to use for a specific pulse, reading out only the high gain data unless it overflows or underflows, in which case the low gain data are used.

Since the digitizer system is situated inside the calorimeter with a non-negligible radiation level and limited access for maintenance, it is important to make the design extremely reliable and sufficiently radiation tolerant**.** For these reasons the digitizer system has been implemented to reduce the impact of single point errors. This is done by decoupling the different parts of the readout chain (Fig 1), so that a fatal error in one component causes limited disruption. In the final design all components in the system will be at least radiation tolerant.

Two prototype digitizer systems have been tested at CERN during summer 1998 [4] and summer 1999. The design was subjected to a production readiness review (PRR) in June 1999, where it was provisionally accepted. However it must be subjected to a final review when the pre-production version is available.

2. SYSTEM ARCHITECTURE

2.1 General

The TileCal Digitizer consists of two chains of digitizer boards connected to a readout interface in the center of the drawer (Fig.2).

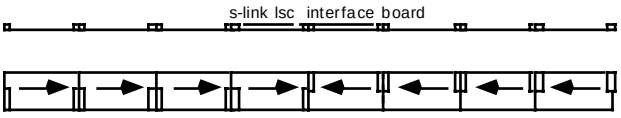

Fig. 2: Two chains of digitizer cards connected to the readout interface in the center of a module.

Each digitizer board samples and stores data from 6 channels. The digitizer boards contain 3 main types of components:

- 12 ADCs (two for each channel)
- 2 Tile-DMUs, which are custom devices containing pipeline memories for three channels, together with readout buffers and control functions.
- One TTCrx chip [5] responsible for system timing and programming.

The readout from each Tile-DMU is connected to the link interface card via point-to-point links (Fig 3). Differential LVDS is used to provide a safe transmission path with a minimum of digital noise fed back to the analog inputs. The signals pass through intermediate boards via pass-through links with no active components. This is done to insure that the consequences of a digitizer board malfunction will be limited to the possible corruption of its own data.

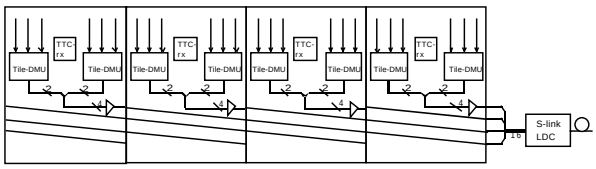

Fig. 3: The data flow along a chain of digitizer boards.

One consequence of this design are distance-dependent variations in the timing of data sent to the link. By adjusting the phase of the output data from the Tile-DMUs, however, this skew can be reduced to within 1 ns. This is performed by adjusting the timing of output data from each board.

The current readout interface consists of an interface card which buffers and transmits data to an S-link source card [6]. Connections between the digitizer boards and readout cards are made using surface mount connectors and printed circuit foils. The lines within the circuit boards and in the foils are given matching impedance to avoid reflections.

The placement of the readout board in the center of the module reduces the maximum readout path length. It also places the fiber-optic readout link in an environment with better radiation shielding than at the ends of the module.

2.2 The Digitizer Board

The digitizer board (Fig. 4) is divided lengthwise into analog and digital parts, each with separate power and ground planes. Low and high gain analog signals for each channel are received differentially from the 3-in-1 shapers via shielded twisted pair cables. The receiving network is fully passive and adapts the signal to the ADCs and also creates the pedestal level. Separate ADCs digitize the low and high gain signals for each channel.

The ADC used is the Analog Devices AD9050. It uses a successive approximation scheme with 5 cycles of latency. Pedestal levels are adjustable in groups of 3 channels via a DAC programmable via the TTC interface.

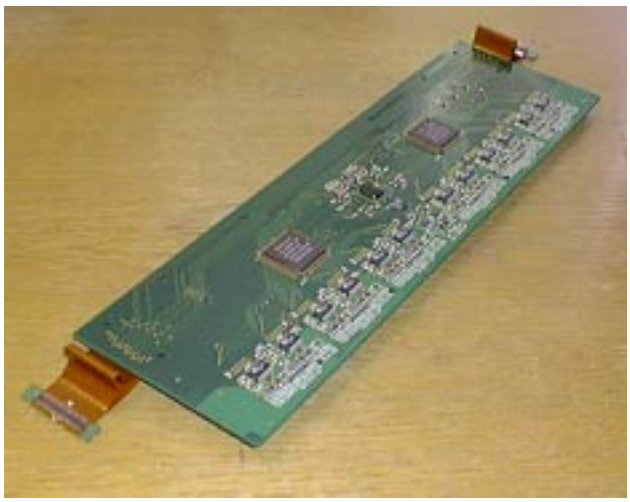

Fig. 4: The digitizer board.

A TTCrx chip on each board receives signals via a coaxial cable from the interface board, which converts and electrically fans out the signal from the TTC fiber.

2.3 The Tile-DMU

The Tile-DMU (Fig. 5) is implemented in a custom gate array. It receives ten-bit high gain and low gain inputs from three different channels. The data are stored in a pipeline memory, pending a Level-1 trigger decision. On an accept, a programmable number of consecutive samples are sent to derandomizer readout buffers implemented in a dual port RAM. The derandomizers use a scheme with memory pointers, where the start address for a stored event is stored in an address FIFO. Between 16 and 32 such derandomizer buffers are available, depending on the length of the time frame used. It is also possible using this memory-pointer scheme to read out events with overlapping time frames.

Four parity bits are added to the data before they enter the pipeline memory. Each parity bit covers overlapping regions of 20 bits.

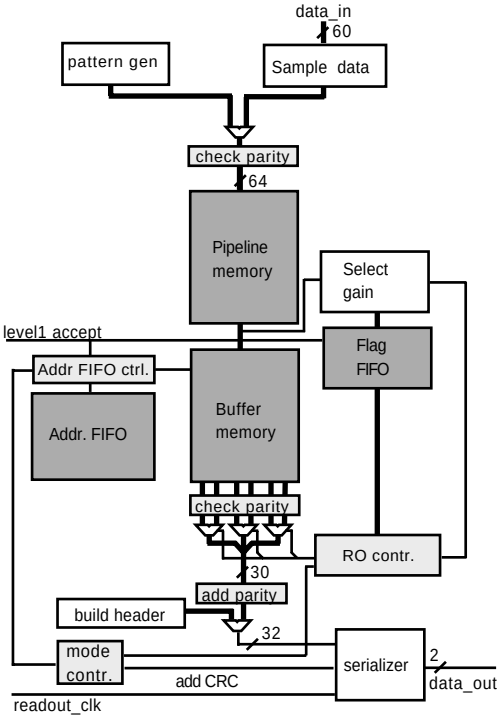

Fig 5: Block diagram of the Tile-DMU

High gain data from each of three channels are compared with programmable limits to determine whether an overflow or underflow condition occurred. A cumulative overflow flag for the full time frame is constructed for each channel. The overflow flags are stored in a flag FIFO.

When the FIFO is not empty, a flag signals the readout controller that there is data to be read out. An address from the address FIFO and corresponding overflow flags from the flag FIFO are retrieved and entered into a header word. The header is followed by data words from the buffer memories, with high or low gain values selected according to the value of the overflow flags.

After data have been retrieved from the buffer memory, they are serialized into a 2 bit output data stream at 40 MHz. A CRC-16 checksum is appended to allow the identification of transmission errors

The 2-bit data sequence from each Tile-DMU is appended with "11" at the start and "00" at the ends with. A sequence of registers, the last of which is latched via a deskewed clock from the TTCrx, is used to adjust the timing of the readout path.

The Tile-DMU has three selectable modes of operation. In addition to the "normal" data taking mode described above, a "calibration" mode reads out both high and low gain data for every channel. A third "test" mode uses a programmable seed to produce walking test patterns in the high and low gain channels for system verification.

The data rate from the Tile-DMU can be controlled by two different methods to adapt to different types of readout. One method is programming the readout controller inside the Tile-DMU to introduce a delay between each consecutive readout cycle. The second method is the use of direct flow control protocols between the readout interface and the Tile-DMU. For example, the Tile-DMU is capable of generating all necessary signals for the S-link readout protocol.

2.3 Readout protocol

The header word contains information about the gains and error bits.

The link control lines (link Reset, Ctrl, Test and Write_enable) are generated by all Tile-DMUs. This means that a drawer will have 16 versions of each signal, one for each Tile-DMU, although only one set is required. To improve fault tolerance, it is possible for the interface board to combine control signals from several digitizer boards, using majority vote to initiate changes.

2.4 System Control

The Tile Digitizer is programmed by commands sent via the B channel of the TTCrx system. The following items are programmable:

- Length of the pipeline
- Length of the time frame
- Phases of the input and readout clocks
- Readout mode (normal, calibration or test mode)
- Readout rate (delay between readout cycles)
- External flow control enable
- Threshold values for high/low gain selection
- Seed for the test pattern generator
- Pedestal DAC value settings

The ADC input clock phase is adjusted to ensure that the PMT pulses are all sampled at their maxima. This adjustment is performed using test pulses produced by the 3-in-1 cards and the TileCal laser system.

The clock phase of the Tile-DMU outputs is adjusted to ensure proper readout timing. The timing in of this clock is performed by varying the phase while running the Tile-DMUs in test mode with a suitable data pattern.

2.5 Testability

There are a number of test points that are continuously monitored via flags in the headers. Single and double bit errors occurring in the TTCrx are reported, as well as the occurrence of parity errors in the memory. There are also means to supervise the combined parity of all programmable registers as well as dynamic registers such as address pointers and state variables. The combined dynamic parity bits from each Tile-DMU should be identical.

The sample data are protected by CRC-16 check sums and horizontal parity bits. The alignment of the data is routinely monitored at the receiving end of the readout link.

3. PRODUCTION AND VERIFICATION

3.1 Tile-DMU design and production

The Tile-DMU is implemented using the CX3161 gate array from Chip Express [7]. This device has 33-48k usable gates and is produced in 0.35µ CMOS, with up to 208 I/Os and 64 kbit of embedded 3 ns memory. The maximum system speed in this device is nearly 200 MHz, which is much greater than the 40 MHz nominally required for the Tile-DMU design. The gate array consists of a large number of identical predefined blocks, which simplifies the design of clock distribution networks. A large number of available macros help to reduce the design effort. These macros include RAMs, PLLs and I/O-driver configurations. The Tile-DMU was synthesized from a high level description in VHDL, using Leonardo from Exemplar logic. Design checks were performed using the Chip Express design kit.

Two small rounds of prototypes were received for evaluation. These prototypes have been used in test beam tests at CERN. One prototype round proved to have occasional parity errors in the memory, while in the other round, these errors have not been observed.

3.2 Radiation tolerance

Expected radiation levels in the drawers are 0.2 krad/year from ionizing radiation, and a neutron fluence of 10^{11} 1-MeV-equivalent neutrons/cm^2/year [1]. Adding appropriate safety margins, the CMOS components of the system should be able to operate after being exposed to 10 krad of ionizing radiation and $5x10^{12}$ neutrons/cm^2. For bipolar components the corresponding numbers are 50 krad and $7.5x10^{12}$ neutrons/cm^2

We have performed tests of 10 to 25 samples of all active components used in the design except the Tile-DMU. Only a few components have to be replaced and the AD converter has passed the tests without failure.

The Tile-DMU technology has been shown to be radiation tolerant [8]. We have tested a ring counter implemented in the same technology with both ionizing and neutron radiation with good results. A sample of the production Tile-DMU will be tested later this year. The production version of the TTCrx is implemented in radiation-hard DMILL technology [9].

3.3 Experiences from Test-beam

The TileCal Digitizer was tested in Module 0 beam tests during the summer of 1999. The noise contribution from the digitizer boards proved to be small. The total high frequency noise in the high gain channels was approximately 1.3 ADC counts (200 MeV), and the corresponding number in the low gain channels was about 0.6 ADC counts (600 MeV) (Fig.6). These numbers include noise contributions from both the digitizer and the 3-in-1 system. The contribution from the digitizer alone was estimated to be 0.5 ADC counts in both cases. This estimate was based on SPICE simulations on the 3-in-1 system.

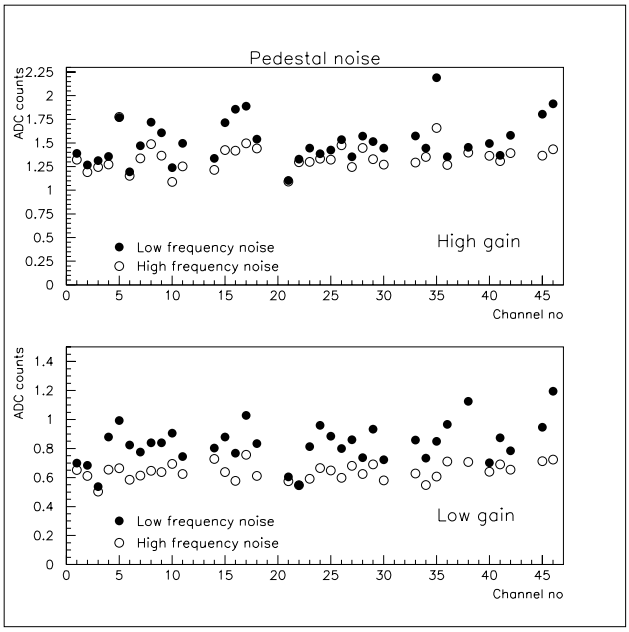

Fig. 6: Pedestal noise for high and low gain channels

The electronics system is calibrated using charge injection pulses provided by the 3-in-1 cards. Five reconstructed pulses of varying charges in one high gain channel are seen in Fig. 7.

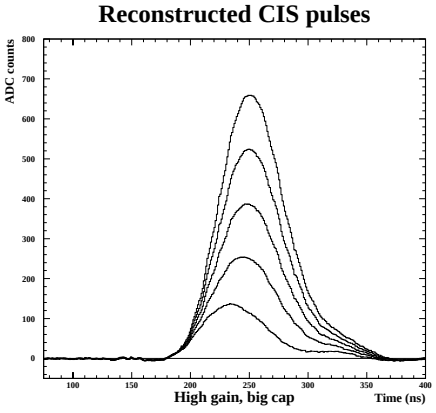

Fig. 7: Five reconstructed pulses of varying charge

The linearity of the system is shown in Fig. 8. In the top plot an energy estimate of the pulse is plotted versus the injected charge for the high and low gain values of one channel. In the bottom plot one finds that the deviations

from the linear fits are well below 1%, thus fulfilling the linearity requirement on the system.

The digitizer system proved to be mechanically and electrically stable except for some problems with SMD connectors.

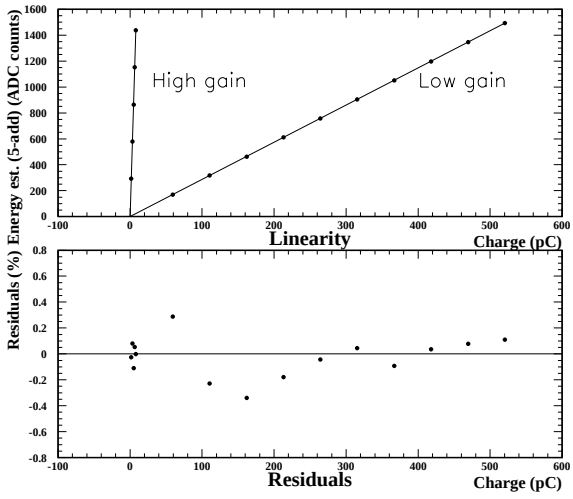

Fig. 8: Linearity of the digitizer system

4. FUTURE UPGRADES

Final production of the Tile Digitizer is scheduled for 2000. Several changes in the design, are being considered, including minor modifications to the Tile-DMU, mechanical improvements, and a new readout link technology.

4.1 Modifications to the Tile-DMU

Some minor modifications to the Tile-DMU design were motivated by test beam experiences. These modifications include inserting the bunch crossing identification number (instead of the even number) in the header, as well as possible improvements to the flow control scheme to simplify communication with the link interface.

4.2 Mechanical improvements

Integration of the TileCal digitizer in the summer 1999 beam tests revealed reliability issues with the SMD and power connectors used in the prototype digitizer boards. Replacements have been found for these parts, and will be included in the final pre-production version of the digitizer system.

The next version of the digitizer boards will also feature a slightly reduced board length to ease drawer assembly.

4.3 Readout Links

The readout interface used in beam tests of the prototype digitizer systems used fiber-channel S-link cards. Unfortunately, there is currently no sufficiently radiation tolerant version of this technology.

The production version of the digitizer system will require a new readout link interface with better radiation tolerance and higher bandwidth. Possible solutions are currently being investigated.

5. CONCLUSIONS

A pre production version of the digitizer system for the ATLAS Tile calorimeter has been designed, built and tested. Most design requirements have been satisfied. Experiences from the system integration and the analysis of test beam data have suggested minor changes which will be implemented in the final version. A small pre production version will be tested towards the end of next year.

ACKNOWLEDGEMENTS

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