RADIATION HARDNESS OF THE ABCD CHIP FOR THE BINARY READOUT OF SILICON STRIP DETECTORS IN THE ATLAS SEMICONDUCTOR TRACKER

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Abstract

The radiation hardness requirements of the ABCD chip are driven by the radiation levels expected in the ATLAS SCT after 10 years of LHC operation, which are 10 Mrad of total ionising dose and 2×10^{14} n/cm^2 of 1 MeV eq neutron fluence for the displacement damages.

The ABCD chip, comprising both analogue and digital circuitry and realised in a BiCMOS technology, is sensitive to ionisation effects as well as to displacement damages. The recent prototype of the ABCD chip, which meets all SCT requirements, has been irradiated separately with X-ray, neutrons from a nuclear reactor, and with 24 GeV protons. In the paper we present and discuss the radiation effects observed in the ABCD chip.

1. INTRODUCTION

The development of the ABCD chip for the binary readout of silicon strip detectors in the ATLAS Semiconductor Tracker [1] has been completed recently. The architecture of the ABCD design is reminded here very shortly since it has been presented and described before [2]. The block diagram of the chip is shown in figure 1. It comprises all blocks of the binary readout architecture, the front-end circuits, discriminators, binary pipeline, derandomizing buffer, data compression logic, and the readout control logic.

The first ABCD prototype chip met most of specification, however, the spread of the discriminator threshold in the front-end was not satisfactory. Analysis of the problem led us to a conclusion that given the matching performance of the DMILL technology, in which the chip was realised, we could not guarantee the required performance, following the original circuit concept. In addition, the performed irradiation tests indicated that matching performance degraded significantly after irradiation. Therefore, we upgraded the design by implementing a threshold correction using a digital-to-analogue converter (TrimDAC) per channel.

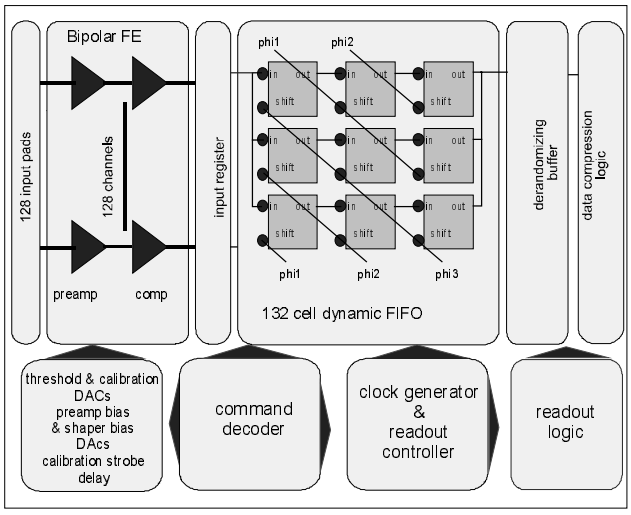

Fig. 1. Block diagram of the ABCD chip.

The prototypes, ABCD2T and a slightly tuned version of the original design (ABCD2NT - without TrimDACs), have been manufactured successfully. Both versions are fully functional and meet the specifications. The performance and parameters of the two versions are presented and discussed in another paper [3].

In this paper we focus on the radiation hardness issues of the ABCD2T chip since this option has been chosen as a preferred one for the SCT. There are two important aspects to be taken into account when considering the radiation hardness of the ABCD2T chip:

(a) the chip is realised in a BiCMOS technology so one has to pay attention to the ionisation effects as well as to the displacement damages,

(b) there is a number of specific effects related to the ABCD2T architecture and particular circuit implementations.

The DMILL technology is qualified as a radiation resistant one. However, the radiation levels expected for the SCT detector in the ATLAS experiments are at the upper limits of those specified for the DMILL process, i.e. 10 Mrad of the ionising dose and 1×10^{14} n/cm^2 1 MeV eq. neutron fluence. In addition, if one takes into account very advanced requirements regarding the noise, speed and power consumption of the ABCD2T chip, it becomes obvious that radiation effects in the basic devices, although limited, can not be ignored.

2. RADIATION HARDNESS ISSUES

On top of a general requirement that the chip should be fully functional after irradiation up to the maximum specified levels, there are some particularly critical issues of the ABCD design, which should be considered carefully with respect to radiation effects. The most critical aspects are: noise of the front-end, matching in the front-end circuit, in particular the offset spread of the discriminator, and the speed of the digital CMOS part.

2.1 Noise

The front-end circuit of the ABCD2T chip is built as a transimpedance amplifier using a bipolar input transistor. One of the noise sources, which contribute to the equivalent input noise charge is the shot noise of the base current of the input transistor. Due to a short shaping time of 25 ns, as required for the SCT readout, and a large detector capacitance, the relative contribution of this noise is acceptable as long as the base current does not exceed a level about 2 μA. For given detector capacitance, shaping time and current gain factor β of the input transistor, one can find an optimum value for the collector current which yields a minimum value of ENC.

In modern bipolar transistors the current gain factor β is degraded by the ionisation effects as well as by the displacement damage. Both types of radiation effects, ionisation and displacement damage, lead to reduction of the lifetime of minority carriers in the transistor base. Thus, a significant degradation of β has to be anticipated, which implies that first of all the circuit design has to be insensitive to variation of β, regarding DC bias conditions as well as AC characteristics. With respect to noise there are two aspects to be taken into account, namely the size of the transistor and the collector current in the input transistor.

The degradation of β depends on the actual current density in the transistor, therefore from that stand point of view one would prefer to use a minimum geometry transistor in the input stage. On the other hand, in order to minimise the series noise contribution from the base spread resistance, one would rather use a large area input transistor. These two requirements are contradictory and an optimum size of the input transistors can be defined provided we know how the β degrades after irradiation for a given technology. The radiation effects in the bipolar transistors in the DMILL technology have been studied and based on these results [4] we chose the emitter area of the input transistor to be 1.2×10 μm^2.

From the radiation tests performed up to now we expect that β of the input transistor will change significantly, by a factor of about 4, during the lifetime of the ATLAS experiment. With the β value decreasing during the lifetime of the experiment the optimum value of the collector current in the input transistor will also decrease. Therefore we have implemented a 5-bit DAC to be able to adjust the current and optimise the noise performance according to the actual value of β in the input transistor. In addition, the bias current in the following stages of the front-end amplifier is also controlled by another 5-bit DAC, which allows to adjust DC biasing of the circuit and compensate the drifts due to decrease of β in the bipolar transistors, shifts of the threshold voltages in MOS transistors and increase of resistor values.

2.2 Matching

One of the most critical issues of the binary architecture, as implemented in the ABCD design, is the matching of parameters of the front-end circuit since a common threshold for 128 channels in one chip is used. The effective threshold of the discriminator is determined by the offset of the discriminator and by the gain of the amplifying stages preceding the discriminator. The preamplifier stage has to be implemented in a single-ended configuration and the gain of the circuit is sensitive to variation of resistors which are used in the feedback loops. Thus, channel-to-channel matching of the gain is limited by the resistor matching across the whole chip. The discriminator circuit is based on a fully differential structure so that the offset of the discriminator is determined by the local matching of resistors and transistors.

From the tests performed for the previous ABCD prototype we have drawn the following conclusions:

(a) matching of resistors is a limiting factor for the offset spread in the discriminator,
(b) matching performance of resistors, which are available in the DMILL technology, is not sufficient to guarantee that the SCT requirements regarding the threshold spread can be met using the original scheme of the discriminator,
(c) matching of resistors degrades significantly after irradiation.

Taking these aspects into account we have proposed and implemented a scheme with individual threshold correction per channel. This is realised by 128 4-bit DACs (TrimDACs) implemented in ABCD2T design.

2.3 Speed of digital CMOS blocks

The digital part of the ABCD chip comprises a number of various blocks, including static and dynamic logic, synchronous and asynchronous circuits. The chip is required to work at a clock frequency of 40 MHz for any set of corner parameters as specified by the vendor, including the changes after irradiation up to 10 Mrad. In addition, the ABCD chip is designed for a digital power supply of 4 V, which is below the nominal supply voltage of 5 V specified for the DMILL technology. In order to cover possible variation of the process parameters, temperature, supply voltage and post-radiation changes, the digital part of the ABCD chip was designed to work at least at a clock frequency of 80 MHz for the typical process parameters before irradiation and for supply voltage of 4 V.

3. IRRADIATION TESTS

The ABCD2T chips have been irradiated in three different experiments:

(a) with 24 GeV proton beam using the T7 irradiation facility at CERN PS accelerator,
(b) with neutrons from the nuclear reactor at Ljubljana,
(c) with X-ray of 10 keV using a standard X-ray facility at CERN.

The proton and the neutron irradiation have been performed for the chips mounted on the ceramic hybrids of the same type as foreseen for the final SCT modules. On each hybrid there was 6 chips, 3 ABCD2T chips and 3 ABCD2NT chips. In this paper we discuss only the results obtained for the ABCD2T chips with the TrimDACs since this option has been chosen for further evaluation. During irradiation the chips were biased and clocked at nominal conditions and the trigger signal was sent in order to exercise all readout blocks in the chips in a similar way like they will work in the experiment.

During proton irradiation the hybrid with the chips was kept inside a cold box filled with nitrogen at temperature about 2°C, while the measured temperature of the hybrid was higher, about 10°C. The proton beam of the size about 1×2 cm^2 was scanned across the hybrid. The chips were irradiated up to a fluence of 3×10^{14} p/cm^2 during a period of 10 days. The measurements were taken every one or two days, depending on the beam intensity. All basic parameters and characteristics were measured, including the noise and threshold spread, for various bias currents in the input transistor.

During the neutron irradiation the chips were biased and clocked in the same way as during the proton irradiation, however, the thermal conditions were different. The chips were not cooled and the temperature of chips was about 40 °C.

The X-ray irradiation was performed for single chips mounted on an evaluation board. The bias and clocking conditions were similar to those used in the proton and neutron irradiation. In the X-ray test we focused on performance of the CMOS digital part of the chip.

In the radiation tests performed so far no particular annealing procedure was applied. The measurements were taken during irradiation or immediately after irradiation. This represents a worst case for the CMOS part since the radiation induced effects in CMOS components exhibit some annealing, which naturally will take place during irradiation with a low dose rate. For the bipolar components the performed tests represent an optimistic scenario due to the dose rate effect, which for bipolar devices means that an irradiation with a high dose rate is less damaging compared to an irradiation up to the same total dose but with a lower dose rate.

4. TEST RESULTS

The radiation test results regarding the chip performance and parameters are discussed in this section. It is important to note that all the results presented were obtained from standard test procedures in which the signal passes the whole data chain, from the internal calibration circuitry through the front-end, pipeline, and the readout circuitry.

4.1 Basic functionality

Given extreme radiation levels, which we used in our tests, a first question was whether there were no catastrophic failures in the chips which would prevent us from detailed measurements of chip parameters. For all performed irradiation we did not observe any of such a failure in the ABCD2T chips, i.e. the analogue parts remained biased correctly and the digital parts worked at least at 40 MHz.

The gain of the front-end circuit as a function of the current in the input transistor after X-ray, proton and neutron irradiation is shown in figure 2. The average gain of 128 channels in one chip is shown for each case. One can notice that after all irradiation tests the circuit still works for a wide range of the preamplifier current. A significant degradation of gain is observed after extreme neutron irradiation up to a fluence of 2×10^{14} n/cm^2.

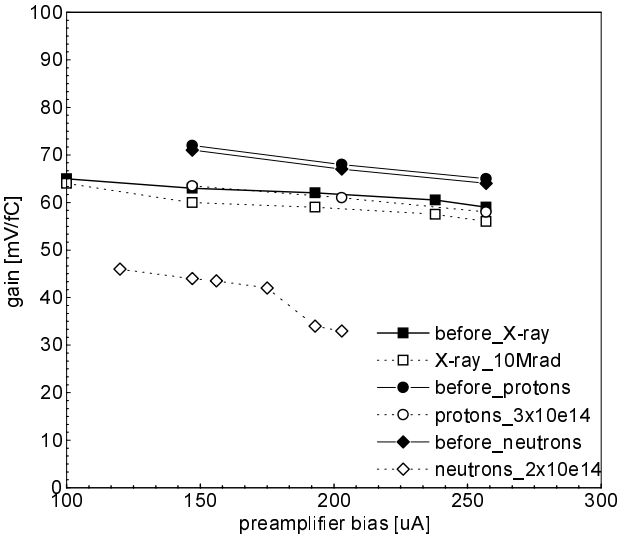

Fig. 2. Gain as a function of the current in the input transistors after X-ray, proton, and neutron irradiation.

4.2 Noise

The irradiated chips have been measured with open inputs so that the capacitance at the preamplifier input can be neglected in a first approximation. Thus, the equivalent noise charge is determined by the parallel noise sources, i.e. thermal noise of the feedback resistor and the shot noise of the base current. Assuming that the changes of the feedback resistor after irradiation are negligible, one can associate the increase of noise with a higher base current due to degradation of β in the input transistor. Figure 3 shows the noise as a function of the current in the input transistor for the same three chips, for which the gain is shown in figure 2. Again, average noise for 128 channel in one chip is shown. After X-ray irradiation we see a small increase of noise as expected since one does not expect a significant degradation of β in this case. For the chips irradiated with relativistic

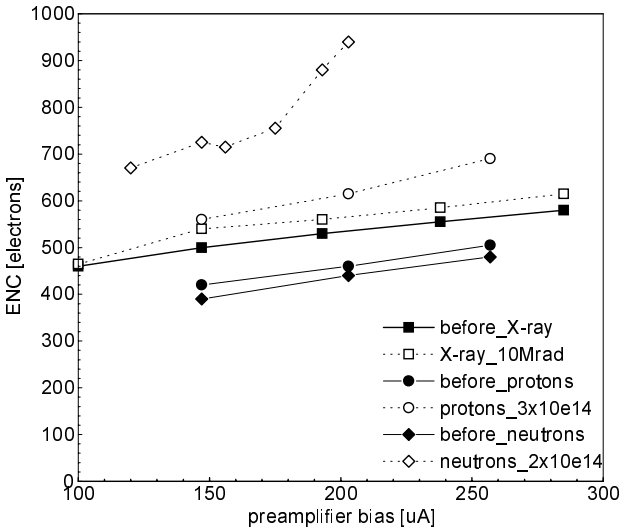

Fig. 3. Noise as a function of the current in the input transistors after X-ray, proton, and neutron irradiation.

protons up to 3×10^{14} p/cm^2 the increase of noise is significant. A large increase of noise is observed after neutron irradiation up to 2×10^{14} n/cm^2. Qualitatively this is consistent with the decrease of gain as shown in figure 2. Assuming that the shaping function of the overall front-end circuit can be approximated by a CR-RC^3 filter with a peaking time of 25 ns one can evaluate the β values corresponding to the measured noise levels, as about 60 after proton irradiation and about 30 after neutron irradiation respectively.

4.3 Matching

The irradiation tests were supposed to provide answers for two questions regarding influence of irradiation on the matching of device parameters:

(a) does the matching degrades after irradiation and,
(b) if so, is the range of the TrimDACs sufficient to cover the post radiation offset spread,

Figure 4 shows the distributions of discriminator threshold for 128 channels in one chip before irradiation (without correction), after proton irradiation up to a fluence of 3×10^{14} p/cm^2 (without correction), and after irradiation and threshold correction using the TrimDACs. One can notice a very significant degradation of threshold spread, by a factor of 3.5, after proton irradiation. After irradiation the TrimDACs work correctly and for majority of channels the offset can be corrected, however, some channels remain outside the range of the TrimDACs. These channels appear as flat tails in the distribution shown in figure 4c.

A similar behaviour of threshold spread was observed after neutron irradiation, however, the effect was smaller. After a fluence of 2×10^{14} n/cm^2 the threshold spread increased by a factor of 2 and in this case the range of the TrimDACs was sufficient for effective correction of the threshold in all channels in the chip.

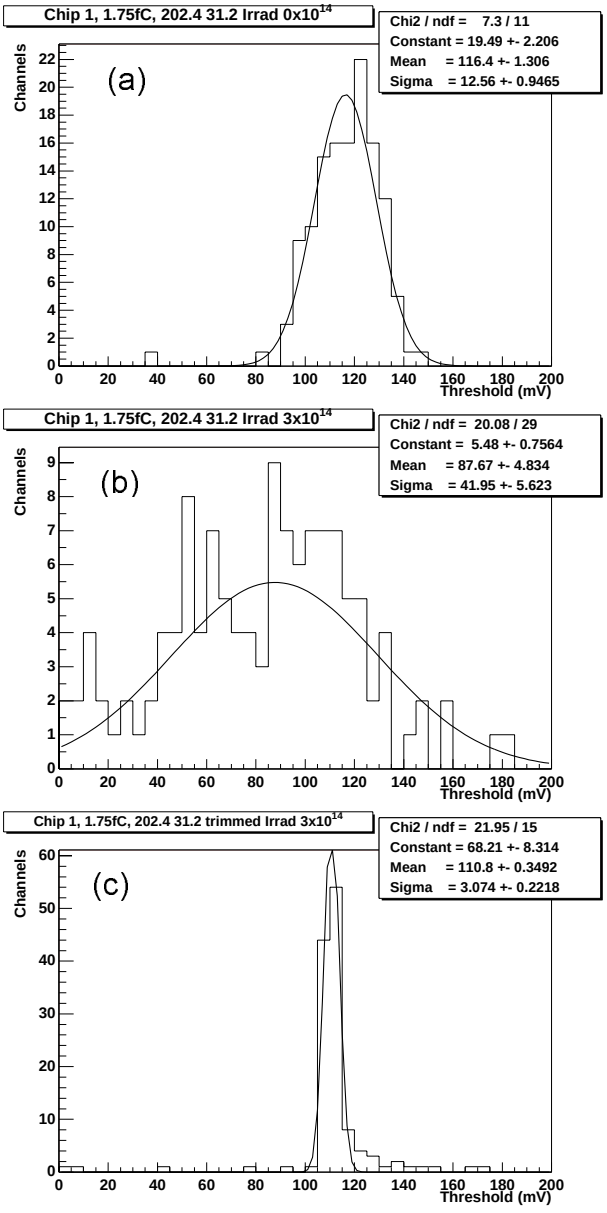

Fig. 4. Threshold spread: (a) before irradiation without trimming, (b) after proton irradiation without trimming, (c) after proton irradiation with trimming.

4.4 Performance of digital circuits

Regarding the radiation effects in the digital CMOS circuitry of the ABCD2T chip, a main concern is the speed, i.e. the maximum clock frequency at which the chip performs correctly all operations. Since the speed of the CMOS circuits depends on the power supply there are two parameters which provide information about the speed margins of the ABCD2T chip:

(a) maximum speed measured at the nominal supply voltage of 4 V,

(b) minimum supply voltage at which the chip works correctly at 40 MHz.

Figure 5 shows the degradation of speed of the ABCD2T chip after X-ray irradiation up to a total dose of 10 Mrad.

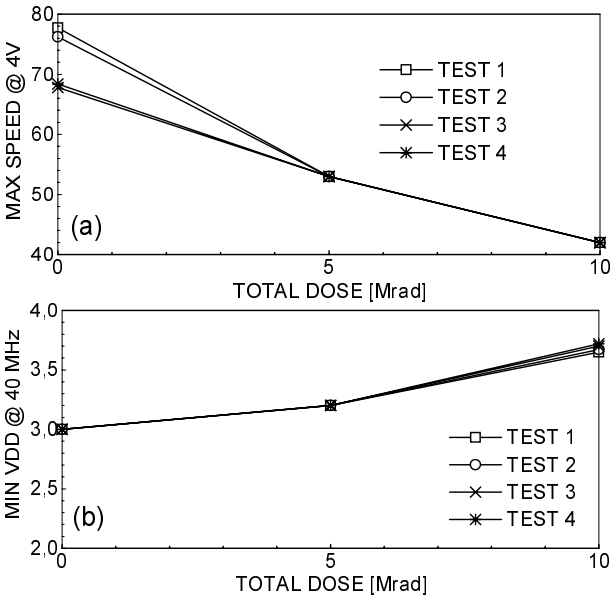

Fig. 5. Maximum speed at supply voltage of 4 V (a) and minimum supply voltage at 40 MHz (b) as a function of total ionising dose.

The results are shown for the following digital tests: TEST 1 - L1/BC counters check, TEST 2 - configuration check, TEST 3 - L1 overflow check, TEST 4 - data taking. We observe a degradation of speed almost by a factor of 2, nevertheless, after 10 Mrad the chip still meets the requirement of 40 MHz at the nominal supply voltage. It is worth to note that the results shown in figure 5 do not include any annealing so that they represent worst case post-radiation conditions.

5. CONCLUSIONS

Extensive irradiation tests of the ABCD2T prototype chips confirmed satisfactory radiation hardness of the design and the DMILL technology, in which the chip has been realised. The individual threshold adjustment per channel implemented in the ABCD2T design has been proved to work satisfactory after irradiation.

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