DMILL IMPLEMENTATION OF THE ANALOGUE READOUT ARCHITECTURE FOR POSITION SENSITIVE DETECTORS AT LHC EXPERIMENTS

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Abstract

The SCTA128HC chip with analogue readout architecture for position sensitive detectors at LHC experiments has been developed using the DMILL process. The chip comprises all functional blocks required for the analogue readout architecture, preamplifier, shaper, analogue pipeline, derandomising buffer, analogue multiplexer and readout circuitry. It suits well for the readout of silicon detectors in a wide range of detector capacitance (from 0 to 25 pF). The design has been manufactured successfully in the DMILL technology. The design and the test results from the prototypes are presented.

1. INTRODUCTION

Following the demonstrators of the analogue readout architecture, SCT32A and SCT128A, developed in the course of implementation of the DMILL technology we have designed and manufactured a 128-channel prototype chip using the stabilised DMILL process [1]. The new design follows the architecture of the SCT128A chip [2], however, some blocks have been redesigned and some other added in order to make the chip compatible with the overall detector readout system [3][4]. The number of external control signals necessary to operate the chip has been reduced by implementation of a 40 MHz serial interface (only one clock and one command line). All signals to control readout of the analogue memory (Analogue Data Buffer – ADB) and the output multiplexer are generated in the chip by an internal sequencer. To improve the testability of the chip an internal calibration circuit has been implemented.

In order to be able to use the chip with detectors of various capacitances and to optimise the front-end noise performance for a given input capacitive load, the internal bias generators controlled by DACs integrated in the chip have been implemented. This solution allows for compensations of the bias drifts due to radiation effects expected in the devices used. The front-end circuit supports both, the positive and the negative polarity of the input signal.

2. THE ARCHITECTURE

Figure 1 shows the block diagram of the SCTA128HC chip architecture. The chip comprises five basic blocks: front-end amplifiers, analogue pipeline (ADB), control logic including the derandomizing FIFO, command decoder and output multiplexer.

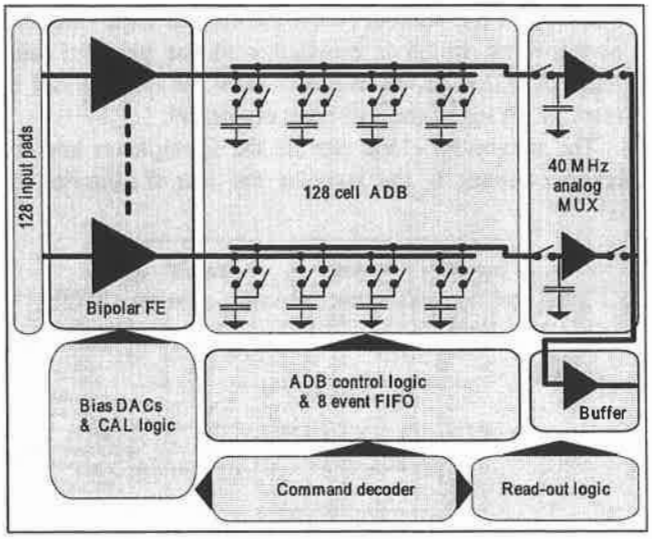

Fig.1. Block diagram of the SCTA128HC chip.

The front-end is a fast transimpedance amplifier, based on a bipolar input transistor, followed by an integrator providing a semi-gaussian shaping with peaking time of 25 ns. The peak values are sampled at 40 MHz rate and stored in the 128-cell deep analogue pipeline. The derandomising function is realised by means of an additional FIFO in which up to 8 addresses of cells containing valid data can be stored. Upon receiving a trigger signal the data is read out through the fast 40 MHz analogue multiplexer.

The bias currents of the input transistor, integrator and readout amplifiers are controlled by 5-bit DACs. In order to improve the testability of the chip an internal calibration circuitry has been implemented. The circuitry allows to generate calibration pulses with the amplitudes controlled by an 8-bit DAC and the delay with respect to the clock phase controlled by an internal delay circuit. One of the four internal calibration lines can be selected by a 2-bit address. Communication with the chip is provided with the command decoder which controls all mentioned above circuits as well as the readout logic.

3. READOUT PROTOCOL

The readout logic is designed in such a way that two 128-channel chips can be read out via one analogue link. Upon receiving the trigger signal the data is sent first from one chip while the second one connected to the same fibre waits for the appropriate number of clock cycles before sending the data. The data package from each chip consists of a 4-bit header, three analogue values which can be used for calibration of the optical links, 1-bit FIFO overflow flag, 4-bit BCO counter and 4-bit Level-1 trigger counter. Figure 2 shows the scope view of a read-out sequence at nominal readout speed of 40 MHz.

The 4-bit BCO counter and L1 counter returned by the chip can be used for synchronisation of each trigger with the physical data from the detector. In the case of overflow of the readout buffer the control logic issues an overflow bit which is bundled with the physical data. After detection of the overflow error the chip should be reset by means of the soft-reset command.

The maximum clock rate of the multiplexer and the readout circuit is the same as the rate of sampling the data, i.e. 40 MHz. The chips can be read out with a lower rate (40 MHz divided by 2, 4 or 8) which is programmable. All communication with the chip i.e.:

- sending the level 1 triggers,
- sending the software reset,
- loading the DACs,
- issuing the internal calibration pulses
- programming the speed of the output MUX

is executed via the fast 40 MHz serial interface.

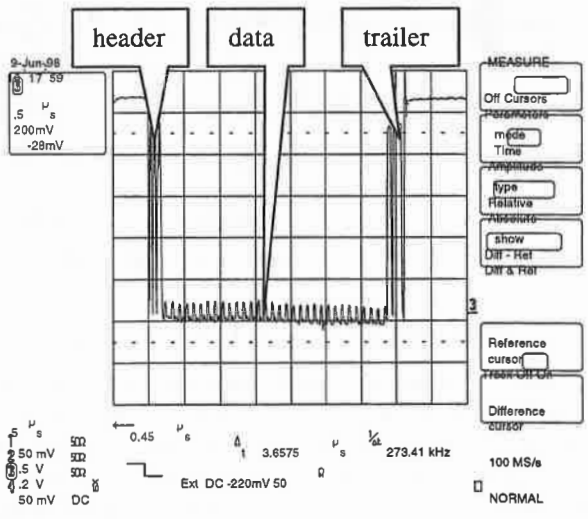

Fig.2. Response of the chip to a 4 fC calibration signal injected in every fourth channel.

4. LAYOUT

Figure 3 shows the layout of the SCTA128HC chip. The front-end channels and the analogue pipeline are laid out with a pitch of 42 μm. Input bonding pads are laid out with 60 μm pitch. The bond pads for supply voltages and control signals are located on both sides of the chip. The die area is 7.9×8.0 mm^2 of which about 30% is occupied by the storage capacitors in the ADB.

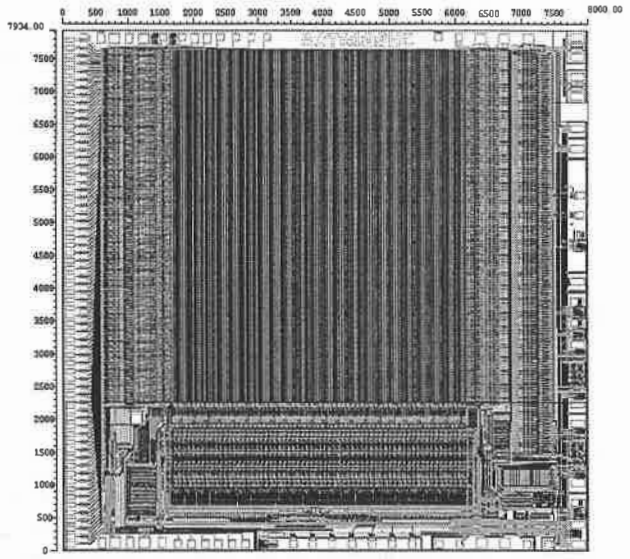

Fig.3. Layout of the SCTA128HC chip

5. TEST WITH CALIBRATION PULSE

The evaluation of the chip performance has been done using a test set-up built of a VME sequencer module (SEQSI) and a VME data acquisition module (SIROCCO) running under OS9 system or via a PC-VXI interface. All presented tests have been done using internal calibration circuitry. The noise measurements have been done using statistics of 500 triggers for each scan point. The data has been analysed using the ROOT package.

5.1 Front-End Performance

The concept of the SCT128HC design is based on a fast front-end circuit providing the peaking time of 25 ns which matches the sampling frequency of 40 MHz. This way only one sample of the peak value for each pulse is stored in the ADB.

The pulse shape at the output of the shaper can be reconstructed by scanning the delay of the calibration signal with respect to the clock phase so that a different time slice of the pulse is readout for each scan point. Because the internal delay register is built as a simple chain of inverters it is not designed for an absolute delay value. Since the range of this register is about 50 ns, allowing delay scans across latency of two consecutive triggers, a cross calibration with an external 40 MHz clock is possible. For the present batch a factor of 1.2 has been obtained. Figure 4 shows the result of one delay scan for a particular channel of the SCTA128HC chip. The injected charge was 6 fC. The obtained peaking time matches very well the design value of 25 ns.

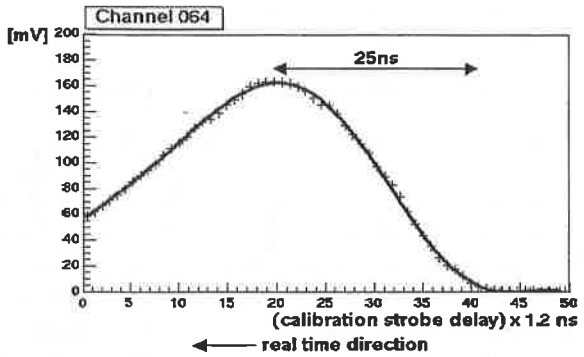

Fig.4. Pulse shape at the multiplexer output obtained from the delay scan. The injected charge was 6 fC.

Varying the amplitude of the calibration signal for the optimum value of delay, the linearity of the gain has been obtained. Figure 5 shows the gain linearity measured for one particular channel. The SCTA128HC chip has good linearity up to 12 fC which is sufficient for tracking applications.

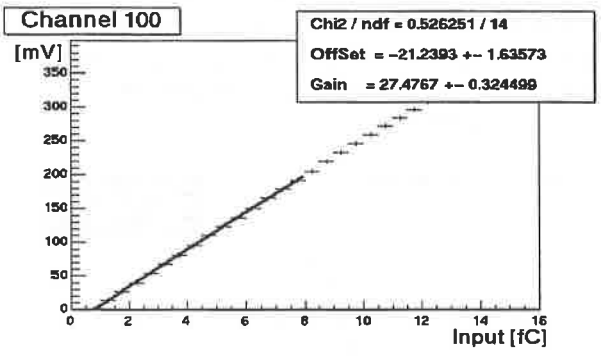

Fig.5. Gain linearity for a single channel.

The gain distribution of 128 channels in one SCTA128HC chip is shown in Fig. 6. The mean value of gain is about 25.5 mV/fC and the spread is 0.9 mV rms, i.e. 3%. Although the uniformity of gain is not a very critical issue for the analogue architecture the obtained figure allows use of the chip without off-line correction.

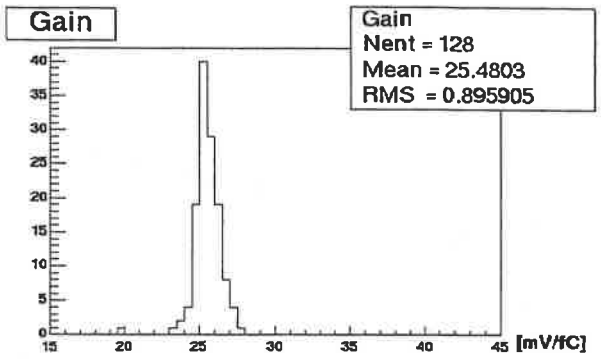

Fig.6. Distribution of the front-end gains in one SCTA128HC chip.

The noise measurements have been performed for the full chip operating at the clock frequency of 40 MHz. The noise was measured by random reading of cells of the pipeline so the measured value includes cell-to-cell variations in the pipeline. Figure 7 shows results of the noise measurements obtained for different currents in the front-end transistor. The two groups of channels at the edges of the chip were connected to a 6 cm long strip detector with total strip capacitance about 9.5 pF while the inputs of the central part of the chip were left open. For the channels with open inputs one can notice dependence of noise on the base current in the input transistor. For the channels connected to strips the resulting noise is the sum of the parallel noise and the series noise which vary in opposite directions with the bias current of the input transistor. As a result the noise is almost constant over quite wide range of the input transistor current.

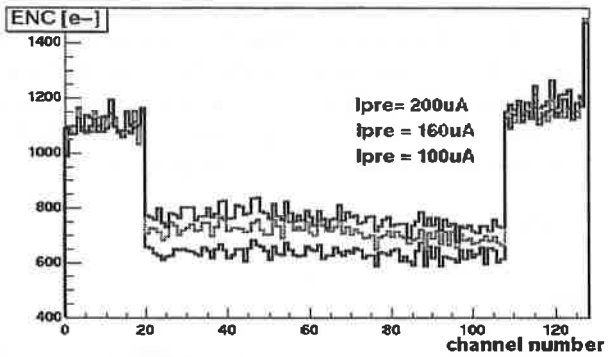

Fig.7. Distribution of ENC noise in a single SCTA128HC chip. The 20 channels on each side were connected to the silicon strip detector.

In figure 8 the mean values of noise for the open and the loaded channels are plotted as a function of the load capacitance, 0 and 9.5 pF respectively. For the bias current of 200 μA in the input transistor the obtained noise figure of ENC = 757 + 38 e⁻/pF is in a good agreement with the results obtained for the previously developed SCT32A prototype [2].

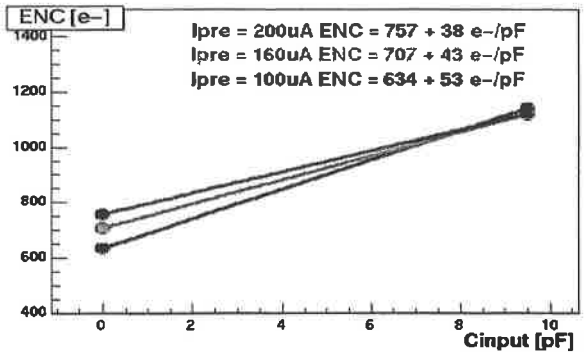

Fig.8. ENC noise slope for the different bias condition of the input transistor.

5.2 Analogue pipeline performance

Since the SCTA128HC chip performs very simple voltage sampling where only analogue information is stored/retrieved from the pipeline the pedestal spread between ADB cells contributes as an additional noise source. By varying the delay between software reset (reset of the write/read pointer in the ADB) and the trigger sent to the chip it is possible to obtain the ADB pedestal map. Figure 9 shows the ADB pedestal map (128 cells × 128 channels) for one particular SCTA128HC chip. From the presented figure one can extract the cell-to-cell pedestal variation as well as variation of the DC offsets between channels.

The spread of the DC offsets between channels is in the range of 20 mV peak-to-peak while the spread of the pedestals along one channel of the ADB is in the range of 5 mV peak-to-peak. The distribution of the pedestals in one particular channel is shown in Fig.10. The spread value of 1.2 mV rms has to be compared with the gain of 25 mV/fC which gives an additional contribution of 300 el rms to the noise generated in the front-end. For a low bias current in the input transistor and a low detector capacitance the additional contribution is about 10% of the overall noise at the output. For higher detector

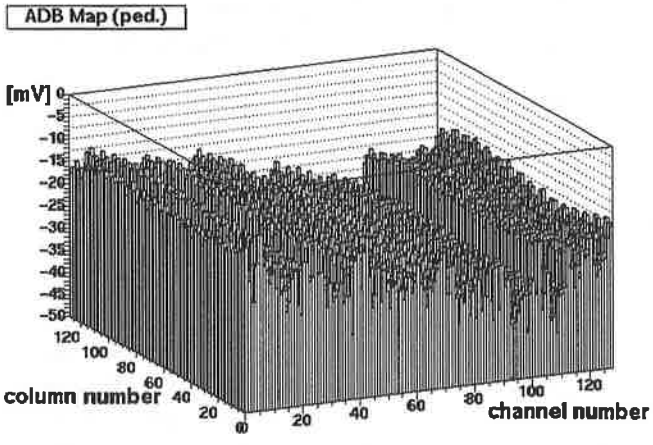

Fig.9. Map of the pedestals in the ADB.

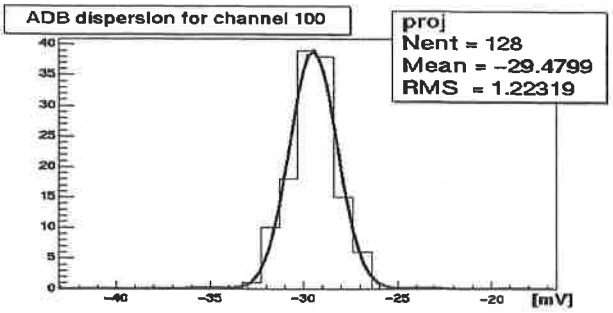

Fig.10. Pedestal distribution of 128 ADB cells in one particular channel.

capacitances and respectively higher currents in the input transistor required for optimisation of noise this contribution becomes negligible.

6. CALIBRATION WITH β PARTICLES

In order to perform absolute calibration of gain and noise the chip was connected to a small 1×1 mm diode. The thickness of the diode was 300 μm and the capacitance was 1 pF. The response to β-particles from a ^{106}Ru radioactive source was measured at the detector bias of 150 V. For each trigger event provided by a scintillator the delay with respect to the clock phase was measured by a TDC module. For the analysis presented below only the events from a 5 ns wide time window around the peak were taken. No signal clustering and no common mode substraction algorithms have been employed in data analysis.

The distribution of the signal amplitude is shown in Fig. 11. By fitting this distribution to the Landau distribution one obtains the peak value of 89.7 mV which corresponds to the gain of 24.9 mV/fC (89.7mV/3.6fC). The above value of gain is in good agreement with the gain of 25.5 mV/fC as obtained from the electronic calibration (see Fig.6). This result indicates that the parameters of the internal calibration circuitry, i.e. the calibration DAC and the test capacitors are close to the nominal designed values.

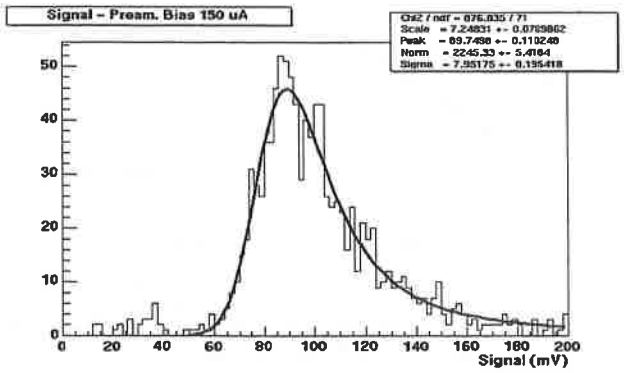

Fig.11. Distribution of signal amplitude from a silicon diode exposed to β-particles.

It must be mentioned that the most probable charge (peak of the Landau distribution) deposited by ^{106}Ru β particle here is assumed to be 22500 eh pairs. Other measurements indicate that the true value is around 20000 eh pairs, as expected from the energy of the β particles being at the minimum of the ionisation curve. Final calibration which is in the progress, may increase therefore the value for the voltage gain by about 10 %.

7.PERFORMANCE OF THE SCTA128HC CHIP WITH A STRIP DETECTOR

In order to demonstrate the performace of the SCTA128HC chip when used for the readout of a silicon strip detector a bench test was performed using β-particles from a ^{106}Ru radioactive source. The chip was connected to a 6 cm long, 350μm thick p-type detector with the strip pitch of 25 μm. The readout pitch of 50 μm was used with one intermediate strip providing capacitive charge division. The total strip capacitance was about 9.5 pF. The detector was biased at 200 V. The input transistor was biased at 200 μA.

The histogrammed result of clustered signal/noise is shown in Fig.12. The Landau peak of the signal/noise is equal to 22.2. The measured common mode noise was about 1.3 mV RMS and contributed additional 5% to total noise of the system.

The cluster multiplicity is shown in figure 13. One can see that due to relatively narrow pitch and charge division structure in the detector majority of events result in 2-strip and 3-strip clusters. The mean signal is about 15% smaller compared to the value obtained from the small pad detector mostly due to charge loss on intermediate strips via their capacitance to the backplane.

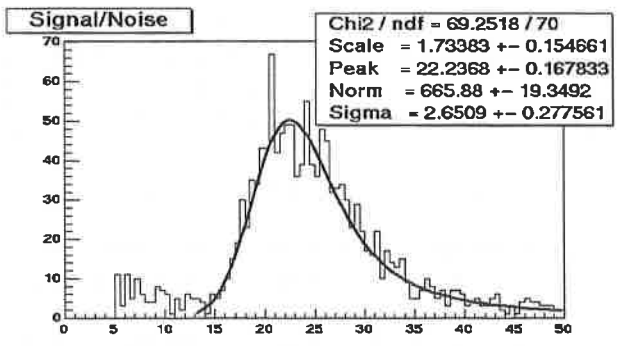

Fig.12. Distribution of clustered signal/noise for β-particles measured with the strip detector.

In the readout logic of the SCT128HC chip a special feature has been implemented which allows for reading of up to 8 consecutive triggers. Using this feature we can see a snap shot of a single pulse along the channel of the ADB. Figure 14 shows a typical response to a single β-particle along the ADB cells. One bin corresponds to 25 ns.

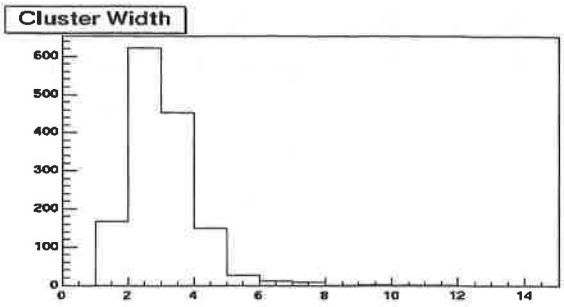

Fig.13. Histogram of signal cluster width.

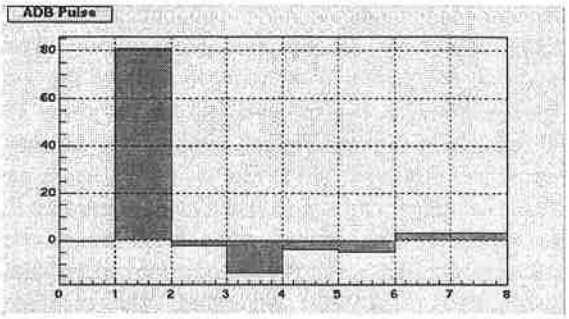

Fig.14. Snap shot of a single β particle signal along the ADB cells. One bin corresponds to 25 ns.

One can see that all the signal is stored in a single 25 ns time slot. Small undershoot is visible as expected. The system can easily provide double pulse resolution of 50 ns as required.

8. CONCLUSIONS

A prototype readout chip with complete analogue architecture has been developed and manufactured in the DMILL technology. The architecture of the design and the implemented readout protocol make the chip compatible with the requirements for the readout electronics of silicon strip detectors in the LHC experiments. The noise and timing performance of the front-end circuit has the required performance for application in a LHC Si tracker.

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