The ENABLE Machine
A Systolic Second Level Trigger Processor for Track Finding*

F. Klefenz[1], R. Zoz[1], K.-H. Noffz[1], R. Männer[1,2]

[1] Lehrstuhl für Informatik V, Universität Mannheim, W-6800 Mannheim, Germany
[2] Interdisziplinäres Zentrum für Wissenschaftliches Rechnen, Universität Heidelberg, W-6900 Heidelberg, Germany

ABSTRACT

The Enable Machine is a systolic processor for 2nd level triggering for the TRD. It is under development within the EAST/RD-11 collaboration at CERN. The task of the processor is to identify electron tracks and to reject pion tracks in less than 10 μs. Track are identified by direct template matching in a region-of-interest (RoI) of the TRD. This is done by histogramming the coincidences of the mask templates and the RoI data for each track. Tracks of the same slope are handled in parallel, tracks of different slope in a pipeline. e/π discrimination is done according to the EAST benchmark algorithm. At an operational speed of 40 MHz the trigger decision time will be 6.5 μs and the latency 7.0 μs. The Enable Machine will be set up with programmable gate arrays so that it can be adapted easily to different applications. It is scalable in the RoI size as well as in the number of tracks processed concurrently. A prototype is scheduled for spring 1993.

1. Introduction

Systolic processors are SIMD (single instruction multiple data stream) machines which consist of a high number of identical processing elements (PEs) with nearest-neighbor connections. The PEs are controlled by a unit that issues the same command to all of them. Data are passed from one PE to a neighbor synchronously. Since all PEs are identical and relatively simple it is straightforward to set up large arrays of such PEs by CAD for an implementation in VLSI or programmable logic. Therefore systolic processors offer massive parallelism for relatively simple tasks. For this reason they are particularly well suited for second level triggering.

The Enable Machine is a systolic processor for the identification of particle tracks in the TRD detector of the LHC collider. It is under design within the EAST/RD-11 collaboration at CERN according to the EAST benchmark specifications[1]. The processor will be implemented in field programmable gate arrays. This implementation has been chosen since it provides high flexibility and reduces substantially the development time as demonstrated earlier[2,3]. The paper discusses the architecture of the Enable Machine, its performance, and its implementation.

2. Principle of Operation

To identify electron and pion tracks the Enable Machine is composed of three functional building blocks, two histogram generation units and a trigger decision unit (Fig. 1). The histo-

* This work has been performed within the EAST/RD-11 collaboration of CERN and has been supported by the Gesellschaft für Schwerionenforschung Darmstadt (GSI), Darmstadt, Germany.

gramming units are identical. In a (ϕ,z) region-of-interest (RoI) selected by a 1st level trigger one unit processes all detector hits ("total" data), the other only those above a threshold ("high" data). The trigger decision unit analyzes the contents of the histogram channels and does the electron/pion classification in programmable hardware.

Every column of the Enable Machine handles all tracks of a fixed slope, i.e., tracks of all possible offsets. The track pattern is stored in a local RAM. According to this track pattern the RoI data increment counters, one for every offset. Since the image is pipelined through the processor array two histogram results ("high" and "total") are computed in every step and can be analyzed in the trigger decision unit to derive the classification result. Since each histogram channel belongs to a track of a certain slope and offset the total number of tracks amounts to n×k (k = number of offsets in the RoI (=20), n = number of different slopes (=16 for one board of the prototyp)).

After histogramming the corresponding histogram channels are combined in the trigger decision unit to derive the classification result. The trigger decision unit has a maxfinder sub-unit that searches for the best defined track. The ratio of (number of "high" pixels)/(number of "total" pixels) for this track, computed by table look-up, is used for electron identification/pion rejection. The table look-up value is compared to a programmed threshold and a trigger signal is generated accordingly.

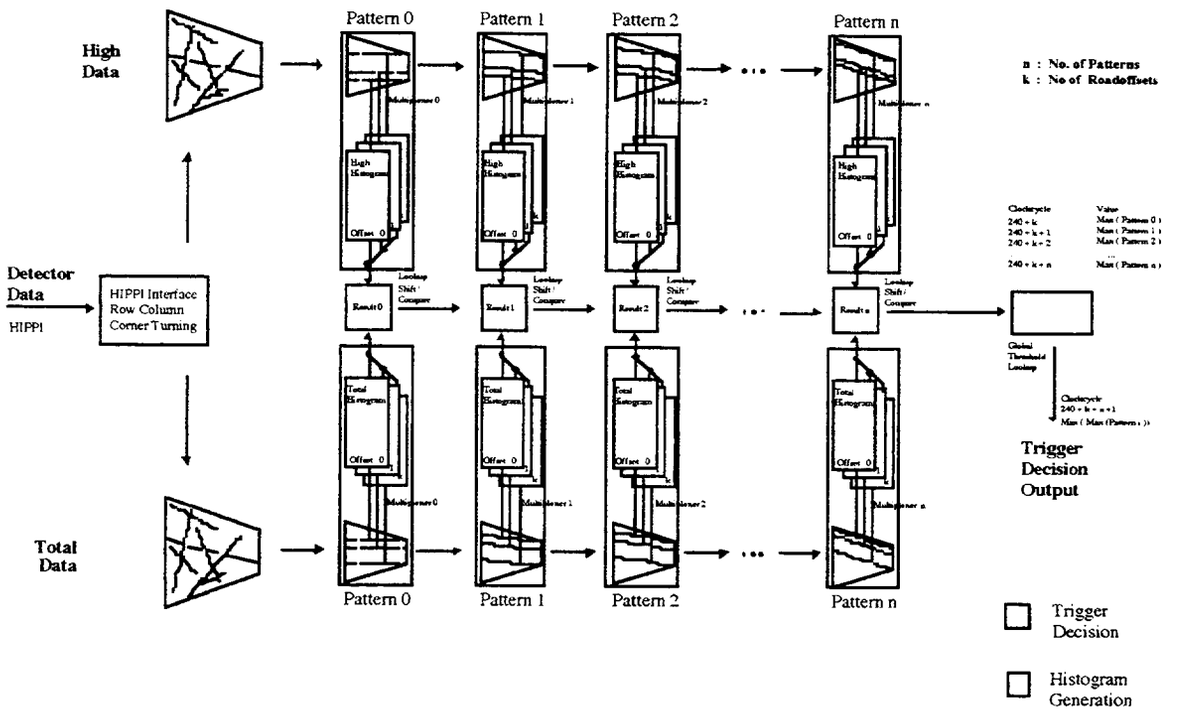

Fig. 1: Detailed layout of the Enable Machine

3. Performance

The speed of the Enable Machine is given in terms of trigger decision time and latency. For a synchronous architecture it depends only on the clock frequency. The latency is the time between entering the 1st column of the RoI into the processor and the output of the trigger decision, whereas the trigger decision time is the time between two successive trigger decisions.

Accordingly the trigger decision time is given by the time c needed to input the RoI into the processor, plus the time required to read out the histogram contents into the local max-finder logic which equals the number of track offsets k. Resetting of the histogram channels is done in a pipelined fashion. New data can therefore be shifted in as soon as the histogram contents of the 1st column have been shifted out. So the trigger decision time t is given by $t = c + k$ with c = RoI width in pixels (240), k = number of track offsets (20).

The latency is given by the time required to generate the histogram and to compute the electron/pion discrimination. It depends on the RoI width in pixels c, the number of different tracks n, and the number k of track offsets. So the latency is given by $z = c+n+k+1$ with n = number of patterns (=16 per board). The dominating term in this formula is the RoI width c that exceeds k and n by about one order of magnitude. Thus the performance of the Enable Machine is determined by the speed of the input data flow.

In the following table the trigger decision time and the latency are given for two clock frequencies of the processor. The estimate of the clock cycle time is due to macro specifications for the logic parts for the XC 400x series.

Clock frequency	Trigger decision time	Latency
40 MHz	6.5 μs	7.0 μs
50 MHz	5.2 μs	5.5 μs

4. Reprogramming of parameters

The architecture of the Enable Machine allows easily to adjust several critical parameters. It is possible to change the trigger algorithm by reprogramming the XILINX chips. In addition several functional elements of the machine are controlled by RAM look-up tables which gives a further degree of freedom. Within the RoI any track can be searched for. It is also possible to search for specific patterns along tracks or for curved tracks if this should be required for a different detector set-up. Additionally settable parameters are the threshold of the electron/pion ratio and the adopted maxfinding procedure. The trigger decision criterion can also be set by programming the look-up table in the appropriate way.

The architecture of the Enable Machine, i.e., its XILINX contents, and the contents of the look-up tables can be programmed from a host workstation via a VME interface. The configuration program for the XILINX chips, e.g., can be downloaded in a few milliseconds.

5. Implementation

As a first step of the implementation the EAST benchmark algorithm has been executed on a hardware simulator of the Enable Machine. All functional elements like accumulators and multiplexers have been defined in the simulation framework. A behavioral model with unit-delay assumption has been used. The data flow has been tested on a clock cycle basis. The hardware simulator assumes that all processing elements operate synchronously in a lock-step fashion. The data routing, locally performed between the columnwise arranged accumulator and multiplexer slices, has been simulated on the register-transfer level. RoI's of 240×80 pixels have been processed. The histogram generation can be traced and displayed step by step. The trigger decision unit has been simulated in the same way. Each column is read out sequentially and the local maximum is computed. Then the global maximum of all columns is searched. The entries of the corresponding "high" and "total" channels for this global maximum serve as a table look-up address that outputs the trigger decision. The simulation is in complete accordance with the off-line version of the EAST benchmark algorithm. It has shown the functionality of the Enable Machine in terms of electron/pion discrimination, latency, and speed.

The Enable Machine is currently being implemented in programmable gate arrays. The architectural studies have been completed and the final hardware scheme has been devised. Several possibilities for design optimization have been considered and integrated into the final design. One column of the histogramming unit has been mapped into a XILINX 4005 chip. Mapping of the trigger decision unit is in progress. Worst-case simulation studies indicate a clock cycle frequency of 40 MHz. A prototype which will serve as a test and evaluation board will be realized with modest cost and is scheduled for spring 1993.

References

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