

# CURRENT STATUS OF CONTROL SYSTEM FOR PLS 2-GeV LINAC

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## Abstract

The PLS 2-GeV electron linac at the Pohang Accelerator Laboratory (PAL) has been served as a full energy injector to the storage ring called the Pohang Light Source (PLS) since September 1994. The linac uses eleven 80-MW klystrons driven by 200-MW modulators. There are 42 constant gradient accelerating sections and 6 quadrupole triplets. A graphic-based real-time control system has been developed and used for the commissioning and the normal operation since 1994. The system has three layers of hierarchy; operator interface for machine control, device interface for data acquisition, and the supervisory layer which provides effective data processing and networking. After providing basic skeleton of machine control system, we added several features such as modulator control windows and RF signal display windows. Also, for beam diagnostics, beam loss monitors are added in the linac and the beam transport line. In this paper, we report the current status of the control system and upgrades during 1995-1996 period.

## Introduction

Pohang Accelerator Laboratory (PAL) has completed the 2-GeV synchrotron radiation source named Pohang Light Source (PLS) by the end of 1994 [1]. The PLS consists of a 2-GeV electron linear accelerator as a full energy injector and a 2-GeV storage ring. The PLS project was started from April 1988, and its construction was completed in December 1994. After the successful commissioning of the linac and the storage ring, the PLS has started its service as a low-emittance light source from September 1, 1995 for various research areas such as material science, surface physics, biology, and semiconductor applications using X-ray lithography.

When the PLS opened to the public service, there were only two beamlines; one for vacuum ultra-violet (VUV) application and one for X-ray application. However, by the end of August 1996, there are four more beamlines constructed; one NIM (normal incident monochromator) beamline, one XAFS beamline, one lithography beamline belong to the company named LG electronics, and one white beamline. The first undulator beamline will be ready in 1997. The number of beamlines will be increased drastically in next several years.

The 2-GeV linac employs 11 klystrons and modulators in the ground floor and 42 accelerating sections in the tunnel. Its overall length is 150-m and the average accelerating gradient is 15 ~ 20 MV/m. In order to achieve such a high accelerating gradient, 80-MW klystron and SLAC-type RF pulse compressor are used. There are also many magnet power supplies (MPS), vacuum monitors, and various beam diagnostics devices. The circumference of the storage ring is 280.56-m. The storage ring lattice is based on the triple-bend-achromat (TBA) with a 12-fold symmetry. There are 36 bending magnets, 144 quadrupoles, and 48 sextupoles. There are three re-entrant type RF cavities with 60-kW klystron per each cavity. In order to correct the beam orbit, there are 108 beam position monitors and corrector magnets around the storage ring. There is a 96-m long beam transport line (BTL) to connect the linac and the storage ring.

Even though the control systems of the linac and the storage ring are developed by different teams, there are three common factors. Each system has a three-level hierarchy structure and a VME-based system with OS-9 operating system. And all custom-made codes are written by C-language.

The linac control system includes the main linac and the whole beam transport line (BTL) except the Lambertson DC septum magnet which is located at the injection straight section of the storage ring. There are also two beam analyzing stations (BAS) to analyze the properties of electron beams up to 100-MeV and 2-GeV, respectively. The structure of control system was finalized by January 1993. At this stage, it was decided that we would use commercial products for all hardware such as CPU boards and I/O boards and concentrate our effort to develop necessary software with the help of commercial development toolkit named RTworks. Before starting the major work, we made the signal list and the design manual for the linac control system [2,3]. The actual S/W development started from May, 1993, and the initial phase of the control system was completed by the end of June, 1994. It played an important role during the commissioning of the 2-GeV linac which started at the beginning of January, 1994.

At present, the linac control system provides a reliable function in daily operations [4]. However, it is obvious that the linac control system is continuously being upgraded based on operational experiences and diagnostic equipment added.

## Hierarchy of Linac Control System

Our aim for the linac control system is to provide a reliable, fast-acting, distributed real-time system. There are three layers in the control hierarchy; operator interface layer, data process layer, and data acquisition layer. Last two layers are based on the VME realtime system. There are also three subsystems divided into their own functional characteristics; modulators and microwave system (MK), magnet power supplies (MG), and beam diagnostic (BM) subsystems. Several special systems are connected directly to the data process layer. These layers are linked with four independent ethernet.

### Device Interface Computer (DIC)

This layer is directly connected to the individual devices to be controlled or monitored. The local computer connected to the individual devices is called the device interface computer (DIC). There are eleven units for the modulator and microwave control systems (MK), three units for magnet power supplies (MG). There are also two units of beam profile monitors and other diagnostic equipment in the linac and the BTL. All DICs are located in the klystron gallery.

Each DIC is consisted of an ELTEC E-16 CPU board, a 14" EGA graphic monitor, a draw-type keyboard, and several I/O boards mounted on the standard 19" rack. The E-16 board includes a Motorola 68030 CPU, 4 MDRAM, an EGA compatible video port, and an ethernet port. There is an extra memory board with 4 MDRAM in each DIC. All of the I/O boards used in the VME system are commercially available. The operating system is OS-9 with the MGR graphic development tool. On-demand local computer control is available to all DICs. This feature is extremely useful for the local commissioning and testing of an individual device, especially 200-MW modulators. Each modulator is now controlled by its own DIC such as the self-recovery from various dynamic interlocks.

### Supervisory Control Computer (SCC)

In order to avoid heavy work loads on the main computer, we divide the linac control system into three subsystems; modulators and microwave system (MK), magnet power supplies (MG), and beam diagnostics (BM). The role of SCCs is an intermediate data manager for the assigned subsystem. Thus, there are three units assigned to their own functions.

Each SCC unit consists of an ELTEC E-7 CPU board, a 19" monitor mounted on the sub-control console, a 3.5" floppy disk, a 900-MB hard disk, and a streaming tape backup system. The E-7 board has a Motorola 68040 CPU, 16 MDRAM, a workstation graphic board. And there are

two ethernet ports in each SCC; one for the data acquisition layer and one for the operator interface layer.

All SCCs are installed in one standard 19" rack in the sub-control room which locates next to the main control room only separated by large glass windows.

Three more such units are installed in another standard rack in the same room. Even though the major role of these extra units is to develop the system software without disturbing the main control system, these can provide backup functions for the main SCCs in case of troubles.

### Operator Interface Computer (OIC)

This is the main computer for the PLS linac control system. The OICs are actually one SUN-4 sparcstation and two X-terminals connected to this SUN workstation. They are located on the main console. A duplicated system is placed in the sub-control room. This is the backup system which is normally used for the development work along with backup SCCs. The operating system is UNIX, and RTworks is intensively used to optimize graphics and data handling between the UNIX system and the OS-9 system.

There is one more SUN-4 workstation in the main control room for physics-related researches. Accelerator physicists can develop various simulation codes and apply their results to real operations later.

### Software

In parallel with the hardware structure, we use three layers in the S/W structure. Subsystems such as MK, MG, and BM are monitored and controlled by an individual task running on the appropriate layer. There are two important features in the linac control S/W; the client/server routines to exchange data and commands between layers, and the separation of monitor/control tasks. When the operator selects a command from an appropriate window, it sends down to the designated device via control client/server routines in the realtime system. The data collected by a given command returns to the operator's window through a separate route. The communication between layers is made by TCP/IP protocol.

### Data Acquisition Layer

The major roles of the data acquisition task in DICs are as following; to store monitored data from individual devices to the designated buffer (`m_buffer`) regularly, and to send updated data to the SCC upon request. For the control command from the SCC, the corresponding control task sends data or messages to control individual device in realtime through proper I/O ports. Other important roles of the data acquisition task are to monitor any malfunction of

connected devices and to provide emergency cures if possible, and to report the status to the SCC.

### Data Processing Layer

The major role of the data process task is to collect the updated data from attached DICs and to store them in the realtime database. These data are sent to the RTdaq running on the OIC upon requests made by the operator. Also a corresponding task sends control commands to the proper DIC in realtime. All the required application software are running in realtime in this layer including client/server routines for the ethernet communications. Every data in the linac operation are stored in the RAM area temporarily and hard/floppy disk for permanent records.

### Operator Interface Layer

A commercial S/W package named RTworks is used to develop graphic-based operator interfaces. The RTworks is actually an integrated development toolkit for an optimum data handling between client/server systems. Using this toolkit, it is possible for one S/W engineer to develop all required operator interfaces for the linac control in a year.

The data received in the RTdaq from realtime CPUs are sent to the RTserver by inter-processing communications, and they are displayed in the monitoring windows by RThci routine. A command selected by a mouse action drawn by an operator is sent to the SCC through user defined processes.

There are several windows for operators to control and monitor individual system such as MPS, bunchers, IPAs (isolator, phase shifter, and attenuator to provide best microwave condition to electron beams), and modulators. Each window has a value display area and a control sub-window. All the control action can be made by selecting areas with a mouse or select items from pull-down menus. The main control window includes the status of 11 modulators and phase angles for IPAs. Subsystems such as magnet control and monitoring windows can be started by selecting proper commands from the pull-down menu.

### Upgraded Features and Future Plans

As of the end of June 1994, most of the linac control system was completed [5]. It has been used for the commissioning to obtain 2-GeV beams and for the routine operations to provide beams to the storage ring being commissioned in 1995. Since then, there have been several features added in the linac control system.

During the summer maintenance period in 1995, a feature of the automatic report generation was added in the linac control system. So, duty operators can report activities

carried out during their duty period. This report includes various setting values of magnet power supplies and phase angles and amplitudes of IPAs.

In April 1996, the control subsystem for beam loss monitors (BLM) were completed. Now, the BLM signals from 42 detectors in the linac and 11 detectors in the BTL are displayed in the main control window.

Signals from beam current monitors are about to ready to display in the main console. This work involves a fast signal processing due to the 1-ns pulse duration of the electron beam. At present, necessary electronics including fast sample/hold circuits for BCM are completed. Full tests of BCM electronics and data acquisition routines was also carried out in June 1996. However, due to the huge amount of digitized data coming from 13 BCMs, the current OIC is not adequate to handle these data properly. Thus, the main computer of OIC is required to upgrade to faster and larger one. This upgrade will be done in next year.

The timing system will be incorporated to the main control system after completing the optical communication circuit between the individual time delay unit located at the sub-control room and the corresponding modulator in the klystron gallery. At present, new optical network is installed but not tested yet. New timing system will be tested in 1997. There will also be a new e-gun control system.

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### References

1. "Design Report of Pohang Light Source (revised ed.)," Pohang Accelerator Laboratory, 1992.
2. I. S. Ko and W. Namkung, "Signal List for 2-GeV Linac," MA/LN-93001, Pohang Accelerator Laboratory, 1993.
3. I. S. Ko, J. H. Kim, S. C. Kim, J. M. Kim, G. S. Lee, and W. Namkung, "Design Manual for PLS Linac Control System," MA/LN-93002, Pohang Accelerator Laboratory, 1993.
4. I. S. Ko, M. H. Cho, J. S. Bak, J. Choi, H. S. Lee, and W. Namkung, "Operational Status of PLS 2-GeV Electron Linac," these proceedings.
5. I. S. Ko, J. H. Kim, J. Choi, and W. Namkung, "Control System of PLS 2-GeV Electron Linac," IEEE Trans. Nucl. & Sci., 43, 1, p25 (1996).