DEVELOPMENTS IN THE HIGH PRECISION CONTROL OF MAGNET CURRENTS FOR LHC

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Abstract

The LHC will require over 1700 magnet power converters, some of which will need an unprecedented precision of about 1 ppm (of 13 kA). This paper presents the approach taken, prototype methods, initial results and charts future design directions. These results confirm that such performance can be obtained reliably and at a reduced cost compared to conventional methods. Developments of a real-time controls infrastructure needed to support on-line beam feedback are outlined.

1 BACKGROUND

For the LHC machine to achieve its full potential, the power converter system needs to attain a peak performance of about 1 part per million (ppm) in terms of resolution, stability and reproducibility. This represents an improvement over current practice of approximately a factor of ten. In addition, the very large electrical time constants presented by super-conducting magnets, coupled with the need to remove dynamic errors required a new approach. In order to meet this challenge a number of studies and practical tests have taken place over the last few years aimed at proving that such increased performance can be obtained reliably. A strategy for obtaining such improvement was presented in an earlier paper [1]. In brief this strategy was :

- Employ digital regulation methods rather than analogue methods.
- Apply digital corrections of known errors.
- Employ real-time feedback mechanisms (both magnetic and beam related).
- Incorporate in-situ calibration techniques (this subject is not covered further in this paper).

This approach required an extensive revision of present practice for the regulation and remote control. This paper presents the design of the prototype system, the results obtained and outlines future design directions.

2 PROTOTYPE IMPLEMENTATION

The digital regulation hardware, shown in figure 1, has been built using a commercial digital signal processor (DSP) card as the heart of the system. This processor, a Texas TMS320C32, 32 bit floating-point device computes the current reference value every milli-second,

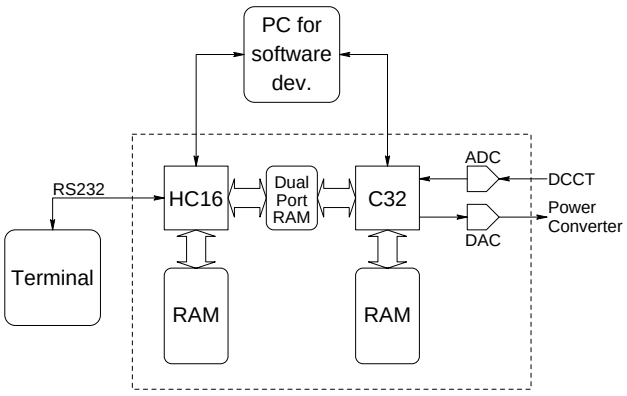

Figure 1: Prototype Hardware.

compares this to the actual measured current and then computes, using a regulation algorithm, the required signal to drive the power converter to the correct value. This signal is converted into analogue form via a digital to analogue converter (DAC). The output current is measured by a purpose designed, Sigma-Delta, analogue to digital converter (ADC), which has better than ±1 ppm performance and is directly interfaced to the DSP. The interface between the DSP, the remote control system and the power converter hardware is provided by a second commercial micro-controller card. This card employs a Motorola MC68HC16Z1 which acts as the 'master' for the DSP.

The software for both processors is written in 'C', using commercial software development tools. Only minor use of assembly language has proven necessary. Both systems employ 'direct to processor' connections to the PC (BDI and JTAG), allowing code down-load and extensive debug capabilities. The reference and regulation algorithms operate as a single repetitive task in the C32 while a simple command monitor running in the HC16 and using a terminal as input, replaces the remote control functionality. For the moment, no real-time operating system is employed but this will be incorporated in the next generation.

In order to evaluate the power converter performance under digital regulation, an independent measurement system has been set up. This uses a high precision HP3458 DVM to measure the current, and also captures data directly from the DSP every millisecond via a FIFO buffer. Display and analysis software is based on MATLAB, which is also used to study and simulate the entire regulation system, allowing theoretical and practical results to be compared.

3 CONTROL ALGORITHM DEVELOPMENT

The control algorithm for the power converter regulation is a key element in determining the overall performance. Two methods have been incorporated and are under detailed investigation. They aim to provide the necessary accuracy, resolution and dynamic performance. The first method is a digital realisation of standard analogue techniques employing proportional-integral-integral (PII) plus feed-forward. The second method employs a more modern approach, namely RST. Both methods have been tested in simulation and have proven to give more than adequate performance for LHC. The PII algorithm has been implemented fully and tested extensively with real power converters and magnet loads. A number of practical problems had to be solved, including start-up conditions and loop saturation. Tests have also been successfully conducted on adaptive algorithms but they are probably not necessary. Both algorithms are deceptively simple in code terms, but do require some attention with the mathematical errors due to the single precision maths of the DSP.

4 REFERENCE GENERATION

The generation of an accurate and smooth acceleration waveform is essential for the successful operation of LHC. The preferred form for the main magnetic elements is explained in another contribution to this conference [2]. The control algorithm requires the precise value of this waveform to be evaluated every loop iteration (1ms). A number of possibilities for implementing this complex waveform exist and have been studied in some detail.

Initial tests were performed using a linear ramp function and subsequently the addition of parabolic start and stop regions. This enabled most evaluations of control loop performance to be made easily. More recent work has aimed at numerical methods, employing quadratic or cubic spline fits, and in this area a number studies have indicated the potential of such methods to reduce the amount of data defining the desired waveform. Such reductions are desirable to reduce the network data flow. The direct application of correction multipliers at 100 Hz to the desired reference waveform has been demonstrated successfully in recent tests on the SPS machine

Latterly, a mathematical model of the preferred LHC waveform has been implemented directly in the DSP. This has allowed a number of interesting tests to be performed and will be of value for subsequent magnetic measurements. However, apart from test purposes, such methods are unlikely to be used for the LHC.

5 PROTOTYPE RESULTS

The results which are presented below are only the latest from a long series of measurements. Tests with simulated loads and model power converters have recently been complemented with full-scale tests on power converters up to 20 kA and with a variety of loads with time-constants ranging from 40 ms to 100 s. Final tests can only be made with the 23,000 s load of the actual LHC machine. Figure 2 illustrates low frequency noise and current steps of 1 ppm. Figure 3 shows a 'short' LHC acceleration curve (up to 5 kA). The form of the ramp was computed in real-time from segment equations. The segments were: (i) parabolic acceleration, (ii) exponential acceleration, (iii) linear ramp, (iv) parabolic deceleration. Figure 4 shows the first six seconds of the ramp in more detail, illustrating the excellent resolution and accuracy of the system. Good control at the start of the ramp is particularly important as the beam is then at its most vulnerable to errors. Analysis of the end of the ramp shows equally good behaviour with no overshoot. Finally, the long term stability of the controller is illustrated in figure 5. The linearity of the system is entirely dependent on that of the ADC (±1 ppm) and current transducer (DCCT), both of which are presently undergoing validation tests.

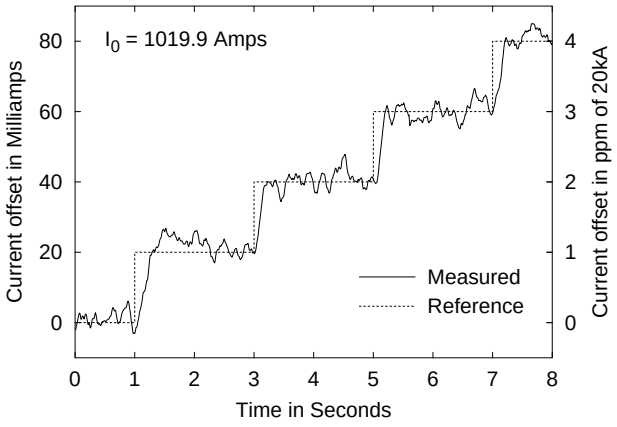

Figure 2: 1 ppm Current Steps.

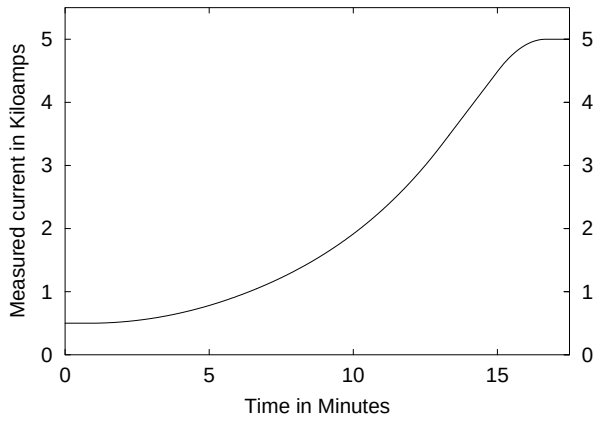

Figure 3: Short LHC Ramp.

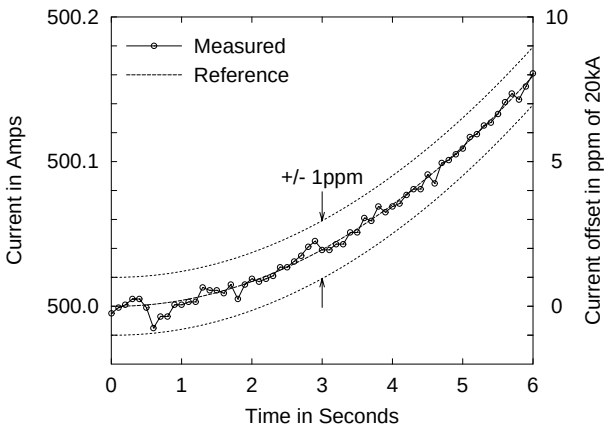

Figure 4: The start of the short LHC ramp.

6 DEVELOPMENT WORK

In order to progress further towards a final system design a number of important steps have been taken recently. The first is the development of a cheaper ADC for the majority of circuits which have less demanding requirements. The second is the completion of a single card design which brings together all of the essential components mentioned earlier. Extensive use has been made of field programmable gate arrays (FPGA's) and a novel serial digital/analogue input system has been developed for power converter surveillance.

A very important third development has occurred recently with the adoption of the WorldFIP field bus as the link between the digital controller card and the LHC accelerator network. This field bus has a number of specific characteristics, among which, its deterministic performance is paramount. This feature enables the WorldFIP to transport reliably the online, 100 Hz, closed-loop correction data around the LHC, while also doubling as a simple transport mechanism for the required machine synchronisation and timing. This results in a considerable cost saving while enhancing reliability due to component reduction. Status and measurement data can equally be up-loaded to the control room at 100 Hz.

Parallel developments in the overall controls network should allow extensive use of real-time control across the entire system. Code down-load and diagnostics up-load also enhances system flexibility and accelerator performance.

7 CONCLUSIONS

The results of the prototype work which have been presented, validate the overall strategy adopted earlier. The performance improvements are such that power converters can now be designed with all major errors reduced to the ppm level. This has been achieved along with an overall reduction in costs. The methods are applicable to a very wide range of power converter loads, ranging from several tens of milliseconds to more than ten thousand seconds. Moreover, on-line feedback can be incorporated at essentially zero cost, while the design realisation allows hardware and software refinement to continue up to and beyond the putting into service of the equipment. Overall system validation remains to be done however, along with an industrialisation process for series manufacture.

8 ACKNOWLEDGEMENTS

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9 REFERENCES

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[2] P.Burla et al. CERN, “Optimisation of the Current Ramp for the Main LHC Circuits”, PAC’99 NY contribution.

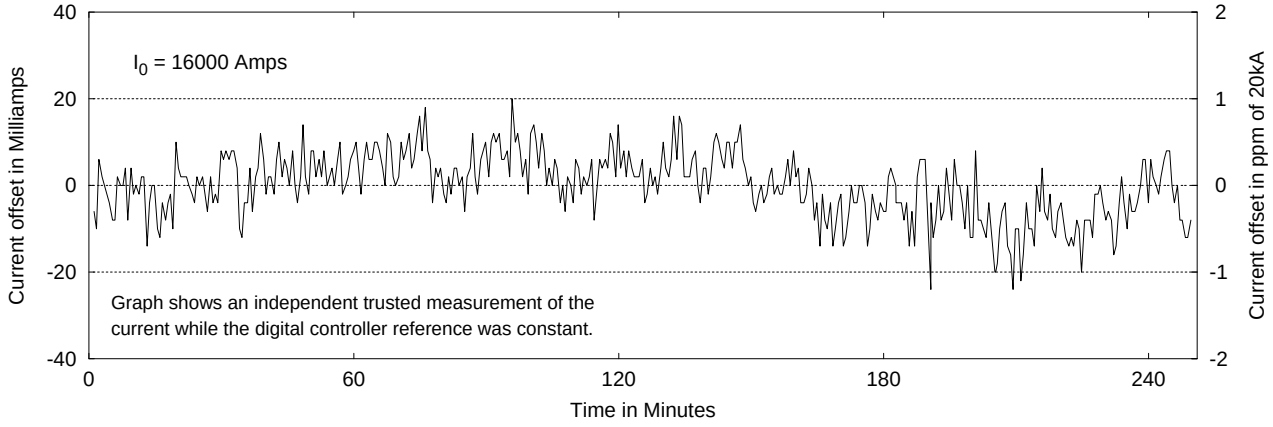

Figure 5: Stability over Time.