Radiation-hard Bipolar and CMOS Front-end Electronics

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The Leading Proton Spectrometer (LPS) in ZEUS at HERA consists of planes of silicon detectors close to the beamline in the forward proton direction (the first plane is 20 m from the interaction point). The front-end electronics for the system must respond to the following design constraints:

- 100 μm pitch (to match detector)
- high speed operation at HERA (10.4 MHz collision frequency)
- data storage during LEVEL 1 trigger decision (5μs)
- data storage during LEVEL 2 trigger decision ($> 100\mu$s)
- high radiation exposure
- low power consumption.

To respond to these needs it was decided to build a digital system. The first stage of electronics is an amplifier and comparator, built in bipolar technology for low noise. The digital stage of electronics, built using 1.2 μm CMOS technology for low power consumption, is a buffer system to allow data storage during trigger decisions. Both stages have been designed and are in the prototyping phase. We report here studies of radiation hardness of components.

The design of the Analog Amplifier Comparator Chip (AACC) has been previously discussed [1]. The amplifier has a peaking time of 20 nsec for pulses from silicon-strip detectors and the power consumption is estimated at 1.6 mW/channel. The comparator threshold can be set as low as 30% of the pulse due to minimum-ionizing particles. The equivalent noise charge is 700 electrons. The design is being fabricated using Dielectric Isolated (DI) bipolar technology and components produced by this process were irradiated to determine their performance. The transistors were exposed to 1 MeV neutrons produced in a beam

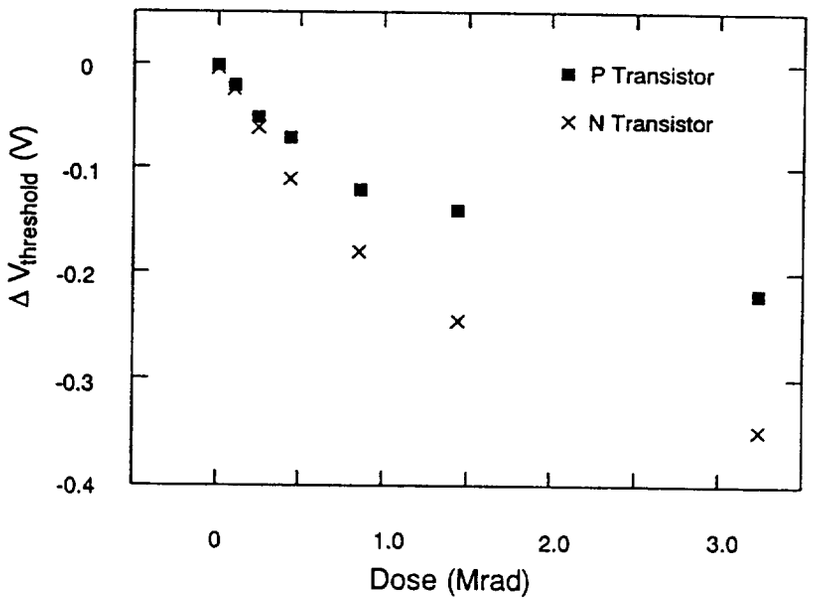

Figure 1: Variation of threshold voltage as a function of photon dose.

dump at LAMPF. The transistor β decreased by approximately 12% after a dose of 5×10^{13} n/cm^2. Transistors were also exposed to 500 and 800 MeV protons up to a flux of 7×10^{14} protons/cm^2 at LAMPF. The dose was approximately 25 Mrad(Si) and is much larger than the estimated dose for the LPS. In this case the β decreased from 85 to 35. Although a significant decrease, it should be possible to operate the chip at these levels.

The design of the Digital Time Slice Chip (DTSC) has been described in reference 2. The first buffer is a 64-stage shift register which stores the data during the LEVEL 1 trigger decision. If a LEVEL 1 valid signal is received then the data is written into a 32-word queue to wait for LEVEL 2. A test version of the chip has been manufactured in a radiation-hard 1.2 μm CMOS process by UTMC[3]. Included on the wafer were some test structures which have been irradiated with photons from a ^{60}Co source at UC Santa Cruz. For both p- and n-transistors, the shift in threshold voltage was measured as a function of dose. The results are shown in Figure 1 and are less than 0.4V for approximately 3 Mrad dose (the operating voltage is 1 V). The test structures also included combinations of transistors to produce inverter and NAND circuits. These were also irradiated and show even smaller shifts as the changes in the p- and n-transistors compensate. After the performance of other structures is evaluated, they will also undergo radiation tests.

We have a design and are working on prototypes for the analog and digital stages of a front-end system for the Leading Proton Spectrometer. We have performed irradiation studies on transistor components produced using radiation-hard bipolar and CMOS technologies. Exposure to 5×10^{13} n/cm^2 of 1 MeV neutrons caused the bipolar transistor current gain, β, to decrease by approximately 12%. The decrease due to 7×10^{14} p/cm^2 was more severe, but still tolerable. The CMOS transisitors and logic circuits showed small changes in threshold voltage ($< 40\%$ of the operating voltage) after exposure to 3 Mrad(Si) of ^{60}Co photons. Our future work includes the irradiation of the functional chips when available with neutrons and photons.

References

1. D. E. Dorfan, NIMA**279** (1989) 186.

2. J. DeWitt, NIMA**288** (1990) 209.

3. United Technologies Microelectronics Center, Boulder CO.