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THE NA48 LKr CALORIMETER DIGITIZER ELECTRONICS CHAIN

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Abstract

The 13 500 channels of the NA48 liquid-krypton electromagnetic calorimeter readout electronics were put into operation in 1997. The digitizer electronics employs a new gain switching technique that expands the dynamic range of a standard 10-bit ADC to 14 bits at 40 MHz sampling rate employing a custom-developed integrated circuit (KRYPTON). The KRYPTON has been fabricated in 1.2 μm BiCMOS technology and was successfully developed together with industry on a short timescale. The performance and the experience from the first year of the operation of the liquid-krypton calorimeter electronics will also be briefly discussed.

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1 Introduction

The NA48 liquid-krypton calorimeter [1], [2] uses the initial current readout method to obtain an energy resolution of 3.5% $\sqrt{E}$ and a constant term of 0.5% together with an excellent position and time resolution. This level of performance puts very stringent demands on the electronics including a 40 MHz ADC with a dynamic range of 14 bits. In order to have short connections and fast response, the charge preamplifiers are placed inside the calorimeter. The output signals of the preamplifiers are transmitted to low-noise transceivers, located close to the feed-throughs outside the calorimeter. The signals from the transceivers are sent to the shaper and ADC digitizers in the electronics racks 10 metres away. Figure 1 shows a block diagram of the readout chain with the relevant signal waveforms. A more detailed description of the front-end electronics is found in Ref. [3].

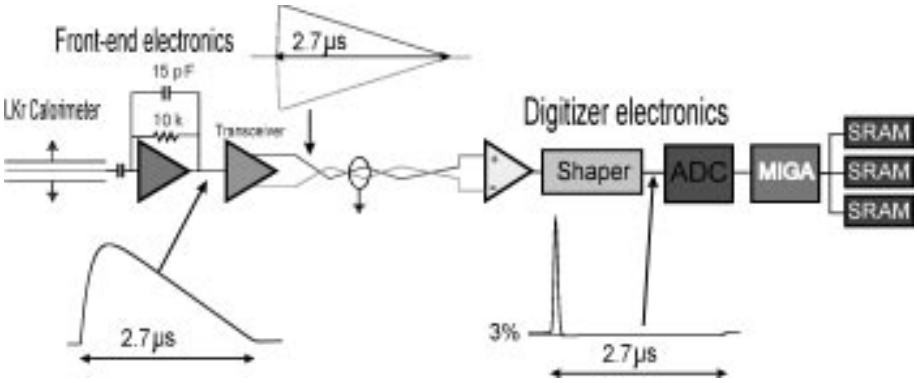

Figure 1: Signals at various parts of the LKr electronics.

1.1 Digitizer electronics

The shaper filters the transceiver signal to an approximately Gaussian-shaped signal with 72 ns FWHM. As seen from Fig. 1, there is a 3% negative undershoot which lasts for a time equal to the drift time of the electrons across the calorimeter cell. The whole waveform is digitized and stored temporarily in a digital memory. Sufficient information is contained in a few samples around the peak of the signal and up to 16 samples are read out from the digitizer memory and used in the analysis. Up to 255 samples can be read in a special mode. The digitizer electronics consists of a shaper, ADC, interface circuits, and memory. The name chosen for the NA48 liquid-krypton calorimeter digitizer is the Calorimeter Pipeline Digitizer (CPD).

At the time of the design in 1994, only a few low-cost 10-bit ADCs at 40-Msample/s were commercially available, although since then, 12-bit ADCs have become available [4]. Therefore, we have implemented a method of dynamic range expansion (dynamic gain switching) which expands the dynamic range of an ADC with four bits in four gain ranges, while maintaining the resolution of the ADC [5]. For this purpose the NA48 experiment has developed a fully customized mixed analog/digital BiCMOS ASIC, which is named KRYPTON. In addition to gain switching, the KRYPTON does analog filtering and trigger signal processing. The high rate (1 MHz) of incident particles requires a digital readout without deadtime. This is implemented as a digital pipeline with a storage

length of 200 μs and an 8k-word readout buffer memory per channel. A digital gate array called MIGA is an essential part of this. It provides intermediate storage and handles the interface between the ADC, the static RAM of 16k $\times$ 24 bits, and the readout bus.

2 Analog signal processing

The signal from the transceiver is first differentiated with a time constant of 20 ns by a passive network before it is fed to the input amplifier of the KRYPTON. In this way low-frequency pickup noise from the front-end electronics on the calorimeter and the cable is rejected. In addition, the requirements on dynamic range on the KRYPTON and also the differential non-linearity are reduced by almost a factor 2. The input amplifier consists of one line receiver with three op-amps in a classic instrumentation amplifier configuration [6]. The amplifiers can be enabled and disabled via a serial control interface. The common mode rejection of the line receiver is better than 40 dB up to a frequency of 20 MHz.

The output signal of the line receiver is fed to both the Bessel filter and the three discriminators for the gain switching logic. This is shown in Fig. 2 for a typical detector signal. It has a risetime of 25 ns and width (FWHM = 40 ns) for a typical detector signal. The Bessel filter implemented combines the requirements of low noise with a very good timing resolution at high rates. The design is based on the results from several prototype tests in an electron beam. A fast shaping which results in a signal with a FWHM of 72 ns was finally implemented, see Fig. 2. This was optimized with Pspice simulations to have the symmetrical transient response using 1% standard components. The filter consists of three Sallen-Key stages with nine poles. The –3 dB bandwidth of the filter is 8.5 MHz. Since the sampling frequency of the ADC is 40 MHz, the Nyquist criterion is fulfilled with a margin of 2.5. This oversampling is beneficial in two ways: firstly, it improves the resolution of the ADC because of the increased statistics and secondly it permits error recovery in case of lost or mismeasured samples. Digital signal processing is applied in the off-line processing for this reason [7].

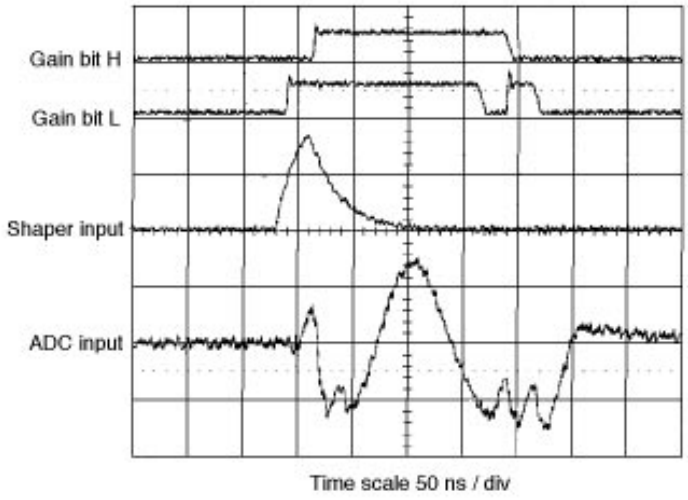

Figure 2: Digital gain bits, signal at the Bessel filter input, and analog input at the ADC for a step input signal.

The gain switching stage uses a passive attenuation network to set four gain ranges. Four channels of identical amplifiers with a total gain of 16 are designed with two cascaded gains of four amplifiers. This method minimizes bandwidth and delay spread between the four gain ranges. The gain ratios have been chosen to match the desired calorimeter resolution. The decision of which gain range to use is made by three discriminators with different thresholds. The Bessel filter provides a delay time of at least 60 ns, see Fig. 2, so that there is sufficient time for the discriminators and logic circuits to settle. The decoded state of the three discriminators called gain bit H and gain bit L is recorded together with the ADC bits at each clock cycle. A chosen gain setting is kept for six to eight samples. The number of samples is programmable. In this way all the samples of a pulse are measured using the same amplifier chain and the calibration is simplified. During calibration of the detector, it is possible to force the gain settings with the help of the serial control circuit.

2.1 Block diagram of KRYPTON

Figure 3 shows the block diagram of the KRYPTON ASIC. The complexity of the KRYPTON circuit can be illustrated by the number of components it contains: 21 high frequency op-amps, 6 fast comparators, 3 monostables, one fast multiplexor and various ECL, CMOS logic circuits. Additional functions integrated on the chip are a programmable trigger circuit for the NA48 neutral trigger and serial control circuits. Also shown are some of the external components needed: the input differentiating network, the Bessel filter components, and external npn transistors.

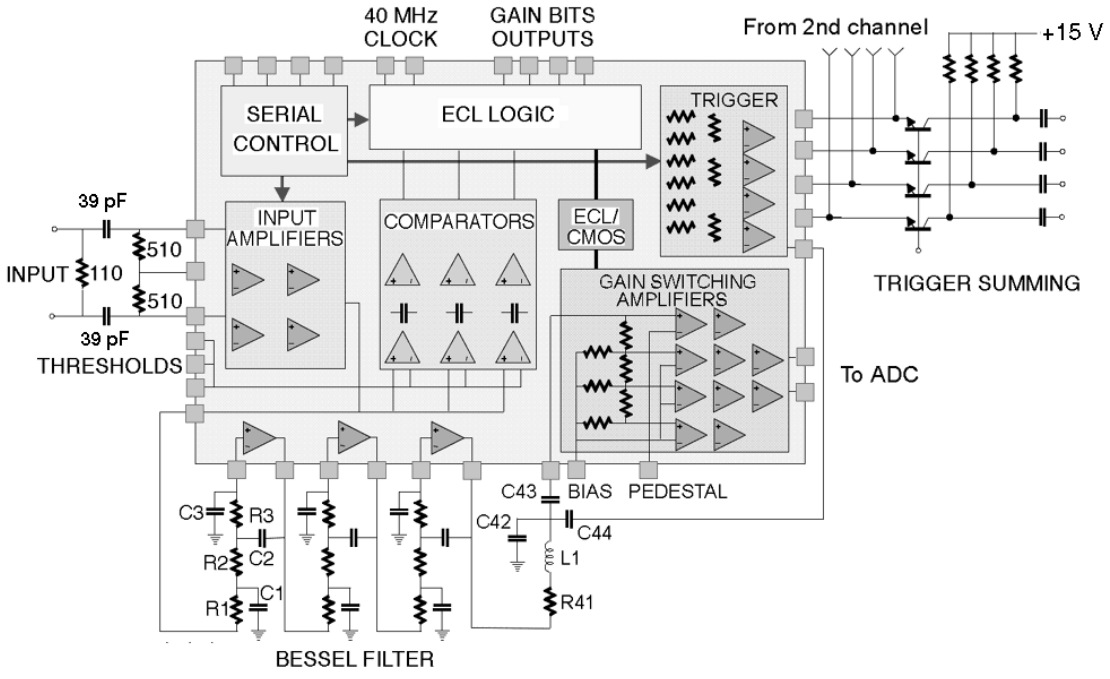

Figure 3: Block diagram of the KRYPTON ASIC with external components.

2.2 Design and development

The design of the KRYPTON ASIC was done in collaboration with CISS [8] and AMS [9]. The KRYPTON is based on a discrete component prototype. It was designed in six weeks. The KRYPTON is implemented in a 1.2 μm BiCMOS process from AMS [8] with npn transistors with a $f_t = 8$ GHz. The same op-amp is used with minor variations in 21 different blocks throughout the ASIC. As the performance of the KRYPTON is entirely determined by this circuit, it is described in more detail. The amplifier is a classical differential amplifier with an emitter follower output stage, see Fig. 4. Bipolar

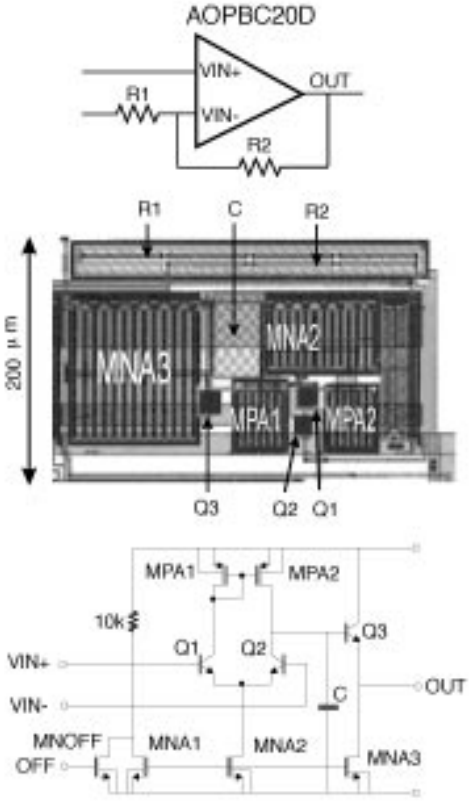

Figure 4: Block diagram, layout and schematic of the op-amp.

npn transistors Q1, Q2, and Q3 are used as active elements owing to their better performance in noise and speed. However, PMOS transistors are used in the current mirror because of the lack of suitable pnp transistors in the process used. The size of a bipolar transistor is a few per cent of that of CMOS transistors for the same current. The main difference between the 21 amplifiers is in the pull-down current (1 to 3 mA) in MNA3 and the compensation capacitor C (1 to 3 pF). The DC gain of the op-amps for the amplifiers used in the Bessel filter is 1.33 with output swing out from 1 to 3.5 V for an integral linearity better than 0.02% of full scale. The open-loop gain is 56 dB with –3 dB at 1 MHz. At a closed loop gain of 1.33 the bandwidth is 430 MHz. The input noise density of the op-amp is about 4 nV/$\sqrt{\text{Hz}}$.

The layout of the complete chip is shown in Fig. 5. The digital circuits are located in the upper part of the diagram. As seen in the diagram, a careful separation of the analog and digital circuits is implemented. The first prototypes were delivered after 10 weeks. With the exception of a logic inversion for the gain multiplexing, the chip was working correctly. The detailed measurements on the first prototypes resulted in a number of improvements: differential PECL logic levels for the logic gain bits instead of CMOS levels for reduced crosstalk; improved compensation of the op-amp to reduce the risk of parasitic oscillations; and improvements of the monostable in the threshold comparators. The total development time of the KRYPTON was one year with one iteration.

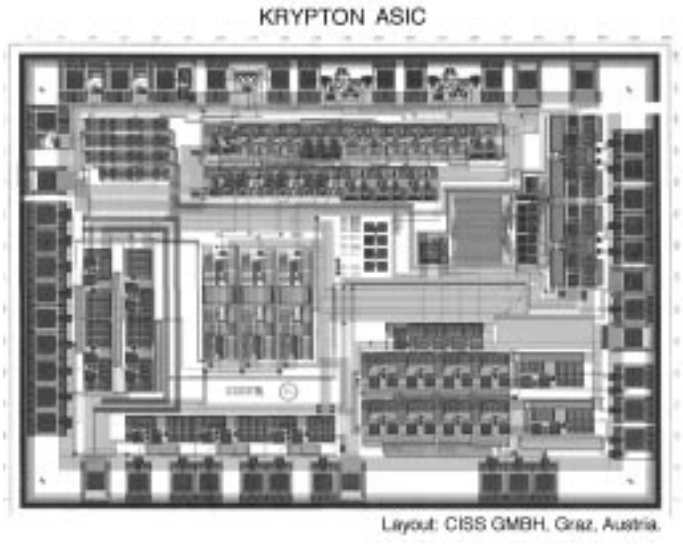

Figure 5: Layout of the KRYPTON ASIC. The size is 2.4 × 3.4 mm.

2.3 Measurements on the KRYPTON

The production test of the KRYPTON ASIC was made with a test board which simulated the actual shaper application. This test was made at the AMS test laboratories using automatic test equipment and large statistics. An example of the results is shown in Tables 1, 2, and 3. Two resistors determine the gain of the Bessel filter stages. Table 1 shows that the ratio matching of two resistors is 0.17% in this process. The gain of the input amplifier is determined by seven resistors and the total spread is 0.42%.

Table 1
Measured DC gain of KRYPTON

Function	DC gain
Input differential amplifier	1.662 ± 0.42%
Bessel filter amplifiers	1.331 ± 0.17%
Switching amplifier gain 0	15.53 ± 0.71%
Switching amplifier gain 1	5.381 ± 0.82%
Switching amplifier gain 2	2.202 ± 1.0%
Switching amplifier gain 3	0.88 ± 1.8%

Table 2
Measurements of the propagation delay of amplifier blocks

Function	Delay
Input differential amplifier	3.85 ± 0.10 ns
Bessel filter	66.52 ± 0.25 ns
Krypton positive output	82.04 ± 0.29 ns
Krypton negative output	82.72 ± 0.27 ns

Table 3
Measurements of the comparators

Comparator	DC threshold	DC hysteresis
1	9.88 ± 1.34 mV	0.18 ± 1.12 mV
2	191.9 ± 1.3 mV	1.28 ± 1.32 mV
3	789.2 ± 1.4 mV	0.61 ± 0.89 mV

The delay spread of the channels caused by the KRYPTON is about 300 ps as seen in Table 2.

The precision of the comparators is about 1 mV as shown in Table 3.

3 Implementation and performance

The printed circuit board of the CPD analog subcard is shown in Fig. 6. It contains

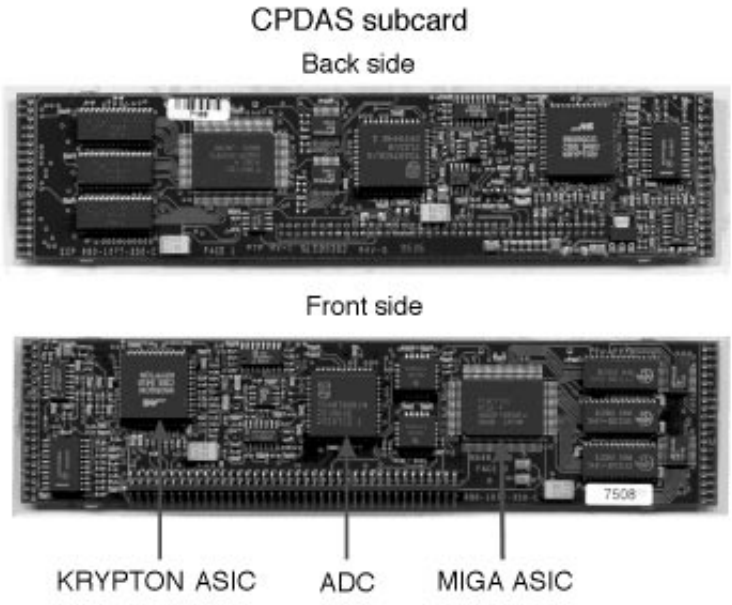

Figure 6: CPDAS analog subcard.

two channels, one on each side of the board. The main problem encountered was the coherent noise, which occurred due to crosstalk from fast digital signals. Careful design of the

printed circuit board and extensive testing solved this problem and the mass production of the 13 500 digitizer channels was started during 1996. The reliability of the system has been excellent during the first year of operation in 1997. The overall non-coherent noise achieved is 10 MeV/channel and the coherent noise is on average 0.54 MeV/channel. The time resolution is better than 100 ps for the electronics chain alone.

Acknowledgments

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