

DD

LAL/RT 97-09  
December 1997

# Laboratoire de l'Accélérateur Linéaire

## BaBar DIRC Electronics Front-End Chain

**C. Beigbeder, R. Bernier, D. Breton, T. Caceres, R. Chase, A. Ducorps,  
A. Hrisoho, P. Imbert, S. Sen, K. Truong, V. Tocut, G. Wormser and F. Zomer.**

Laboratoire de L'Accélérateur Linéaire  
*IN2P3-CNRS et Université de Paris-Sud, F-91405 Orsay*

**G. Bonneaud, F. Dohou, F. Gastaldi, P. Matricon, C. Renard, C. Thiebaut,  
G. Vasileiadis and M. Verderi**

Laboratoire de Physique Nucléaire et Hautes Energies,  
*Ecole Polytechnique, CNRS-IN2P3, F-91128 Palaiseau*

**P. Bailly, J. Chauveau, L. Del Buono, J.F. Genat, H. Lebbolo,  
L. Roos and B. Zhang.**

Laboratoire de Physique Nucléaire et Hautes Energies,  
*Universités Paris 6 et 7, CNRS-IN2P3, F-75252 Paris*

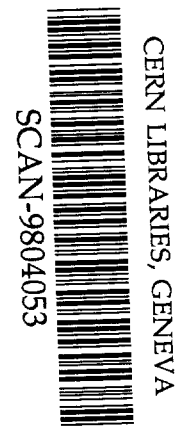
**G. Oxoby and J. Va'Vra.**

Stanford Linear Accelerator Center  
*Stanford University, Stanford CA 94309 USA*

**D. Warner and R.J. Wilson.**

Colorado State University  
*Fort Collins, CO 80523 USA*

*Talk given by D. Breton at the 3rd LHCC Electronics Workshop  
September 1997, London*



swg815

**U.E.R**  
de  
l'Université Paris-Sud



Institut National  
de Physique Nucléaire  
et  
de Physique des Particules

Bâtiment 200 - 91405 ORSAY Cedex

## BaBar DIRC Electronics Front-End Chain.

P. Bailly<sup>1</sup>, C. Beigbeder<sup>2</sup>, R. Bernier<sup>2</sup>, D. Breton<sup>2</sup>, G. Bonneaud<sup>3</sup>, T. Caceres<sup>2</sup>, R. Chase<sup>2</sup>, J. Chauveau<sup>1</sup>, L. Del Buono<sup>1</sup>, F. Dohou<sup>3</sup>, A. Ducorps<sup>2</sup>, F. Gastaldi<sup>3</sup>, J.F. Genat<sup>1</sup>, A. Hrisoho<sup>2</sup>, P. Imbert<sup>2</sup>, H. Lebbolo<sup>1</sup>, P. Matricon<sup>3</sup>, G. Oxoby<sup>4</sup>, C. Renard<sup>3</sup>, L. Roos<sup>1</sup>, S. Sen<sup>2</sup>, C. Thiebaux<sup>3</sup>, K. Truong<sup>2</sup>, V. Tocut<sup>2</sup>, G. Vasileiadis<sup>3</sup>, J. Va'Vra<sup>4</sup>, M. Verderi<sup>3</sup>, D. Warner<sup>5</sup>, R.J. Wilson<sup>5</sup>, G. Wormser<sup>2</sup>, B. Zhang<sup>1</sup>, F. Zomer<sup>2</sup>.

<sup>1</sup>Laboratoire de Physique Nucléaire et de Hautes Energies, Universités Paris 6 et 7, CNRS/IN2P3, 75252 Paris, France

<sup>2</sup>Laboratoire de l'Accélérateur Linéaire, Université Paris-Sud, CNRS/IN2P3, 91405 Orsay, France

<sup>3</sup>Laboratoire de Physique Nucléaire et de Hautes Energies, Ecole polytechnique, CNRS/IN2P3, 91128 Palaiseau, France

<sup>4</sup>Stanford Linear Accelerator Center, Stanford University, PO Box 4349 Stanford CA 94309 USA

<sup>5</sup>Colorado State University, Fort Collins, CO 80523 USA

*Abstract*

The DIRC Front-end electronics chain for the BaBar experiment is presented. Its aim is to measure to better than 1 ns the arrival time of Cerenkov photoelectrons, detected in a 11,000 phototubes array and their amplitude spectra. It mainly comprises 64-channel boards (DFB) equipped with eight ASIC VLSI full-custom Analog Chips, performing zero-cross discrimination with 2 mV threshold and shaping, four ASIC VLSI full-custom Digital TDC chips, performing timing measurements with 500 ps binning and a readout logic selecting hits in the trigger window, and crate controller cards (DCC) serializing the data collected from up to 16 DFBs onto a 1.2 Gb/s optical link. Extensive test results of the chips pre-production units will be presented, as well as system tests.

## I. INTRODUCTION

The DIRC Sub-system of the BaBar Detector [1] is intended to provide particle identification, particularly separate  $\pi$  and K mesons to better than three sigmas for momenta between 0.15 and 4 GeV/c. Cerenkov photons are internally reflected in 144 quartz bars towards 10,752 photomultiplier tubes (PMT). A water tank is used as leverage between the quartz bars ends and the photomultipliers. The Cerenkov angles are deduced from the pattern created on the PMT wall. The momentum is measured in the BaBar Drift Chamber. The noise in the DIRC due to the PMTs themselves is estimated to 1 kHz, the PEP II machine noise is estimated to 30 kHz including a safety factor of ten; for an average BB event, 5.7 primary tracks hit the DIRC and produce each 33 photoelectrons to which must be added six extra hits from background generated by these tracks. An equivalent number of background photons of the order of 200 is generated by secondary interactions between the event tracks and the detector (mostly Compton scattering in the quartz). Therefore, photomultipliers with a 1 ns time resolution have been chosen, that the

Front-end electronics should not degrade significantly [2]. The Level 1 trigger is built from Drift Chamber, Calorimeter, and Muons Detector flags. Its latency is 12  $\mu$ s, with an uncertainty of 1  $\mu$ s. On receipt of the Level 1 trigger, raw data are pulled from the Front-end electronics, after selection within the corresponding time-window. Pipelining is avoided using the accurate time information that is provided by the DIRC Front-end chips. Therefore, the dataflow from the Front-end electronics to DAQ is reduced by a factor of ten.

## II. SYSTEM DESCRIPTION

A full description of the system is given in [3]. The Front-end electronics, shown Figure 1, is installed very close to the detector, in order to save cables and keep the required single electron sensitivity. It is therefore highly integrated. CMOS electronics is used wherever possible, housed in 192 DIRC Front-end Boards (DFB). Twelve Front-end VME mechanics crates are linked to the data acquisition system by twelve BaBar standard 1.2 Gbit/s optical fibers. The 1 Gbit/s stream is paralleled in the 16-slot crates at 59.5 MHz. Six readout modules [4] equipped with Power PC 604 chips process the DIRC data for data-block building, detector calibration, and other purposes. The real-time commands such as Level 1 accept, fast strobes, are dispatched through the BaBar Electronics under control of a Fast Control Timing System housed in the VME DAQ crates.

## III. PHOTOMULTIPLIERS ELECTRONICS.

The DIRC PMT base system comprises printed circuit boards equipped with surface mounted components allowing to operate the phototubes around 1.1 kV. Boards are overcoated with an insulating coating on both sides.

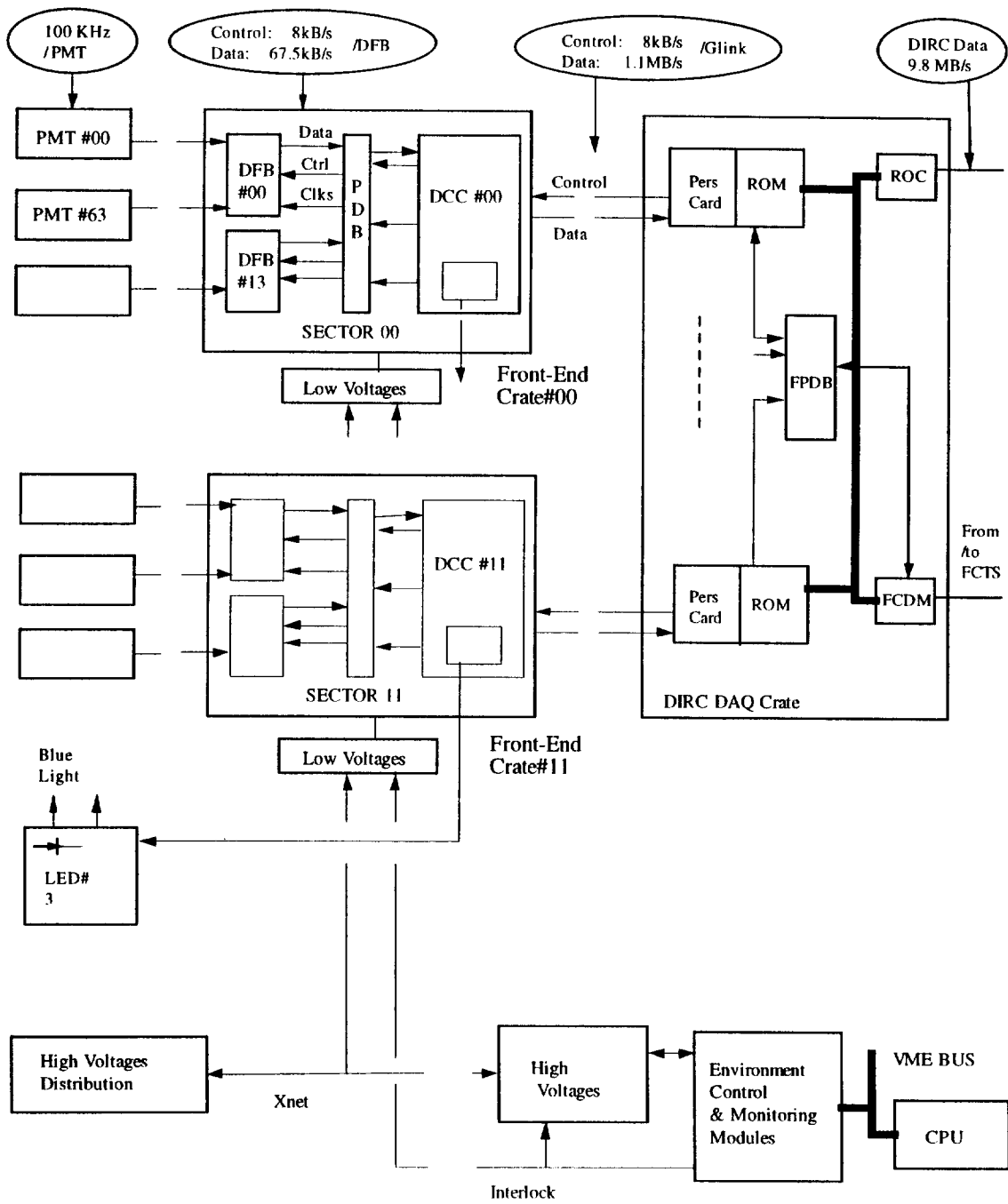


Figure 1. DIRC Electronics and Dataflow

A molded plastic base housing has been designed and passed the SLAC fire requirements. A custom high voltage small size connector has also been designed. A distribution board feeds 16 PMT channels. The planned base current is  $150 \mu\text{A}$ .

The High Voltage System, in the electronics house, comprises 56 high voltage channels per sector, sent to the front-end through twelve 56-way high voltage cables. The voltage can be set between 1 kV and 1.6 kV.

#### IV. ANALOG CHIP.

The PMT signals are amplified, thresholded and pulse shaped by an 8-channel analog chip [5,6] shown Figure 2. A digital pulse timed with the peak of the input pulse is output by a zero-cross discriminator, as well as a pseudo-gaussian pulse shaped at 80ns peaking time. The Analog Chip block-diagram is shown Figure 4.

##### A. Zero-Crossing Detection

A time resolution better than 800 ps over an amplitude range of 20 is achieved using the crossing of a zero level from the differentiated input pulse. In practice, instead using two discriminators, one for arming, the other for timing, a single hysteresis comparator is used, where the hysteresis is set equal to the threshold. Therefore, the trailing edge is synchronous with the zero-crossing of the input pulse. This edge is pulse-shaped as a 5ns digital pulse sent to the TDC chip. A first amplification stage, common to all channels is implemented with a programmable gain. The comparator hysteresis is kept constant, the effective threshold being obtained by changing the gain of the input amplifier, corresponding to a threshold between 1 and 10 mV. The dead time after a zero-crossing detection is 80ns.

##### B. Pseudo-Gaussian Pulse Shaping

A CR-RC pulse shaper peaking at 80ns provides a maximum output proportional to the input charge. Analog voltage gain is set between 2.5 and 25. A multiplexer selects the channel to be output towards the ADC. Use is made of ICON active resistors [7] wherever high values are needed. The analog chip is manufactured by AMS (Austria Mikro Systems) using a  $1.2 \mu\text{m}$  2-poly 2-metal CMOS process. Total power is 200 mW. The chip area is  $14 \text{ mm}^2$ . It is housed in a 68 pin package.

##### C. Results

The Analog Chip time walk as a function of the input pulse amplitude is showed Figure 3. It is less than 800 ps on an amplitude range of 20.

#### V. DIGITAL CHIP

The digital chip [8,9,10] is a 16-channel TDC with 500 ps binning input buffering and selective readout of

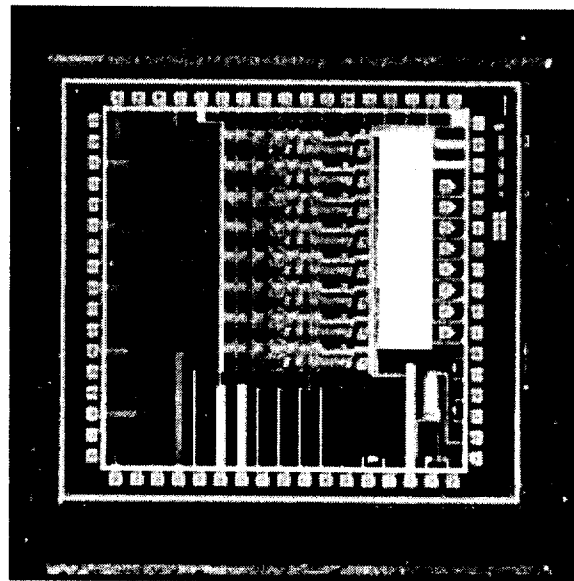


Figure 2. BaBar DIRC Analog Chip.

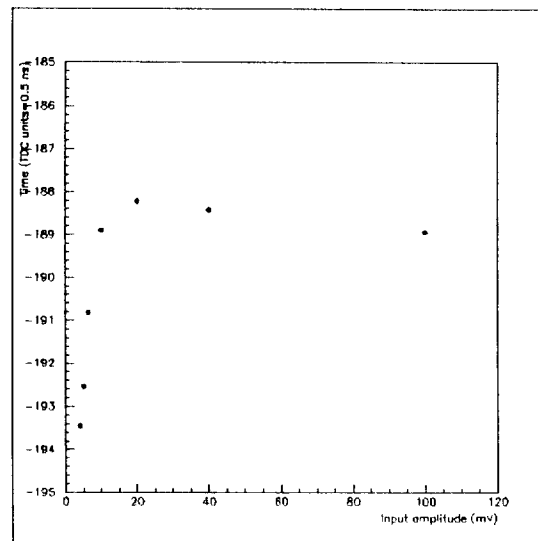


Figure 3. Analog Chip Time Walk.

the data in time with the trigger. The digital chip block-diagram is shown Figure 6. A binning of 500 ps has been chosen, with a full-scale of 32  $\mu$ s in order to cope with a first level trigger latency of 12  $\mu$ s, or higher. The selective readout process extracts data in time within a programmable window available at any time in an output FIFO.

Sixteen channels have been integrated in a single 0.8  $\mu$ m CMOS mixed-design chip housed in a 68-pin package, manufactured by ATMEL-ES2. The die size is 36 mm<sup>2</sup>, power less than 60 mW at 100 kHz average rate input on all channels, and 60 MHz clock frequency. The Digital Chip is shown Figure 5.

### A. TDC Function

The TDC section uses sixteen independent digital delay lines to digitize time with 500 ps binning [8]. A calibration channel allows to tune the chip delays on the 60 MHz reference clock, in order to cope with supply, temperature and process variations. Coarse time is measured with a fast counter common to all channels, providing the 11 most significant bits. Double pulse resolution (equal to the conversion time) is 32 ns.

### B. Input Buffering

An internal buffering is implemented with sixteen independent four-deep dual-port channel FIFOs in order to store data before a readout is requested, limiting the detector dead-time to less than 0.1% at 100 kHz input rate. Data stay there until the selective readout process described below transfer them to a common Latency FIFO.

### C. Selective Readout

The selective readout process [9] extracts data from the input FIFOs as soon as possible and builds a time-ordered list stored in an intermediate FIFO during the Level 1 trigger latency. Data beginning to be candidate for a possible incoming trigger are stored into an output FIFO, until they get out of the trigger resolution window. Therefore, at any time, the set of data in time with an incoming trigger is available in the output FIFO. A block-diagram is shown Figure 9. In order to sort the input FIFO data compatible with the 100 kHz maximum random input rate with an acceptable dead-time, time has been sliced in 256 ns frames, within which the arithmetics is performed in parallel using 15 comparators. In addition, possible errors from the wrap-around of the 11-bit coarse-time count are avoided.

### D. Measurements

The tests performed on the prototype chips have shown that the process uniformity within a chip allows to integrate 16 channels on a single die, keeping integral linearity under 100 ps RMS with the proposed calibration scheme. Figure 7 shows the differential linearity histogram for all channels of the preproduction run. An histogram of the selective readout window showing a peak of events synchronous with the trigger among random events is shown

Figure 8. The calibration process has been found stable and transparent, no differences have been found in time measurements with or without the phase-lock running. Crosstalk between adjacent channels is less than 125 ps, and power less than 60 mW at 100 kHz input rate. A yield of 90 % has been obtained on the hundred measured parts.

## VI. DIRC FRONT-END BOARD

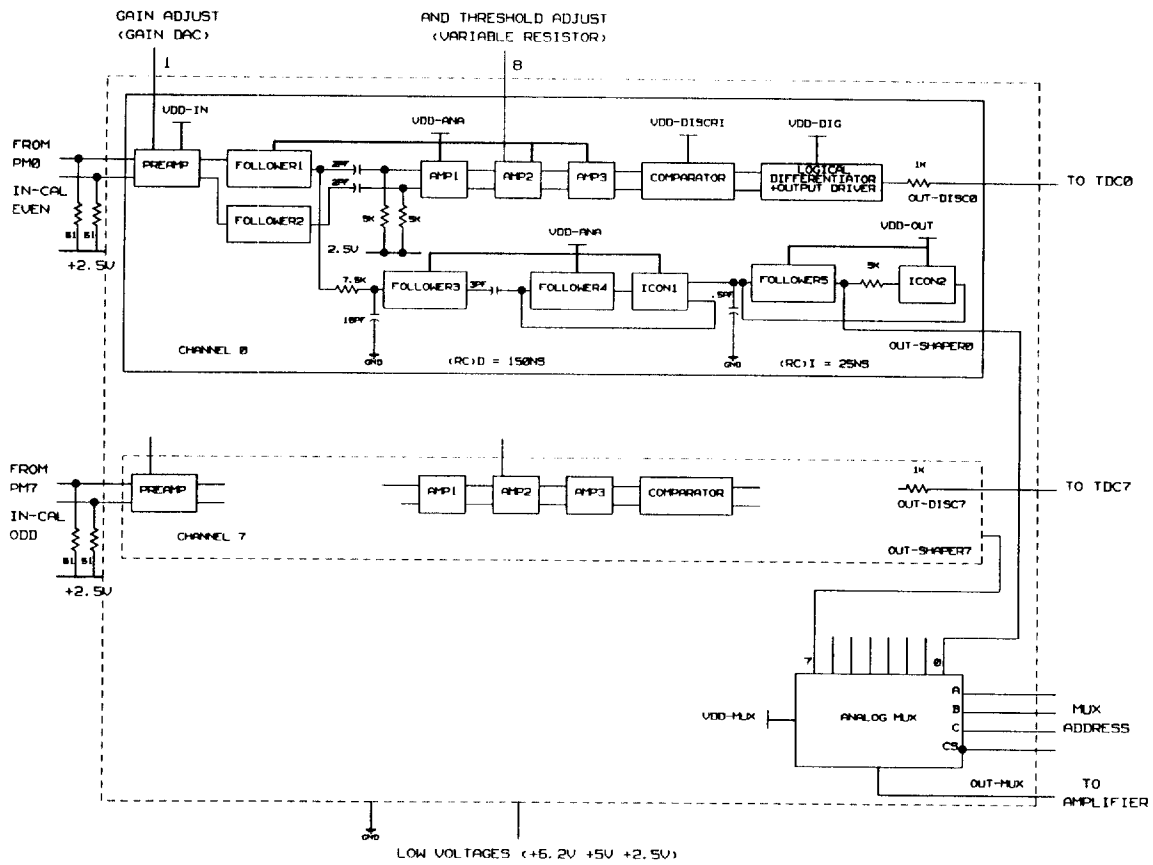
The DIRC Front-end Board (Figure 11) processes 64 PMTs inputs. It houses eight analog chips, four digital chips, one 8-bit flash ADC, and a set of FPGAs used for serial protocol encoding and decoding, multi-event buffers and control registers implementation, tests and diagnostic functions. It is connected to a custom crate backplane, the Protocol Distribution Board (PDB), described in section VII through one single 96-pins connector interfacing clocks, serial data input and output lines and supplies. The gain of each channel is set on-board within 5% of the nominal value. A unique ground plane is used as a voltage reference for all input signals. Such a grounding scheme, combined with a copper shield housing the analog chips and input circuitry, allows to operate thresholds down to 1 mV, the actual limit reachable on the analog chips test benches.

The DFB receives either run-time commands (BaBar detector global commands) such as L1 trigger accept, readout and calibration strobes, clear multi-event buffers, synchronization, and sub-system commands [11] used for initialization such as calibration control, threshold registers loading, trigger window loading, or hardware tests.

A dedicated software has been written that allows to build time and charge histograms and derive statistics for the 64 channels.

## VII. DIRC CRATE CONTROLLER

Twelve DIRC Crate Controllers (DCC) interface the Glink fiber optics coming from the six readout modules in the DIRC DAQ VME crate to the DIRC Front-end crates. The DCC comprises mainly the Glink interfaces, called DIRC Glink Boards, (DGB), and the DIRC Monitoring Board (DMB) that manages DIRC Detector environmental controls such as High Voltage status, magnetic field sensors, hygrometry, and temperature of the Front-end crates. It is interfaced to the system using the CAN-bus standard adopted within BaBar. The DMB monitors also the status of the Glink interface, and generates a digital pulse that triggers the light pulser for the DIRC detector calibration. This pulse is synchronous with a Calibration strobe sent by the Fast Control Distribution System of BaBar. DGB and DMB are connected together with on-boards connector. The PDB backplane distributes the 60 MHz demultiplexed bit stream from the 1.2 GHz sent through the fiber optics to the fourteen DFBs. The DMB houses also a pulse generator used to calibrate the DIRC detector.



### BABAR DIRC ANALOG CHIP

Figure 4. Analog Chip Block-Diagram.

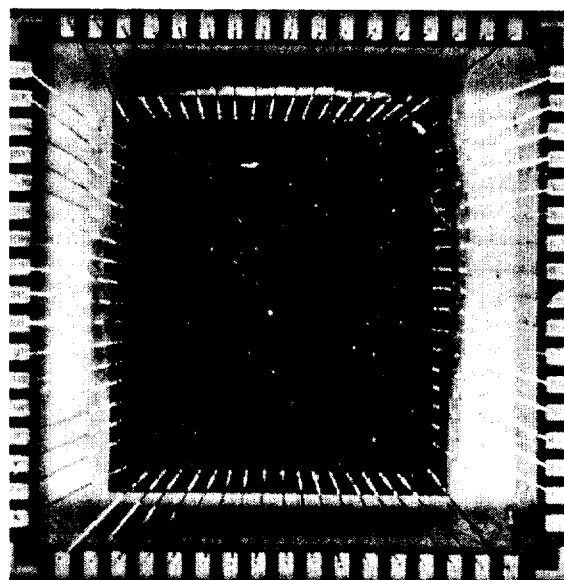


Figure 5. BaBar DIRC Digital Chip.

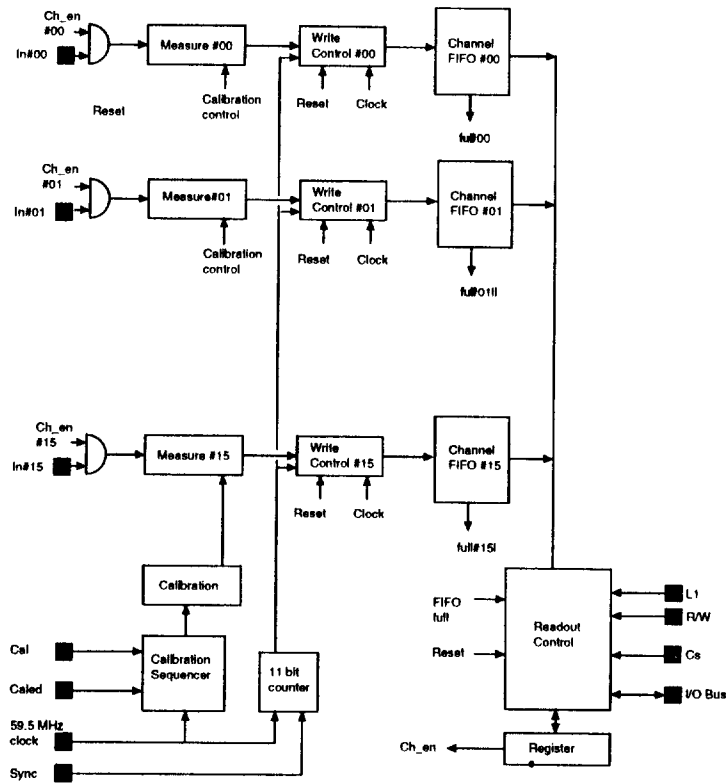


Figure 6. Digital TDC Chip Block-Diagram.

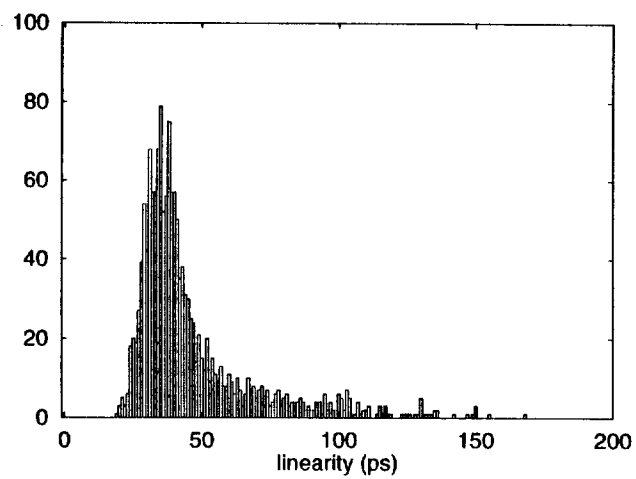


Figure 7. Digital TDC Chip Differential Linearity Distribution on 1,600 Channels.

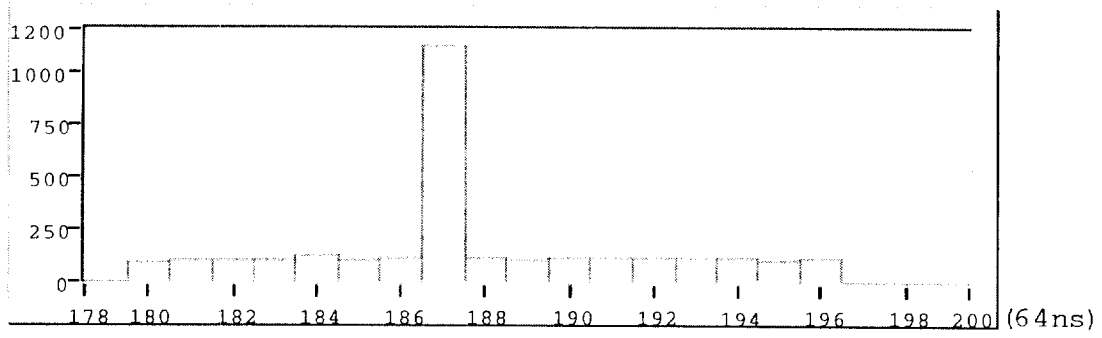


Figure 8. Readout Synchronous Events among Random Events.

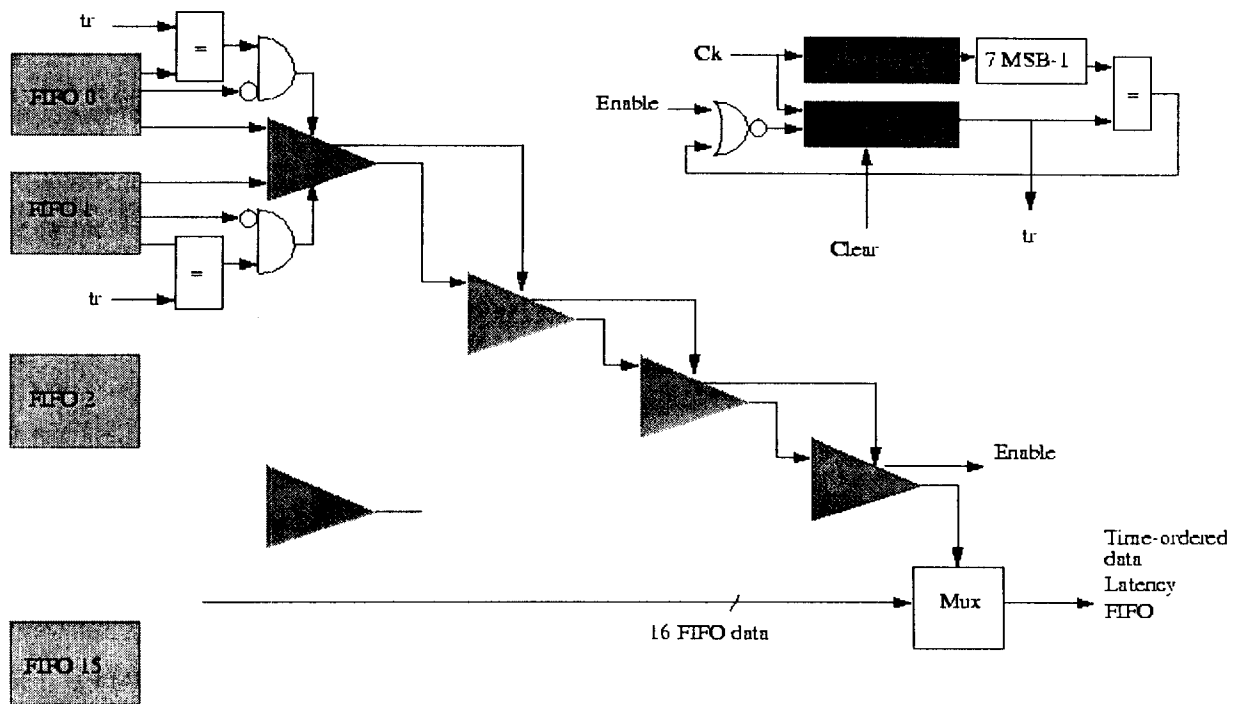
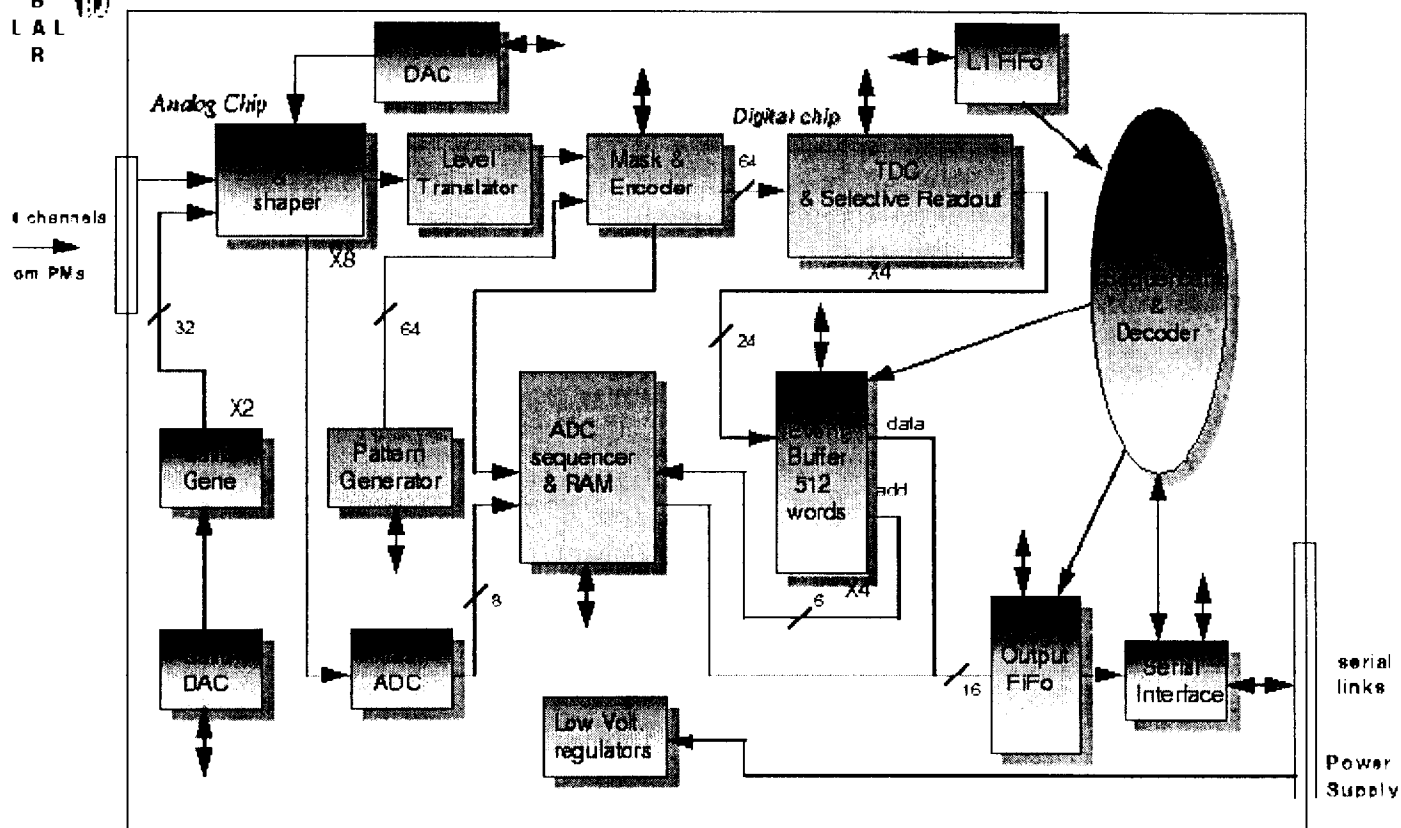


Figure 9. Digital TDC Chip Selective Readout.



# Dirc Front-end Board



LAL ORSAY - January 1997

Figure 10. DIRC Front-End Board Block-Diagram.

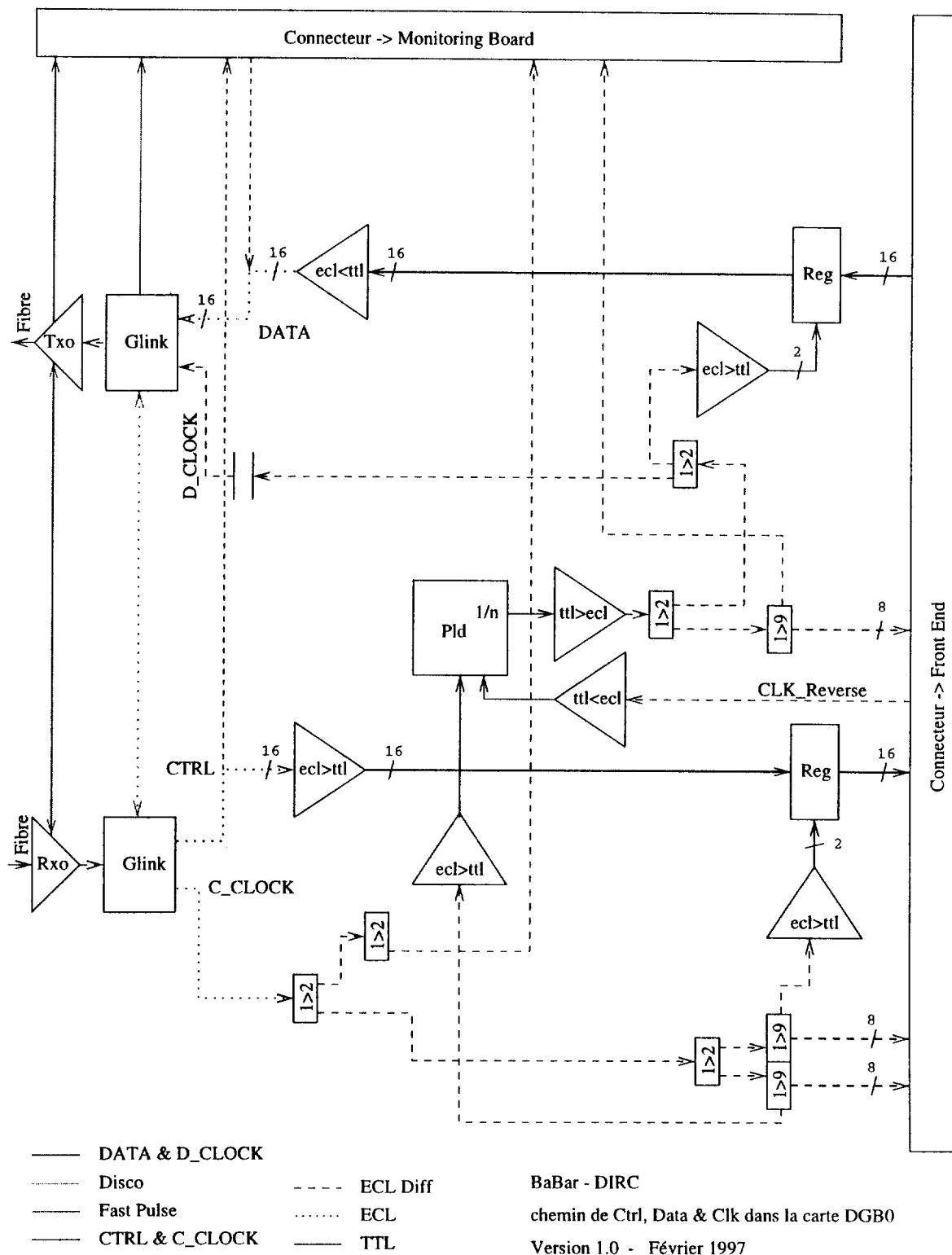


Figure 11. DIRC Glink Board Block-Diagram.

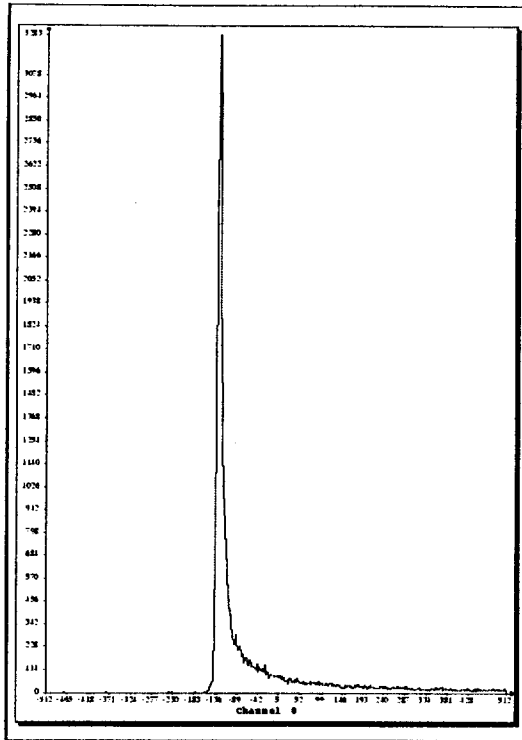


Figure 12. Time Histogram from Single Photo-Electrons.

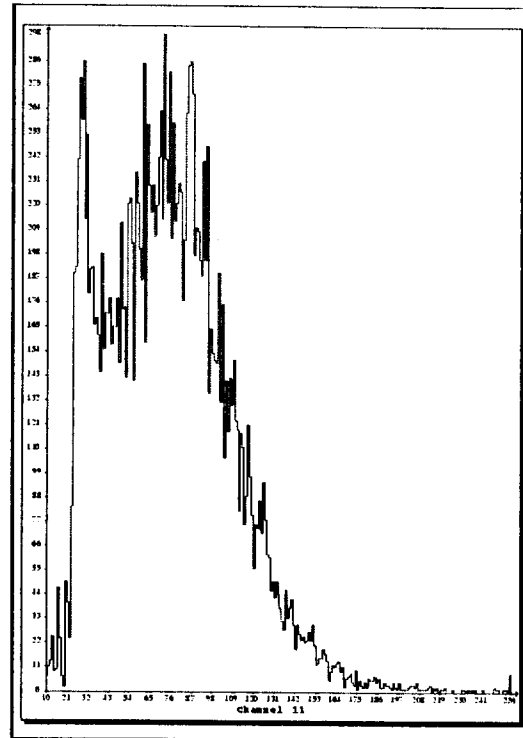


Figure 13. Charge Histogram from Single Photo-Electrons.

### A. DIRC Glink Board.

The DGB (Figure 12) receives two fibers optics for control (Clink) and data exchange (Dlink). It converts the 1.2 Gbit/s stream into sixteen 60 MHz streams linked to the Front-end cards by point to point connexions. Synchronization allows to perform time measurements with the required accuracy. Clock jitter measured at the end of a 30 m fiber after clock recovery in the receiver chip is 124 ps RMS in presence of data exchange. The main components of the DGB are:

- 1 The Glink transmitter/receiver chips from Hewlett-Packard, that perform multiplexing and demultiplexing function, clock recovery, error detection, and link control.
- 2 The Optical transmitter/receiver from Finisar.
- 3 Two pipe-line registers, one for each data stream.

### B. DIRC Monitoring Board.

The DMB includes a microcontroller chip Motorola 68HC705X32, the CAN bus interface, a pulse generator whose delay with respect to a global calibration strobe command is programmable with 500 ps steps, and the sensors for detector slow controls.

### C. Backplane.

The Protocol Distribution Board (PDB) is a 19 slots backplane, allowing to connect up to 16 DFB cards and the crate controller. The two remaining slots are used for

debugging purposes. Clocks are sent using ECL differential levels, data serial lines are standard TTL levels.

## VIII. RESULTS.

Extensive tests with the actual DIRC PMTs and a LED light source tuned to generate single photons events have been performed with the full Front-end electronics chain. The analog chip time walk can be seen on Figure 3 as a function of the input amplitude: after an initial walk-time of 2 ns very close to the threshold, a negligible effect is obtained between 10 and 100 mV. The charge and time spectra shown on Figures 12 and 13 have been obtained with a threshold set to 2 mV. A threshold of 1 mV can be used without digital to analog crosstalk or unstabilities. A BaBar run-time value of 3 mV is foreseen. Measurements synchronous and asynchronous with respect to the LED pulse gave satisfactory results, both in accuracy and efficiency.

## IX. CONCLUSION.

The DIRC Electronics Front-End Chain performs sub-nanosecond timing with single photo-electron over 10,000 channels. It makes use of two custom VLSI chips, a single comparator zero-crossing discriminator, and a digital TDC. The TDC chip delays are locked on the 60 MHz

system clock. The discriminator chip integrates a pulse shaper used to build single photo-electron response of the photomultipliers during calibration runs. The digital chip integrates a selective readout of data compatible with an incoming Level 1 trigger reducing the dataflow by a factor of 10. Both chips can process input signals up to an 100 kHz average rate. Chips are housed on a 64-channel board read by a Crate Controller connected to the Data Acquisition system using the Glink standard at 1.2 Gbit/s links. This complete electronic chain for 11,000 channels occupies a volume of about 1m<sup>3</sup> and dissipates less than 5 kW.

## REFERENCES

- [1] BaBar Technical Design report, SLAC-R-95-457, March 1995.
- [2] The DIRC Electronics Group.  
BaBar DIRC note 29, DIRC Electronics Requirements, Feb 1996.
- [3] The DIRC Electronics Group.  
BaBar DIRC note 324, DIRC Electronics, Oct 1996  
<http://www-lpnhep.in2p3.fr/babar/local/elec/fdr/ds.ps>
- [4] G. Haller.  
BaBar DAQ Readout Module.  
<http://www.slac.stanford.edu/BFROOT/doc/electronics/ReadoutModule/rom.html>
- [5] A. Ardelean, R.L. Chase, A. Hrisoho, S. Sen, K. Truong, G. Wormser.  
A discriminator and shaper circuit realized in CMOS technology for BaBar.  
Proceedings of the 7th Pisa meeting on Advanced Detectors, Livorno, Italy, May 1997, and LAL -RT-97-xx  
<http://www.slac.stanford.edu/BFROOT/doc/electronics/>
- [6] The DIRC Electronics Group.  
Analog Chip FDR Documents. June 1997.  
<http://www-lpnhep.in2p3.fr/babar/local/elec/fdr/anachip/anachip.html>
- [7] F. Anghinolfi et al.  
ICON, A Current Mode Preamplifier in CMOS Technology for use with High Rate Particle Detectors.  
IEEE 0-7803-0513-2/92 \$0.3.00
- [8] J.F. Genat.  
High Resolution Time to Converters, Nuclear Instruments and Methods, Vol A315, pp 411-414, 1992.
- [9] P. Bailly, J. Chauveau, J.F. Genat, H. Lebbolo, B. Zhang.  
A 500 picosecond resolution TDC for the DIRC at BaBar
- [10] B. Zhang.  
Developpement d'un Circuit integre VLSI assurant Mesure de Temps et Lecture selective dans l'Electronique frontale du Detecteur DIRC de l'experiance BaBar a SLAC. These de Doctorat. Universite Pierre et Marie Curie. Paris, France. Sept. 1997.
- [11] A. Ducorps et al.  
The DIRC Subsystem Commands.  
A 500 picosecond resolution TDC for the DIRC at BaBar  
<http://www-lpnhep.in2p3.fr/babar/local/elec/dfb-64Protocol.ps>

