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PERFORMANCE OF Si PAD SENSORS FOR A RICH DETECTOR

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Presented by P. Weilhammer

Abstract

Silicon pad sensors with 256 cells have been used to detect single photoelectrons from a CsI photocathode. These sensors are part of a Hybrid Photon Detector (HPD) to be used in a RICH detector in the LHC-B experiment. The I-V and C-V measurements are presented. The pad sensors are read out with the low noise VA2 chip. Results from tests with these detectors with a ^{90}Sr source are reported. Measurements of photoelectrons created by 160 nm wavelength photons in a CsI cathode in a test set-up are also reported. Finally, the prospects of using such sensors with fast LHC readout electronics are discussed.

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1 INTRODUCTION

Single Photon detection combined with good position resolution is of great interest both for imaging applications and for particle physics experiments. In particle physics the detailed study of B-meson decays has become a focus of activity and a substantial effort is at present devoted at high luminosity e^+e^- colliders (B factories) and at high energy proton colliders to a measurement of possible CP violation effects in the B-meson system. One of the important ingredients for a clean measurement of CP violation effects is very efficient particle identification. In the case of high energy hadron colliders, identification up to high energies is essential. RICH Cerenkov counters are the most performant detectors for this purpose.

In this article a development is described to build a Hybrid Photon Detector using multicell Si pad detectors [1] with readout electronics originally developed for the readout of Si strip detectors. The principle of the readout is to route each pad with a thin metal line on top of a 5 μm thick oxide to the periphery of the device, where a bond pad layout identical to that of a strip detector is implemented. This type of sensor is a straightforward solution when pad sizes are required which are either bigger or smaller than naturally covered by pixel detectors, where the one to one correspondence of the size of one electronics channel and the pixel dimensions of the sensor put practical limits to the size of a single cell. It is in general an attractive alternative to pixel detectors in cases where the number of cells are not too big. The application of pad sensors is clearly limited by the maximal number of pixels which can be read out in this way. A practical limit when using 4″ sensor technology is about 6000 pads with an area of each pad less than 1 mm^2. Advantages of pad sensors are that there is no constraint on the readout electronics in terms of layout space and that a simple and robust connection technology with wire bonding exists. Disadvantages are increased capacitance from routing lines leading to higher noise and the limitations in number of cells for single devices.

In the following, results from a prototype HPD detector are described. This prototype consisted of two 128 cell pad detectors. Each detector is connected to one 128 channel VA2 readout chip [2]. The pad sensors and the readout chips are mounted inside a vacuum chamber. Above the pad sensors, at a distance of 50 mm, a CsI photocathode was mounted with a metal grid connected to a high voltage supply. The CsI photocathode could be illuminated by photons from a hydrogen flash lamp with a wavelength of 160 nm through a CaF_2 window. Data were taken at different high voltage values, and with different light source intensities.

A different approach to building an HPD, using pixel detectors and pixel readout electronics, is described in Ref. [3].

2 THE Si DETECTOR

2.1 The Si pad sensor

Each Si sensor [4] consists of 128 pads of 4×4 mm^2 size with an approximately semicircular cross-section with a radius of 36 mm and a total area of 20.48 cm^2 [Fig. 1]. Each pad is defined by a 3.96×3.96 mm^2 p^+ implant on high resistivity n^- material (~ 5 kΩ cm). The separation between pads is 40 μm. A guard ring surrounds the periphery of the pads. Each pad is contacted to a metal line, which is routed to one side of the sensor, where 128 bond pads, 120×60 μm^2, with a transverse distance of 50 μm are arranged in two rows [see insert in Fig. 1]. These double rows of bond pads were duplicated to allow two different positions for placing the readout chips.

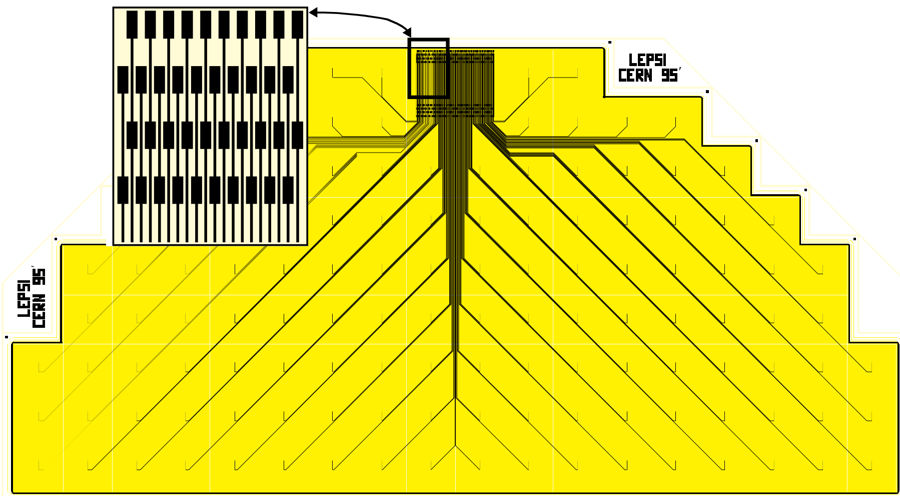

Figure 1: Layout of Si pad sensor.

The basic steps in the fabrication are:

– Boron implantation through 1000 Å thick oxide.
– A very shallow ($\sim$ 200 nm depth) phosphorous implantation on the reverse side of the sensor to have a thin entrance window to minimize charge loss in the dead n^+ layer.
– Deposition in 2 steps of a 5 μm thick LTO oxide on the p^+ side.
– Etching of via-holes (40×40 μm^2) through the thick oxide to allow contacting of the p^+ pads.
– Aluminium metallization on top of the thick oxide. The Al thickness was chosen to be 3.5 μm in order to ensure low resistivity of routing lines. The metal lines were etched to 7 μm width.
– The n^+ implant was covered with a very thin (50 Å) Aluminium layer for the bias contact.

In the processing, 4″ wafers were used with two thicknesses: 500 μm and 1000 μm. Thick material was used for this application in order to obtain a low backplane capacitance for these relatively big pads.

2.2 The readout electronics

The pad sensor was bonded to a VA2 low noise Si strip detector readout chip with 128 channels. Each channel consists of a charge sensitive preamplifier using the folded cascode configuration, a shaper, and a sample-and-hold (S/H). A 128 cell analog multiplexer on the chip switches sequentially all 128 S/H capacitors to a differential output bus which is connected to a VME Flash ADC. The data are clocked out with 2 MHz. The chip also has an input multiplexer which allows a test pulse to be sent to each individual channel. Furthermore, the chip control allows the output of the shaper of each channel to be switched separately to the differential output bus, and in this way directly sample the waveform at the output of the shaper.

The measured performance of the chip is summarized in Table 1.

Table 1

Noise	ENC = 79 e^- + 16 e^-/pF	$\tau_p = 1\ \mu s$
Noise	ENC = 68 e^- + 11 e^-/pF	$\tau_p = 2\ \mu s$
Power consumption	$P \approx 1.5$ mW/channel	$I_d = 500\ \mu A$
Dynamic range	± 17 fC fully linear	
Peaking time adjustable	$\tau_p = 0.5 - 3\ \mu s$	

3 THE SENSOR PERFORMANCE

The important performance criteria are the leakage current and the capacitance of each pad to ground. The leakage current needs to be small in order to keep the contribution of the shot noise small. Also since the sensor has DC coupling into the input of the preamplifier and considering that the amplifier is originally designed for AC coupling, it is important not to exceed a few nA per pad in order not to drive the preamplifier too far off its working point. The capacitance will determine the overall noise performance of the system.

One pad sensor was specially prepared to measure the capacitance and leakage current of single pads. For this purpose all channels have been bonded to a kapton trace and could be grounded together. Then any chosen single channel could be disconnected from the kapton trace and be contacted individually for current measurement or be connected to a capacitance meter. A positive bias voltage was applied to the backplane of the sensor. Leakage currents on two particular pads were measured to be between 50 to 60 pA with a relatively flat plateau above V_{bias} = 80 V up to V_{bias} = 120 V [Fig. 2]. The leakage current of all pads was 70 nA at V_{bias} = 80 V but was rising to 1.2 μA at V_{bias} = 140 V. The relatively high average current at 80 V and the strong rise of current above 80 V is attributed to contributions from a few single pads which develop high currents once the depletion voltage is exceeded.

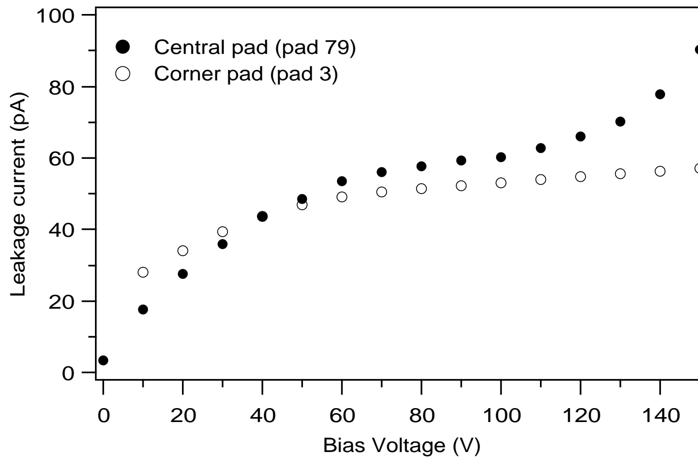

Figure 2: Leakage current versus bias voltage of single pads, normalised to 20°C.

The capacitance of all pads to the backplane has been measured to be 420 pF [Fig. 3a] in good agreement with 424 pF calculated from the surface area of 20.5 cm^2 of all pads. It can be seen that the sensor depletes fully around 80 Volts. A single pad in the corner of the sensor has 3.5 pF and a single pad in the middle of the sensor has 3.7 pF [Fig. 3b], with respect to the backplane. The capacitance of one pad to all the neighbours

was measured by grounding all pads except the pad under measurement. For a pad at the edge of the sensor 3.2 pF were measured and for a pad in the middle, which is completely surrounded by all other pads, 6.3 pF were measured [Fig. 4].

The total load capacitance of one pad is therefore taken to be 11 pF including 1 pF capacitance for the bond connection.

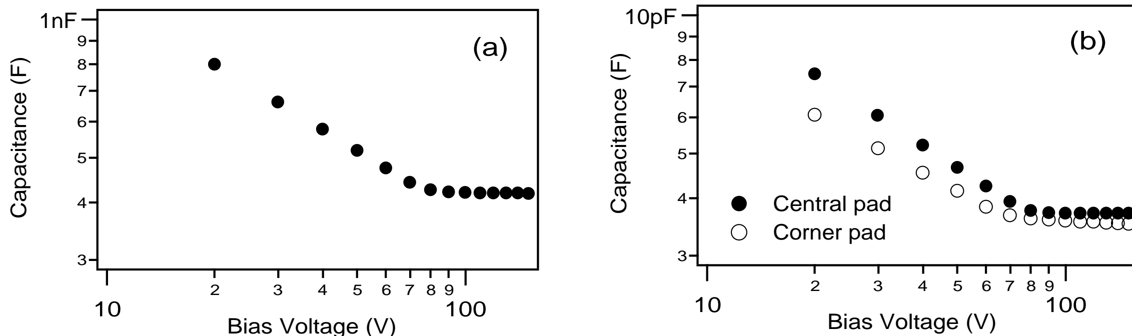

Figure 3: Capacitance of (a) all pads and (b) a single pad to the backplane.

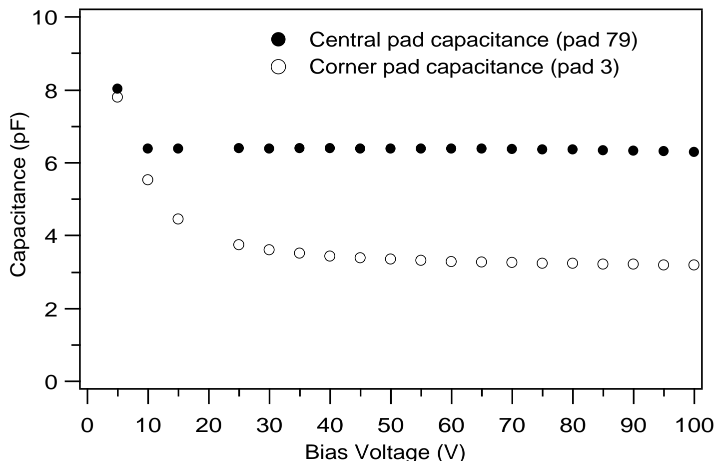

Figure 4: Capacitance of single pads to neighbours.

4 DETECTOR PERFORMANCE ON ^{90}Sr TEST SET-UP

One of the 500 μm thick detectors was exposed to a ^{90}Sr source. The VA2 chip was latched by a trigger signal from a scintillation counter placed underneath the Si detector.

The bias voltage was set to 20 V since the charge in the Landau tail from a β traversing the fully depleted detector would have saturated the VA2 chip which has a dynamic range of less than ± 15 fC. Figure 5 shows the Landau distribution for ^{90}Sr betas. Figure 6 shows collected charge measured at the peak of the Landau distribution as a function of the bias voltage. The decrease of the collected charge for voltages below full depletion is slower than expected from a $\sqrt{(V/V_{F.D})}$ law. ($V_{F.D}$ is voltage at full depletion.) This demonstrates that charge created in the non-depleted region of the sensor is transported into the depletion zone by diffusion over a distance of several tens of microns.

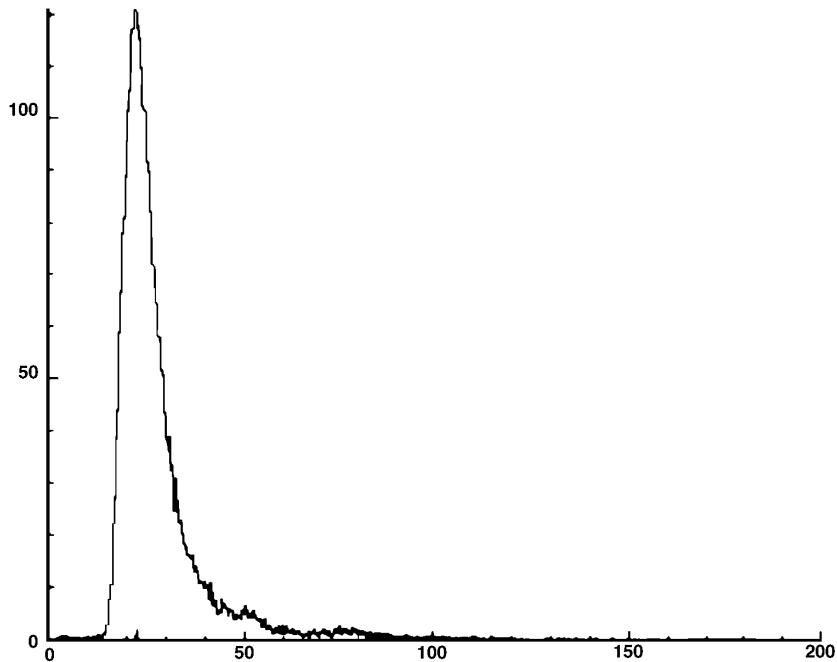

Figure 5: Landau distribution for betas from a ^{90}Sr source. Bias voltage was 20 V.

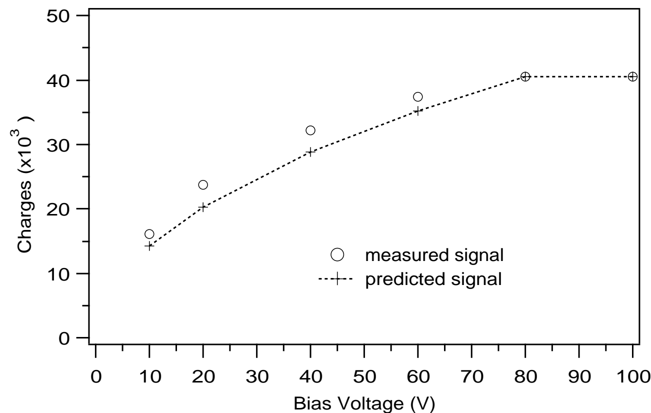

Figure 6: Collected charge as a function of bias voltage. Dotted line is the charge at full depletion times $\sqrt{\mathrm{V}/\mathrm{V}_{\mathrm{F.D}}}$, $\mathrm{V}_{\mathrm{F.D}} = 80$ V.

The cluster multiplicity is strongly peaked at n = 1 (94% of the hits). The width of the pedestals of all pads was measured to be between 3 and 3.8 ADC counts except for 4 channels with a width of around 5 ADC counts. These are the pads lying underneath the bond pads.

At full depletion the most probable value of the observed charge corresponds to approximately 41 000 e^- in a 500 μm thick Si detector. Using the Landau peak as a calibration the noise for most of the pads is calculated to be between 300 and 390 e^- ENC. Taking the measured noise slope of the VA2 for a peaking time of 900 ns, the predicted noise is calculated to be around 280 e^- ENC. Another small contribution to the noise can be expected from the ohmic resistance of the routing lines. The longest line has

a resistance of 80 Ω. Given a transconductance of 6 mS for the input FET of the VA2, this increases the total noise by another 10–15%. Shot noise from the measured leakage current during data taking (I_L =130–150 nA) contributes about 100 e^-. Therefore in total one predicts a noise of about 325 e^- ENC. Within the uncertainty of the calibration there is good agreement between the measured value and the predicted value of the noise.

5 A HYBRID PHOTON DETECTOR PROTOTYPE

5.1 Experimental set-up

The Si pad detector was assembled together with a CsI photocathode, a high voltage supply, and a pulsed light source in order to measure the response of the detector to single and multiple photoelectrons emitted from the CsI photocathode and accelerated to energies between 3 keV and 15 keV.

5.1.1 The Si pad detector mount

The Si pad sensors were placed on a ceramic support plate [Fig. 7] which could hold two sensors. Each sensor was clamped with small ceramic plates. The VA2 chip was glued (in a final HPD tube the chip will also be clamped) to a ceramic board providing the chip supply and control lines. All 30 gold traces on this hybrid are routed through metallized, laser drilled holes from the lower side of the hybrid to the upper side. A second ceramic board distributes these lines to two standard vacuum feed-through connectors with 16 pins each, which are mounted on a metal base plate with vacuum seals. The 128 channels of the VA2 chip are connected by wire bonding to the bond pads on the pad sensor and the control and supply lines are bonded to the corresponding pads on the chip. Again wire bonding is used to connect the lines on the two hybrid boards.

The pins of the two feed-through connectors are connected via an adapter board to the VA2 repeater card which defines control signals and voltage levels and drives the output signals from the chip.

5.1.2 Data acquisition

A NIM timing unit is used to produce the clock pulses and the shift-in pulse for the chip multiplexer and register, together with the hold signal to latch the data on the chip at the correct time. The analog information on each S/H is then clocked on a differential line into a VME Flash ADC and memory unit. The online DAQ program monitors the data, calculates and updates pedestals and noise from each channel, and outputs pedestal subtracted data after common mode correction to the hard disk.

5.1.3 The photocathode, the light source, and the high voltage system

A CsI photocathode is evaporated on a CaF window, which can be vacuum sealed. A pre-deposited gold grid (85% optical transparency) is used to define the potential of the photocathode. As a light source a pulsed hydrogen lamp is used with a wavelength of 160 nm. The light is guided in Ar gas to the CaF window and can be collimated to a spot of about 500 μm diameter. The collimator can be moved in x-direction by ±12 mm and in y-direction by ±6 mm. The high voltage power supply provides up to 15.7 kV. It was selected for minimum ripple. The system provides no focusing. The distance between the anode, which is the backplane of the Si pad sensor, and the CsI cathode is 50 mm. The base plate with the Si detector and the CaF window are mounted vacuum tight on the bottom and top of a steel vessel [Fig. 8]. More details on this set-up can be found in reference [5].

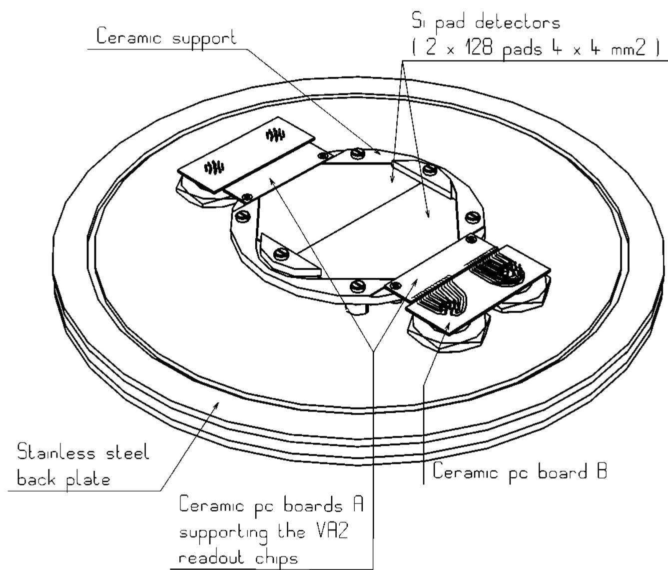

Figure 7: Ceramic support plate for Si pad sensor.

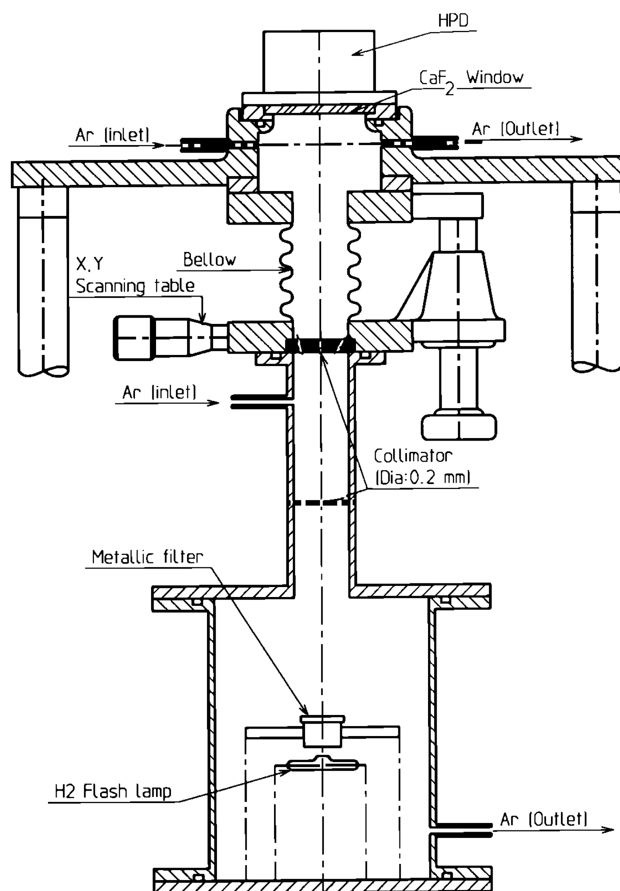

Figure 8: The HPD set-up.

5.2 Experimental results

Data were taken at different settings of the high voltage and with different light intensities. The peaking time of the VA2 circuit was set to $\tau_{\mathrm{p}} = 2\ \mu$s. Figures 9 and 10 show typical pulse height spectra taken at voltages of 15.7 kV and 8.4 kV for low (a) and high (b) light intensities. These data are taken with the light source positioned in the middle of a particular pad. Spectra taken with other pads are very similar. At 15.7 keV and 8.4 keV the photoelectron peak is separated from the pedestal peak by about 15 σ, respectively 6 σ of the electronic noise. The electronic noise has been determined from a fit to the pedestal taken at 0 kV. In order to obtain a calibration, data with a ^{241}Am source were taken. This yielded a calibration of 102 e^- per ADC count. Thus a noise of 270 e^- ENC was calculated for this particular pad. It was checked that charge collection was complete at bias voltages above V_B = 70 V [Fig. 11]. The pulse height spectrum exhibits clear 2, 3 and 4 photoelectron peaks spaced equally from each other. The one photoelectron peak corresponds to 4130 collected charges.

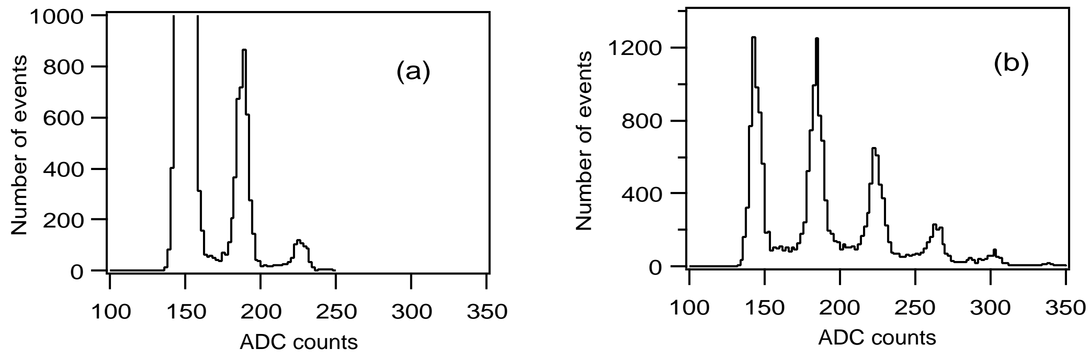

Figure 9: Pulse height spectra measured at 15.7 kV acceleration voltage (a) low light intensity, (b) high light intensity.

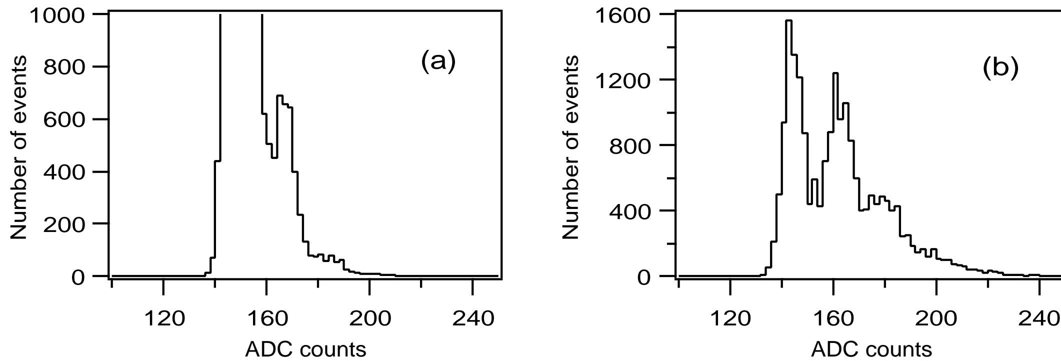

Figure 10: As Fig. 9 for 8.4 kV acceleration voltage.

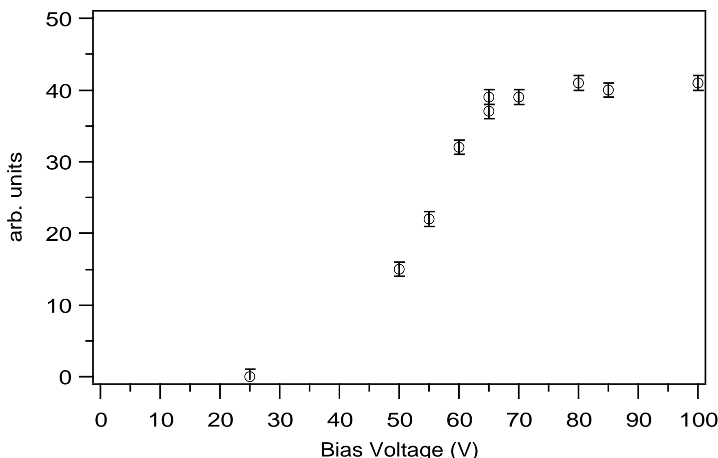

Figure 11: Pulse height of single photoelectron peak as function of bias voltage of pad detector.

The region between the pedestal and the 1 photoelectron peak exhibits an approximately flat distribution at the level of about 8% of the 1 photoelectron peak intensity for the 15.7 kV data. The region between the 1 and 2 photoelectron peaks and the 2 and 3 photoelectron peaks has approximately 16% and 27% flat distribution with respect to the 2 and 3 photoelectron peak intensities. A more detailed inspection of the distribution shows that this intensity is flat only in a region below about 175 ADC counts for the 1 photoelectron peak contribution. Above 175 ADC counts it increases towards the 1 photoelectron peak to a maximum of about 8 times the constant value. This behaviour can be seen more clearly in Fig. 12, which shows conversion electrons from ^{73}As decays with 42.3 keV and 52 keV energy measured in a Si pad detector which was manufactured in an identical way. This continuum part of the spectrum, which is observed when low energy electrons are absorbed in a Si detector is referred to as the back-scattering contribution [6]. Electrons are scattered elastically from Si nuclei into the backward hemisphere and will exit from the Si back into the acceleration field zone. Except for scattering angles very near to 180° these electrons will not fall back onto the same pad. However, with the very good separation of the one photoelectron peak from the noise, most of the back-scattered electrons are detected in the proper pad, thus giving valid position information. The small fraction of back-scattered electrons which fall back on other pads on the sensor will however appear like an uncorrelated background.

In order to achieve an accurate determination of the peak positions in the spectra the form of this continuum has to be parametrized in an appropriate way. Figure 13 shows the charge deposition of the electrons in the Si detector as a function of the acceleration voltage as determined from the single photoelectron peak position in the spectrum for two different light intensities. The observed charge is the charge deposited by the electrons in the sensitive volume of the detector. The thickness of the dead layer could be estimated from the exact observed position of the ^{73}As conversion electron peak (nominally 42.3 keV) in Fig. 12, since the energy scale in this plot is precisely known from a simultaneous measurement of the ^{241}Am γ-line at 59.536 keV [7]. The fitted peak position is 41.964 keV which yields an energy loss of ΔE = 0.34 keV. Using the non-relativistic Bethe-Bloch formula for ionising energy loss dE/dx in Si this value corresponds to an effective dead layer thickness of 290 nm. This dead layer thickness is in good agreement with what one

expects from the implantation depth of 200 nm, which was targeted in the processing and the subsequent anneal step.

Applying the Bethe-Bloch formula at 15.7 keV energy the energy loss in a 290 nm thick dead layer is 0.67 keV. Thus the expected charge using w = 3.62 eV is calculated to be 4150 charges in perfect agreement with the 4130 charges found from the ^{241}Am calibration.

In Figure 13, the circles show calculated values of the expected charge correcting for a loss of charge in a dead layer of 290 nm thickness. These calculations assume again an average ionisation energy of w = 3.62 eV to produce an electron hole pair in Si. The data are in excellent agreement with this calculation. It can be seen that no charge will be observed in the Si below an electron energy of about 2.6 keV.

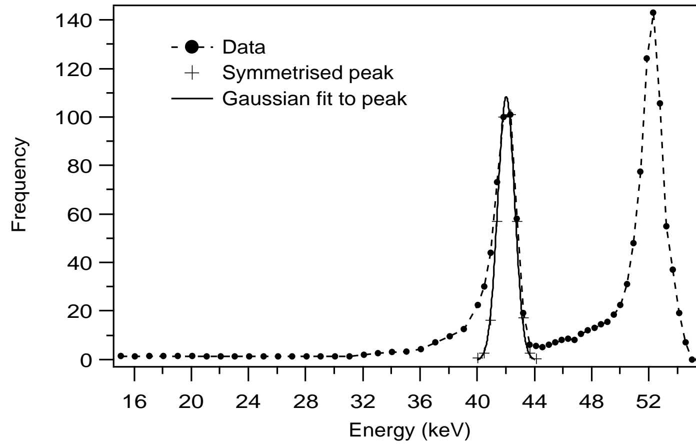

Figure 12: Conversion electron spectrum from ^{73}As isotope.

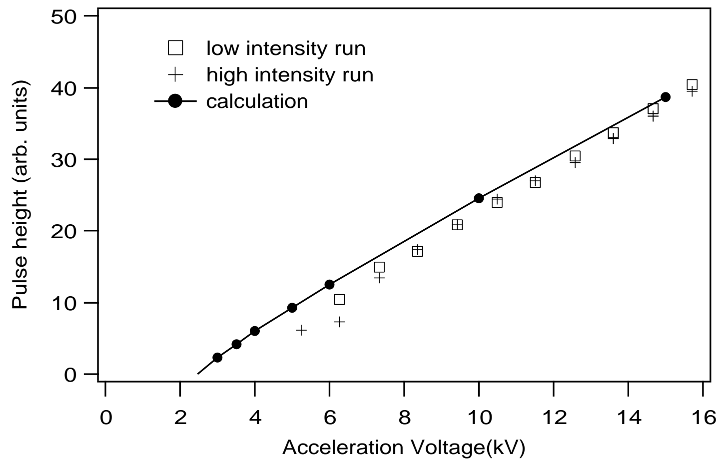

Figure 13: Measured charge at single photoelectron peak as a function of acceleration voltage at low and high light intensities. The circles are predicted values using the non-relativistic Bethe-Bloch formula.

6 PROSPECTS FOR READOUT WITH FAST LHC READOUT ELECTRONICS

With approximately 4000 charges available from a single photoelectron with an accelerating voltage of 15 kV very low noise electronics is an essential issue. Over the past years fast readout electronics for Si strip detectors to be used in the inner tracking detectors at LHC has been developed [8]. These circuits have been optimized for load capacitances of 15-20 pF corresponding to typical Si strip detectors with 12 cm long strips. In particular, a readout chip with a bipolar input stage, an analog pipeline and a fast output multiplexer has been developed and implemented in the form of a 32 channel prototype SCT32A chip [9]. The input stage consists of a bipolar preamplifier followed by a fast shaper producing a semigaussian waveform. The 112 cell pipeline is a capacitor array with switches to a read and a write line. The control block allows simultaneous read and write. The shift registers controlling the write and read operations are clocked at 40 MHz. Thus a first level trigger delay of up to 3 μs is possible. This chip has been produced in radiation hard DMILL technology [10]. The SCT32A chip has been tested and the noise has been measured as a function of external load capacitance. In Fig. 14 the pulse form for an injected charge of 3.6 fC is shown before (a) and (b) after irradiation. The irradiation was done with a ^{60}Co source and a total dose of 10 Mrad. There was no load on the input. The peaking time is 19 ns (a) and 25 ns (b).

The noise as a function of capacitance is shown in Fig. 15 for a test circuit containing only the preamplifier and the shaper (solid lines) before and after irradiation. The two separate points in Fig. 15 show the noise performance for the 32 channel full architecture chip. The main limitations in this chip it its present form for applications at low load capacitance are: i) the shot noise from the base current of the input BJT; ii) the parallel noise from the feedback resistor of the preamplifier, which in the present version is chosen to be $R_F = 100$ kΩ; iii) noise contributions from stages in the chip which follow the preamplifier, mainly from the non-uniformity of the pipeline. The series noise contributions coming from the transconductance of the BJT and its base spread resistance R_{bb} are relatively small in the case of small load capacitance of pad sensors. It is planned to use pad sensors with either 2 mm $\times$ 2 mm or 1 mm $\times$ 1 mm pad size with respectively 512 and 2048 cells for the final HPD for the LHCB RICH detector. The load capacitance of one pad will be between 2 and 3 pF. For this case one can estimate that one can achieve a total noise of about 350 to 400 e^- ENC at 25 ns shaping time.

With a collector current of 25 μA, implementing a feedback resistor of 200–300 kΩ (the feedback capacitance has to be decreased accordingly in order to maintain the same shaping) and increasing the gain of the first stage by a factor 3, one can calculate the expected noise contributions of this circuit optimally adapted to low load capacitance. The parallel noise will be around 250 e^- ENC and the series noise around 220 e^- ENC. The noise slope expected for a collector current of 25 μA is calculated to be about 73 e^-/pF. This will result in a total noise of about 350 e^- ENC which is largely sufficient to get a very good single photoelectron separation even at 15 kV acceleration voltage. Figure 16 shows a measurement of the noise with zero load capacitance measured with the preamplifier shaper test circuit as a function of the collector current (stars). It drops from 700 e^- ENC to 500 e^- ENC when decreasing the collector current from 220 μA to 25 μA. The dotted

line in Fig. 16a represents a calculation for the present circuit, the full and dashed lines are predictions for a chip with $R_F = 200$ kΩ and increased voltage gain (about a factor 3) for β_{DC} values of 120 (typical value before irradiation) and 60 (typical value after 10 Mrad). Figure 16b gives the same prediction including the series voltage noise caused by a 2 pF load.

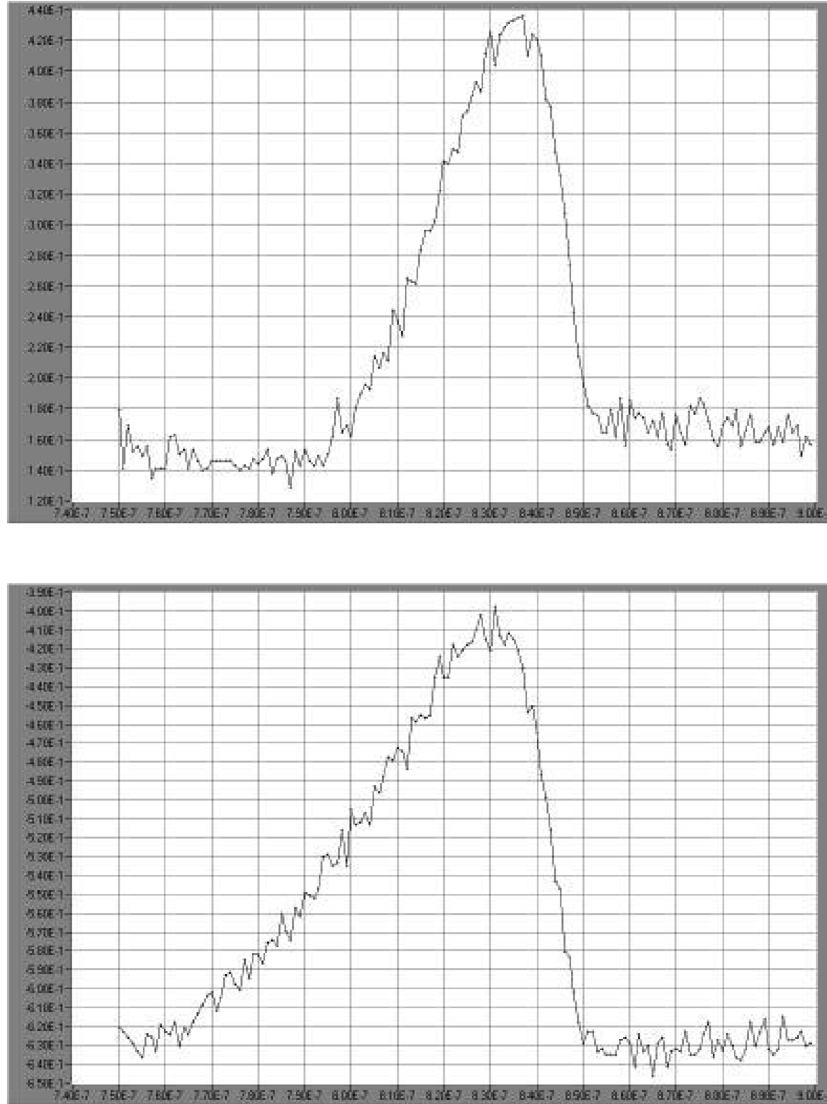

Figure 14: Pulse shape at output of shaper of fast LHC type amplifier (a) non-irradiated (b) after 10 Mrad with ^{60}Co Source. (Note: time goes from right to left.)

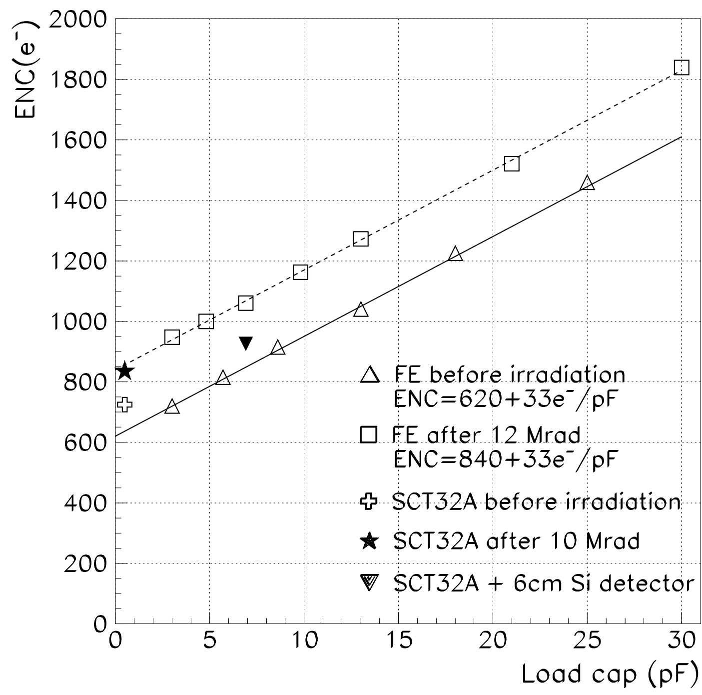

Figure 15: Noise as a function of capacitance load for fast amplifier.

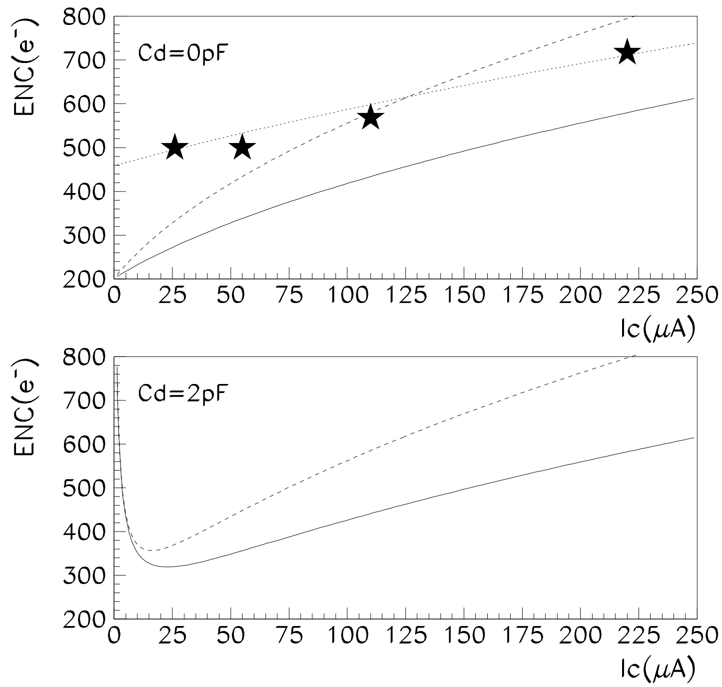

Figure 16: Noise as a function of collector current in input BJT of fast amplifier.

7 CONCLUSION

It has been demonstrated that single photoelectrons from a CsI photocathode can be observed with a 128 cell pad detector equipped with a low noise strip detector readout chip as a sensor for electron detection without background. At 15 kV acceleration voltage the single photoelectron peak is separated from the pedestal by 15 σ_{noise}. The observed charge deposition from single p.e. is in excellent agreement with w = 3.62 eV per electron-hole pair. It is shown that similar performances can be obtained with 25 ns shaping time pipeline readout electronics which is developed for LHC Si tracker readout. A prototype readout chip developed for the ATLAS Si tracker and an existing 484 cell pad detector with 1 mm^2 pads will be used to make first measurements of single photoelectrons with LHC speed electronics.

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