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ABSTRACT

Highly integrated readout electronics were developed and produced for the 182,000 channels of the four TPCs of the NA49 heavy-ion fixed target experiment at the CERN SPS. The large number of channels, the high packing density and required cost minimization led to the choice of a custom electronics system. The requirements, the design and the performance of the electronics components are described.

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1. Introduction

The NA49 collaboration studies nuclear matter under extreme conditions of temperature and pressure. The goal is the observation and study of the phase transition between hadronic matter and the quark–gluon plasma (QGP), a deconfined state of freely propagating quarks and gluons. The tool for studying high energy density nuclear matter in the laboratory is the collision of heavy nuclei at very high energy [1]. Successful programs at the Brookhaven AGS and the CERN SPS have been carried out using heavy ion projectiles at relativistic energies. Recently, the CERN accelerator complex was upgraded to accelerate lead beams to 160 GeV/nucleon, supplying for the first time collisions of the heaviest ions at this energy.

The NA49 experiment was designed specifically to study central collisions of lead nuclei at the SPS. The complexity of these collisions is unprecedented in accelerator–based nuclear and high energy physics experiments: each central collision produces up to 2000 secondary particles. While this environment presents a significant experimental challenge, it also presents a unique opportunity. Because of the very high multiplicity, measurement of a large fraction of all produced charged hadrons in each event will allow statistically significant analysis *event–by–event* of many of the possible signals of the QGP phase transition: $<p_T>$, slope of the p_T spectrum, K/π ratio, event-by-event Hanbury-Brown Twiss (HBT) correlations, etc [2]. This necessitates a very large acceptance spectrometer with good momentum and particle identification capabilities for charged hadrons. These are the fundamental requirements of the NA49 detector.

Because of the very high track densities in these collisions, previously used projective measurement techniques for large acceptance spectrometers, such as the streamer chamber used in the NA35 experiment [3], are not applicable. The natural choice for three–dimensional imaging of very complex events is the Time Projection Chamber (TPC) [4]. The ability of TPCs to track in the heavy ion environment has been demonstrated by NA36 [5] at CERN and by E810 [6] at the AGS. Particle identification, however, can not be performed in the traditional way by reading out the wires. A new approach was developed by the NA35 [7] and EOS [8] collaborations to use a very large number of contiguous pads for tracking and to perform particle identification by measuring the mean energy loss <dE/dx> . Cost constraints and the necessity to limit the number of cables carrying the signals away from the detector in a magnet led to two new developments: the use of custom integrated circuits (first for the analog storage only) and digitizing and multiplexing all the signals on the detector into a few optical fiber cables. This type of detector with a new approach to electronics has been successfully used in high energy heavy ion collisions, and with the appropriate choice of gas works well both within [8] and outside [7] of a magnetic field. Recent dramatic progress in silicon chip technology and computing techniques makes the readout and storage of data from a very large number of electronics channels feasible from the points of view of both engineering and cost [8,9].

Particle identification over a large part of phase space for fixed target experiments

at the SPS energy can be performed by the combined measurement of particle momentum and specific ionisation in a gas in the relativistic rise regime [10]. However, this places stringent demands on the pulse height resolution (4 %), requiring a track length of over 3.5 m.

There are four TPCs in NA49 (Fig. 1). Two Vertex TPCs (VTPC1, VTPC2), are situated within large dipole magnets, and two Main TPCs (MTPCL, MTPCR), are situated downstream of the magnets. The electrons generated by ionizing tracks passing through the TPC gas are drifted in an electric field upwards to the TPC readout chambers, where they are amplified. The signals measured on small cathode pads are induced by the charge on the adjacent anode wires. Each pad is connected to a separate electronics channel. Two spatial dimensions of the measurement are obtained from the pad location, and the third is obtained by measuring the electron drift time through sampling of the waveform on the pad. Spread of the signal over several pads and time slices is due to diffusion in the gas, the pad response function (charge amplified near a single anode wire induces signals on several pads), and the shaping of the signal by the electronics. This spread allows position interpolation to much better spatial resolution than the pad or time bucket size.

Detailed discussion of the design of NA49 and requirements for the TPCs will be given in a forthcoming publication [11]. Gas choice, readout chamber design and pad design were optimized for the varying tracking environments within each of the TPCs. For mechanical reasons, each TPC readout region is subdivided into sectors. Wire and pad geometries within a sector are optimized for the environment in that part of the chamber. Parameters of the NA49 TPCs are given in Table 1.

The characteristics of the readout electronics should match the response of the chambers, for instance with time constants compatible with the drift and diffusion characteristics of the gases and noise low enough not to contribute to the spatial resolution. A common electronics design that satisfied the need for low noise, good linearity and dynamic range was used in all TPCs. The need for good pulse height and momentum (position) resolution required development of an extensive calibration and monitoring system for the electronics. In total, the NA49 experiment incorporates 182,000 channels of TPC readout, each 512 time buckets long. A raw event from the NA49 TPC has a data volume of 93 MBytes. Data are compressed via zero suppression before recording on tape, resulting in a recorded event size for central lead-lead collisions of 8-10 Megabytes.

Construction of the NA49 experiment was completed and data taking with the full apparatus was begun in November 1995.

2. Requirements of TPC Electronics

The most stringent requirement on the density of the electronics is imposed by the VTPCs in the magnetic field where a density of up to 32 pads per 40 cm^2 is reached. The total height of the front-end printed circuit board and cabling is restricted by the need to fit into the 15 cm gap between the VTPCs and the magnet coil. This

density of electronic channels is achievable through large scale integration. Extensive developments [8, 7, 12] have resulted in a design in which the analog signal is digitized on-chamber, with multiplexing reducing the data path to a small number of optical fibers bringing the signal from the chamber to the counting house.

Matching of the diffusion characteristics of the gases, reasonable drift velocities, and overall length of the drift volume lead to a shaping time constant of 180 ns, a clock frequency of 10 MHz, and 512 time samples per pad to cover the 50 μs drift time. Pulse shape over the full dynamic range should be symmetric and Gaussian, with stable return to baseline, for optimal single and two-track resolution. Long term under- or overshoot should be below 0.2 % to avoid systematic shifts in measured pulse height (and corresponding deterioration of dE/dx resolution) as a function of total integrated charge in an electronics channel. Channel-to-channel gain variation after calibration should be less than 2 % in order not to contribute to the resolution of the dE/dx measurement.

The requirement for the single pulse dynamic range is governed by several factors and is coupled to the noise level. Only singly charged particles need to be measured. Tracking studies show that good momentum (position) and two–track resolution are achieved by a 30:1 signal–to–noise ratio for the most probable energy deposition of a minimum ionizing track passing over the center of a pad. The noise must be kept as low as possible to achieve this resolution while operating the chambers at low gain, which enhances stability. The pulse height increase due to the relativistic rise requires a factor of 1.4 in dynamic range. Landau fluctuations in the gas require a factor of about 4. The product of these factors results in a needed dynamic range relative to the noise level of about 170. Given the achieved noise level of 1100 electrons equivalent at input (see below), or equivalently 1.6 ADC counts at output, digitization of the signal to 8 bits gives sufficient dynamic range.

Detailed simulations of the TPC response show that a differential nonlinearity of about 1 % over the dynamic range is sufficient for good position resolution and pulse height resolution.

Crosstalk between electronics channels should be below 1 %. Since the charge from a single track is shared over several pads and time buckets due to diffusion, the pad response function, and the shaping time, some level of "natural" crosstalk exists in the chambers. The traces connecting pads to the readout electronics map adjacent pads to adjacent electronics channels, therefore reducing the influence of electronic crosstalk.

Simulations using a representative event generator [13] show that up to 30 minimum-ionizing-equivalent tracks may pile up on a single pad in an event in the highest track density regions. This sets the requirement for the integrated dynamic range of the preamplifier over which good linearity must be maintained.

The overall speed of the electronics and rate of digitized data flow are driven by the requirement to record one million events during a four week beam period, resulting in a modest rate of about two events per second. Throughout the design of

the electronics and data acquisition system, multiplexing techniques have therefore been applied in order to reduce cost, by minimizing the number of components at the expense of the less critical signal handling and data acquisition time.

3. Overall electronics layout

The design of the components was driven by the requirements of resolution and noise performance. The overall design was governed by the needed large number of channels and large event size combined with a low event recording rate. With the chosen solution it was possible to produce the required large number of channels at low engineering and production cost, minimizing the number of components and data links through a high degree of data multiplexing. The design follows the readout structure developed for the EOS experiment [8]; a similar approach has been adopted by the STAR collaboration [12]. The structure of the NA49 readout electronics can be seen in figure 2. Signal amplification, shaping, storage and digitization of 32 TPC pads are performed on the front-end (FE) card that is directly mounted on the TPC pad plane. This minimizes the generation of noise and pick-up by limiting the trace for the analog signal to a maximum of 6 cm. The digitized data of 24 FE cards are then collected by a control-and-transfer (CT) board through flat cables, 0.5 to 1.8 m long. The data of all 768 channels are then multiplexed by the CT board into a fiber link, sending the data to a receiver board located in the NA49 counting house 20 meters away.

3.1. The front-end card

The front-end card is directly connected to 32 TPC pads by a single inline connector as seen in figure 3. Most of the electronics components are integrated into two custom designed chips. One contains the preamplification and pulse shaping stages (PASA) the other contains an analog storage device and the analog to digital converter (SCA/ADC). Each chip has 16 channels, the FE card therefore carries two PASA and two SCA/ADC chips. The schematics of the card and a photograph can be seen in figures 4 and 5.

3.2. The preamplifier

The design of the charge integrating preamplifier has been adopted from the EOS experiment TPC readout system [8] and has been integrated into a chip that performs both amplification and pulse shaping. The entire chip is built in the CMOS p-well, 2 micron, 2 poly, 2 metal process by Orbit[1].

Amplification is performed in an integration circuit with a 1.5 pF feedback capacitor. Instead of the usual feedback resistor a FET switch is used to discharge the feedback capacity. The event trigger opens the FET switch and starts the integration which continues for 50 μs, corresponding to the maximum TPC drift time. Since noise performance and dynamic range of the preamplifier are crucial for the entire

[1]Orbit Semiconductor Inc., 1215 Bordeaux drive, Sunnyvale, CA 94089

readout chain, special care has been taken to match the needs of a TPC detector readout. The equivalent noise charge (ENC) has been measured to be ENC=1100 $e_{r.m.s.}$. The dynamic range of the preamplifier is designed for 4200:1. Its conversion gain is 50 mV/fC .

3.3. The shaper amplifier

Major guidelines for the shaper amplifier design [15] are the creation of a near Gaussian pulse-shape of a defined width, low additional noise and optimum compensation for the long 1/T tail of the chamber signal. This is achieved by a circuit as shown in figure 6. Two 2-pole-integration sections are followed by a differentiation stage. The signal width (FWHM) is chosen to be 180 ns to match the diffusion width of the charge signal in the chamber gas. The feedback loop of the output amplifier performs the 1/T tail correction. The voltage gain of the output section is g=25 and its bandwidth is 20 MHz, to reproduce Gaussian waveforms of less than 200 ns width. Preamplifier and shaper characteristics are summarized in table 2.

3.4. The analog storage array

In order to perform three dimensional reconstruction, the signal output of the shaper has to be recorded both in amplitude and time. For the amplitude digitization and time sampling we follow the scheme developed by the EOS experiment [8]. The analog information is sampled and stored in a switched capacitor array (SCA). Following the event, each successive time bucket is then digitized in an ADC. Since the event rates in NA49 are rather low, flash ADC digitization is not needed, thereby avoiding the flash ADC's disadvantage of high power consumption and large surface needs on the silicon chip. The SCA, recently developed at LBL [16, 17], has several advantages over analog storage in CCDs: higher on-chip component density can be achieved, clock distribution is easier and heat dissipation is lower.

The SCA can be regarded as a series of 512 capacitors in parallel, with a sample and hold circuit for every capacitor. After an event has been triggered the signal from the shaper is directed into the capacitors at a frequency of 10 MHz, storing the charge at 100 ns intervals into successive capacitors. For a drift speed of 2 cm/μs this results in a spatial sample size of 2 mm. After storage has been completed, the sample and hold circuits are used to direct the charge from each capacitor into an ADC. This is done at a frequency of 100 kHz, limited by the ADC's conversion rate.

Sixteen of these arrays have been integrated into one chip. The size of a single capacitor is 1.5 pF, channel to channel variations have been measured to be less than 0.4 %. Power consumption per channel is 10 mW and the output noise is smaller than 0.6 mV at 10 MHz sampling frequency.

3.5. The ADC

The ADC is realized in CMOS technology on the same chip that houses the SCA. It is designed as a "Wilkinson" style, single slope ramp and counter, analog-to-digital

converter. To simplify the design both ramp and counter are shared by all 16 channels [18].

The digitized output has been designed for 12 bits but only the lower 9 bits are used in NA49. (8 bits have sufficient dynamic range for the signal. The additional bit is to accommodate the wide range of dc levels at the shaper output.) The data are reduced to 8 bits through pedestal subtraction on the receiver board (see Sect. 3.11). The conversion time per pulse is 10 μs; the conversion of all 512 time slices takes therefore about 5 ms. The nonlinearity of the ADC over its entire range has been measured to be 1.4 counts r.m.s. Its power consumption is about 7 mW per channel. Basic characteristics of the SCA/ADC chip are summarized in table 3.

3.6. FE card production and tests

All PASA and SCA/ADC chips were tested before being mounted on FE boards. Those tests included search for short circuits and other clear failure modes as well as performance measurements such as noise, crosstalk, linearity and saturation evaluation. About 40 % of both chips met all of those requirements.

The cards were then tested for a series of parameters at computer-based test stands. For the noise test the r.m.s. of the pedestal value was required to be σ <3.0 ADC counts. The average noise of all accepted cards was measured to be 1.6 ADC counts. Crosstalk between channels on a card was checked by sending a sequence of signals into every channel individually and rejecting cards with signals in adjacent channels. Average crosstalk of accepted cards was measured to be smaller than 0.3 % . The saturation of every channel was determined by sending a sequence of pulses of high amplitude (corresponding to about 3 times minimum ionizing particles) into every channel. All FE card channels were required to reproduce at least 10 such pulses.

The influence of leakage current on the preamplifier saturation was measured by comparing single high amplitude pulses early in time (around time bucket 100) to pulses of identical input amplitude late in time (around time bucket 400). A noticeable change in measured signal was a sign of preamplifier saturation. The criterion for card rejection was set at a difference of 5 % in amplitude.

The FE card nonlinearity can be determined by measuring signals of increasing amplitude for every channel. A card was rejected if a channel with a deviation of more than 1 % from linear was found. For the accepted cards the average deviations were smaller than $\pm$ 0.4 %.

3.7. Clock and gate distribution

A 25 MHz master clock and an "Event Gate" are generated in the counting house and distributed to all on-chamber electronics as differential ECL signals over equal-length flat ribbon cables. In this way the sampling of all 182,000 pad signals are synchronized ($\pm$ 1 ns). The event gate is actually synchronized with the clock (to avoid race conditions) and the phase shift between the real-time trigger and the distributed event gate is measured with a simple CAMAC TDC.

3.8. FE card cooling

An FE card dissipates about 2 W of heat in normal operation. Due to the large number of front-end electronics channels and the resulting integrated heat dissipation on the readout surface of the TPC, a cooling system was installed. It was required to prevent the electronics from overheating and to keep the temperature stable at the top of the TPC gas volume in order to minimize temperature dependent drift velocity and pulse height variations.

The system is realized as a cooling water circuit[2] connected to numerous copper plates inserted between every pair of rows of FE cards on the TPC sectors. The pressure of the water in the system is kept below atmospheric pressure to avoid water leakage. The water temperature is regulated in order to maintain stable conditions on the readout sectors. The TPC and water temperature are monitored by a slow control system and power to the electronics is automatically turned off when irregular values are detected.

3.9. The control and transfer board

The Control and Transfer (CT) boards collect the data from the FE cards. They reside in the experimental area close to the Time Projection Chambers. The maximum distance between CT board and FE electronics is 0.5 m for the MTPCs and somewhat longer (1.8 m) for the VTPCs because of geometrical restrictions in the magnet. Each CT board connects to 24 FE cards (768 pads) via flat ribbon cable and transmits the data off the TPC to the receiver boards. In addition, the CT boards provide the FE cards with power, over-current protection circuitry, and monitoring of all FE voltages. An on-board microprocessor is used for setting operation and test modes. For system diagnostics, the CT board can generate simulated data or enable charge to be injected by the preamplifiers. The schematics of the board can be seen in figure 7.

The CT boards provide the signals necessary for controlling the custom ICs (PASA and SCA/ADC) on the FE cards. The state machine used to produce these functions is implemented using Xilinx field programmable gate arrays (FPGA). The FE data are then multiplexed and shipped over the fiber optic link. The CT board continuously sends data to the receiver for a total transmission time of 62 ms, necessary to send the data of 768 pads at a speed of 62.5 MHz. The transmission speed is here limited by the write access time of the storage memory (DRAM) on the receiver board. The optical driver interface is the Advanced Micro Devices TAXI chip, AM7968. The Hewlett Packard fiber optic driver HFBR-1414 is used to drive the cable. It is capable of transmitting signals at 120 MHz. In addition to sending physics data, the CT board also transmits house keeping data. This includes the board ID, the type of event, the 32 bit event number, and the digitized values of all FE and CT board voltages.

For slow control, the CT board has an Intel 8044 microprocessor running Intel's BITBUS protocol. This uplink, running at a serial rate of 62.5 KHz, is used for

[2]Leakless Cooling Systems (LCS), M.Bosteels, CERN/EST, Geneva, Switzerland

configuring the board's operating mode and simulated data mode. In addition, it is utilized for resetting the 32 bit event counter, setting which channels of the preamplifier inject charge, producing artificial data patterns, and generating a local event gate. The modes of charge injections and artificial pattern are used for test and diagnostic purposes.

Slightly different boards were produced for VTPC, MTPC high (HR) and standard (SR) resolution sectors. 130 standard resolution boards were produced using multilayer technology, and 120 high resolution boards were fabricated using multi-wire technology. In order to test these boards, each CT board was connected to 24 FE cards and one receiver board. Software was written to generate events using BITBUS and to compare the outputs of the receiver board with expected results.

3.10. CT board power supplies

The power for the CT board and FE cards is supplied by custom made power supplies. They are built as one-slot VME cards residing in 6U-220, 21 slot, VME crates running VME-FB F6852 power supplies. One VME card is used for each CT board, connected by cables up to 16 m long. A card provides +5 V for the CT board and −2 V and +5 V for 24 FE cards. The power dissipation per board is 32.7 VA. The boards sense over-current on CT and FE boards and power is turned off for those channels if necessary. All VME crates (18 in total) are connected to a Macintosh computer via a Mac-VME V370 interface running LabVIEW software which simplifies power on and off operations and monitors the performance of the entire system. Monitor data are sent to the central NA49 slow control system at fixed intervals.

3.11. The receiver board

This board is a 9U size VME board that contains four identical channels, each receiving data from one CT board through an optical fiber link (figures 8 and 9). The receiver channels serve as data storage during the 5 second beam burst. For this purpose they have 32 pages of 512K×9 bits of input memory, where the information from 32 events can be stored. The data are received through a TAXI chip and then sent through a field programmable gate array (FPGA, Xilinx) at a speed of 6.25 MByte/s. This FPGA first reorders the pad data from its multiplexed format on the CT board to a more natural sequence of time and pad information. Because the SCAs on the FE-cards have a pedestal that may be different for each cell, an 8 bit pedestal memory is used to subtract this bias while data are passing through the FPGA. Since this subtraction can yield negative values, the 9th bit of the input buffer is used as a sign bit; the effective resolution of the data in the input buffer is therefore 8 bits.

A digital signal processor (Motorola DSP 96000) is used for zero suppression. It has two external ports, A and B, of 32 bit address and data width, fast on-board memory, and can be clocked at a speed of up to 40 MHz. Its A port is connected to the input buffer, its B-port to the output buffer, whose size is only 1 MByte, since data compression to less than 10 % of the original data volume can be reached for

central Pb-Pb events. For events with lower multiplicity this data reduction fraction will be higher. The data compression code is written in assembler language. Its basic principle is to scan the input memory looking for pulses in time (drift) direction, a pulse being defined as two adjacent time slices above threshold. Time slices before and after a pulse can be added to the output data stream. The number of these pre- and post-pulse time slices and the threshold can be varied in order to study the data compression and accuracy of the pulse information for different data analysis tasks.

Data compression by the DSP processor starts after the first event has been received, but can be performed until the end of the 20 s accelerator cycle, therefore allowing 20 s for the compression of 32 events received during the 5 s beam burst. However, DSP access to the input buffer is disabled while data are being received by that buffer.

Input buffer, pedestal memory and 1 MByte of output buffer on the receiver board are read and write accessible via VME bus, for board development and testing. An additional 3 MByte buffer is only accessible from the DSP processor and is used for pedestal and noise calculation. To reduce the size of the address space per board, only one 512K×9 bit input buffer memory window can be seen from VME at a time. This window can be moved to any of the 32 pages using a VME accessible pointer; therefore a receiver channel occupies only 4 MBytes of VME address space. Since the transfer speed through the receiver board is not exceedingly high, it is possible to use dynamic RAM for the bulk memories, thus reducing the cost of the overall system considerably.

The data from all the output buffers are collected within a VME crate by processors (Motorola 68040, MVME166) which then write the data into dual ported memory in a master VME crate through their VSB slave interface. Event building, steering of the entire data acquisition process and transfer to the tape unit are carried out in a processor that resides in the master VME crate. A more detailed description of the daq system can be found in [19].

4. The Calibration system

The size and complexity of the TPC electronics system requires a device that can monitor basic performance characteristics independent of the TPC operation. Such a system should be able to generate pulses similar to TPC signals that then pass through the entire amplification, storage, digitization and readout chain. It should be possible by using this device to measure the amplification gain and nonlinearity for every channel, record channel-to-channel timing differences and detect defective channels.

Both the amplification gain and timing measurement are crucial for the proper performance of the system. As the x-coordinate (horizontal, perpendicular to the beam) is determined from charge ratios on adjacent pads, gain variations affect the accuracy of that measurement. Assuming that this coordinate is obtained by calculating the weighted mean of three pads, an average gain uncertainty of 10 % would

lead to an additional error of about 0.2 mm in the x-coordinate at a pad pitch of 3 mm. An uncertainty of 10 ns in the drift time determination leads to an error of 0.2 mm in the y-coordinate (vertical).

The calibration system was realized as a pulser that injects a signal into the field wires of the TPC. This field wire pulse induces a charge signal on the pads in the same way a signal is generated when a charge cloud reaches the wire plane. A dedicated trigger is used for the readout of these pulser events.

The pulse shape of the artificial pulser signal should reproduce the TPC signal as closely as possible. Its shape is generated by a 12 bit digital to analog converter in combination with a 3 step RC network. The generated signal has been compared to TPC pad signals in order to optimize its shape.

A schematic layout of the pulser can be seen in figure 10. The pulser can generate signal amplitudes spanning the entire dynamic range of the preamplifier and shaper system of the pad readout electronics. The nonlinearity of the pulse amplitude generation has been measured to be less than 0.1 %. The time of the pulse with respect to the readout trigger and the number of pulses in a readout gate can be varied arbitrarily. Remote control of these different functions is performed via a BITBUS interface by an Intel i80c152 chip on the board of the pulse generator connected to an XVME-402[3] interface in a VME crate. During data taking, dedicated runs were carried out a few times a week devoted to calibration data.

To obtain a gain calibration all field wires were pulsed repeatedly with signals of a mean amplitude. The signals were recorded and an average gain value determined for every channel. The gain values were entered into a database and then used in the off-line analysis for gain correction. The spread of the gain values over all channels of one TPC follow a Gaussian distribution with a sigma of about 10 % . More detailed studies [14] show that these are primarily caused by manufacturing differences in the chip production of the preamplifier and shaper parts of the front-end card. Study of track residuals using laser tracks shows that an improvement of the position resolution of about 30 μm can be obtained when applying the gain calibration. This value is smaller than the gain variation value of 10 % would lead one to expect. It can be explained by the distribution of the gain values: because sixteen adjacent channels reside on one chip, the average variation between adjacent pads is relatively low (around 1 %) thus leading to only small distortions in the position determination unless a chip boundary is crossed.

All channels within a TPC detector receive the pulser signal at the same time, so that the determination of the signal time for every channel can be used to correct for channel-to-channel time variation in the readout. Time variations of up to 50 ns are seen within a TPC detector corresponding to half a time bucket or about 1 mm drift. They are primarily caused by differing delays in the clock distribution to the front-end cards. Time differences within channels of the same front-end card are relatively small (< 5 ns). The values of these time calibrations are entered into a database and

[3]XVME-402 Bitbus controller, XYCOM, Saline, Michigan 48176

then used as corrections for the time information in the off-line analysis.

To determine the linearity of the front-end electronics, events of 16 different pulser amplitudes were taken. The amplitudes ranged from 40 to 180 ADC counts. The average deviation from a straight line fit for all channels in VTPC2 is shown in figure 11. The maximum deviation is about 0.6 %. Similar results were obtained in the other TPC detectors. Given this small value no correction for the nonlinearity is applied in the data analysis.

5. The NA49 run in 1995, Performance of the system

The full electronics system went into operation for the 1995 run when the entire NA49 TPC apparatus first took data. The total number of channels read was 182,016 corresponding to the number of pads on the readout planes of the TPCs. Each VTPC has 27,648 pads. The MTPCs have 63,360 pads. Accordingly, 5,688 FE cards, 238 CT boards and 60 receiver boards are needed.

The time to read one event from all FE cards into the receiver board memory was measured to be about 65 ms, dominated by the transfer time from the CT board to the receiver. Under normal running conditions of the experiment 32 raw events could be filled into the input buffer of the receivers during the 5 s beam burst. The 20 s accelerator cycle allowed up to 600 ms for the event zero suppression, which in fact required less than 300 ms. The average event size for central Pb-Pb events was determined to be 8.5 MBytes, which compares to the raw event size of about 90 MBytes, thus a data reduction of 10:1 was achieved. About 800,000 events were recorded within 4 weeks of data taking in 1995.

During the run pedestal data were taken about once a day. As these pedestal data are subtracted on line from the incoming data, it is important to ensure that variations in pedestal values are small between those pedestal runs. During a pedestal run 30 beam-off events were taken for all pads and time buckets, the mean values calculated by the DSP processors, and the resulting values stored in pedestal memory. At the same time the square-root of the variance (sigma) as well as the pedestal values themselves were written to mass storage. This variance over the very short period of time of 30 events is due to noise, so that these values can be used to estimate the noise of the electronics and TPC chambers.

The change of pedestal values between the measurements was small: an average change for all channels of 0.2 ADC counts was measured over a period of 24 hours. The average noise on the pedestal values for all channels was measured to be σ = 2.1, slightly greater than the value obtained from electronics bench tests (σ= 1.6), indicating that additional noise sources are present when the equipment is installed on the chamber. Additional noise is seen in the first four time buckets (400 ns), caused by the switching of the TPC gating grid voltage. Here the σ-values can be as high as 4.0 .

Figure 12 shows a pad signal as recorded by a sequence of 512 samples of ADC information. Pedestal values are subtracted online, and the zeros suppressed through

data compression. Every signal represents a charge cloud reaching the sense-wires and inducing charge on the pad. The data shown span a drift time of 51 μs, corresponding to about 110 cm in the MTPC.

To study the pulse-shape in more detail, pulses of similar amplitude, similar drift time and similar phase between peak position and clock were averaged. Pedestal subtraction was turned off when these data were taken in order to study both positive and negative signal amplitudes. Subtraction of previously measured pedestal values was then performed off-line. Figure 13 shows the pulse shape as measured in the MTPC. The shape is averaged over several hundred pulses. An asymmetric, near Gaussian signal can be seen. The small undershoot at the pulse end is caused by the compensation circuitry for the long 1/T tail of slowly drifting ions. The signal apparently returns to the baseline after the pulse although the precision of the measurement is not high enough to determine this with high accuracy. This effect is smaller than 1 ADC count and has no influence on the tracking performance, but may degrade particle identification capabilities at high drift length and track density. Work is in progress to determine this more quantitatively.

Analysis of VTPC data show saturation effects in the high track density region close to the beam. This manifests itself as loss of signal at large drift distances. This can be explained by the accumulation of a lot of charge due to spiraling electrons. It could be verified that the total charge accumulated before saturation corresponds to the charge equivalent of about 30 minimum ionizing particles.

A raw data display from all readout sectors of MTPCR is shown in figure 14. The grey level of a pad represents the charge accumulated on that pad. For the selected display, integrated charge between time slices 224 and 288 are shown. Taking into account the drift speed, this corresponds to ionisation generated by charged particles around the mid plane of the detector. Tracks pointing back to the target and traversing the entire TPC can be seen.

6. Conclusions

Electronics were built to read the signals from 182,000 pads of the NA49 TPCs. Each component and the overall system were designed in order to match the needs of a TPC detector and to fulfill the NA49 goals as a heavy ion experiment. Special care was taken to simplify the construction of the very large number of channels. Amplification, pulse-shaping and digitization are performed in components that are directly mounted on the chamber. The required event rate is low, which allows the data to be highly multiplexed in order to reduce the number of transfer links. VME modules were custom designed to perform fast pedestal subtraction, store the incoming data during the beam burst and perform zero suppression between spills. The entire system was successfully used in a Pb-Pb run at the CERN SPS in fall of 1995. First data from that run indicate that the system operated according to the design specifications.

7. Acknowledgments

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TPC:	VTPCs		MTPCs	
Length:	260 cm		384 cm	
Width:	200 cm		384 cm	
Height:	72 cm		129 cm	
Drift distance:	69 cm		115 cm	
Drift voltage:	13 kV		16.5 kV	
Gas mixture:	Ne/CO_2		$Ar/CH_4/CO_2$	
Gas composition:	91/9		91/4.5/4.5	
	VTPC1:	VTPC2:	HR:	SR:
Sectors per TPC:	6	6	5	20
Pad-rows per sector:	24	24	18	18
Pads per pad-row:	192	192	192	128
Number of pads/sector:	4,608	4,608	3,456	2,304
Pad width:	3.0 mm	3.0 mm	3.13 mm	4.95 mm
Pad length	16 mm/28 mm	28 mm	39 mm	39 mm
Gap sense-wire/pad-plane:	3 mm	2 mm	2 mm	3 mm
Number of pads per TPC:	27,648		63,360	
Total number of pads:	182,016			

Table 1: Main parameters of the NA49 TPC detectors. The MTPC detector has sectors with different pad size: high resolution (HR) and standard resolution (SR).

Number of channels/chip:	16
Preamp gain:	50 mV/fC
Preamp noise (ENC):	1100 $e_{r.m.s.}$
Nonlinearity:	< 2 %
Shaper signal width (FWHM):	180 ns
Tail correction:	1 % at 1 μs
Power consumption:	30 mW/channel

Table 2: Parameters of preamplifier and shaper (PASA) chip.

Number channels/chip:	16
Number of SCA time slices:	512
Sampling frequency:	10 MHz
Readout frequency:	100 kHz
Capacitor size:	1.5 pF
Gain variation:	< 0.4 %
ADC type:	Wilkinson
Conversion time:	10 μs
Range:	12 bits, 9 bits used in NA49
Power consumption:	20 mW/channel

Table 3: Parameters of the SCA/ADC chip.

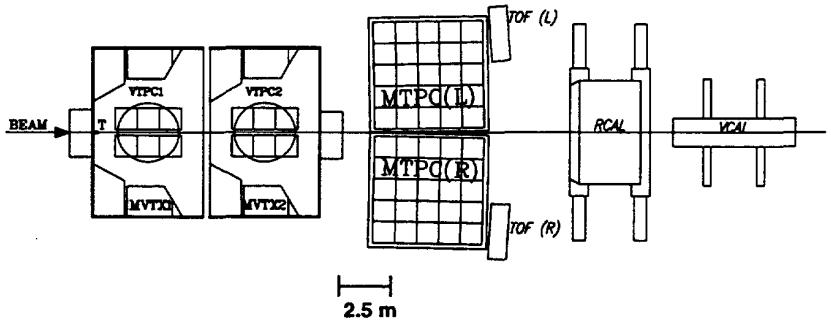

Fig. 1: Schematic layout of the NA49 experiment. The SPS beam impinges from the left on the target at point T. The Vertex TPC detectors VTPC1 and VTPC2 are installed inside dipole magnets. The Main TPC detectors MTPCR and MTPCL are located behind the second magnet. Behind the MTPCs are time-of-flight walls, followed by the Ring Calorimeter (RCAL) and Veto Calorimeter (VCAL). The VCAL signal is used to define the event trigger.

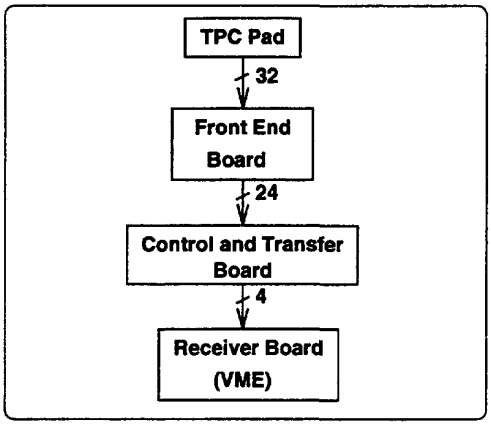

Fig. 2: Overall layout of NA49 TPC electronics from readout pad to VME board. All components up to the Control and Transfer Board reside on the chamber, and are connected via optical fiber to the Receiver Board in the counting house.

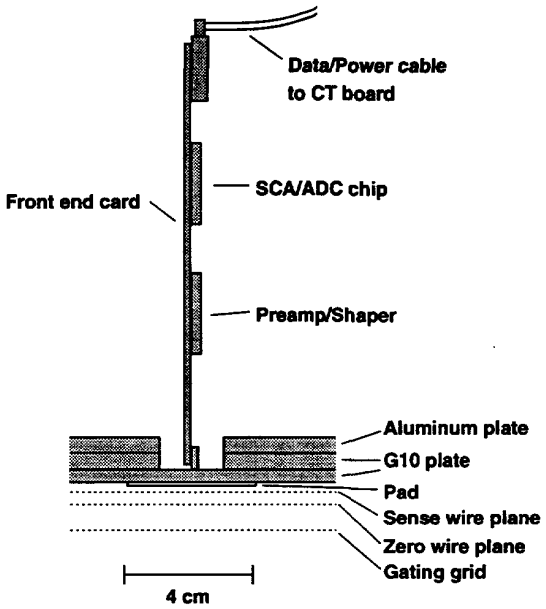

Fig. 3: Schematic drawing of the connection of a front-end card to the pads on a TPC sector.

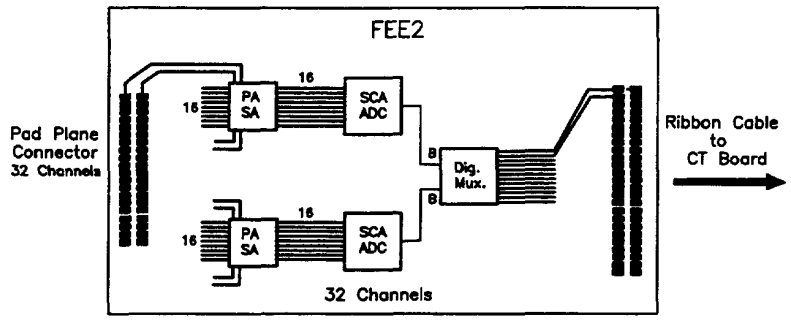

Fig. 4: Schematic layout of the front-end card. The PASA chip contains the preamplification and shaping stages. Analog storage and digitization are performed in the SCA/ADC chip.

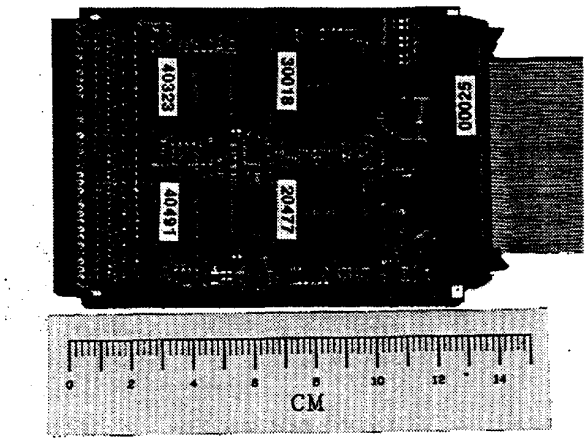

Fig. 5: Photograph of the NA49 front-end card. The two preamplifier shaper (PASA, left) and SCA/ADC (right) chips can be seen. The left connector plugs into the TPC readout plane, the cable on the right goes to the CT board.

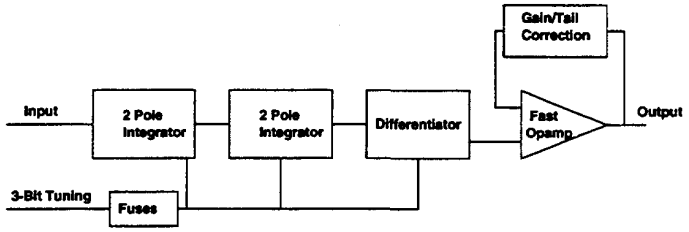

Fig. 6: Schematic layout of the NA49 shaper amplifier. The 3 bit fuses were used during the design for pulse shape tuning; due to high time constant homogeneity they were not modified during the production.

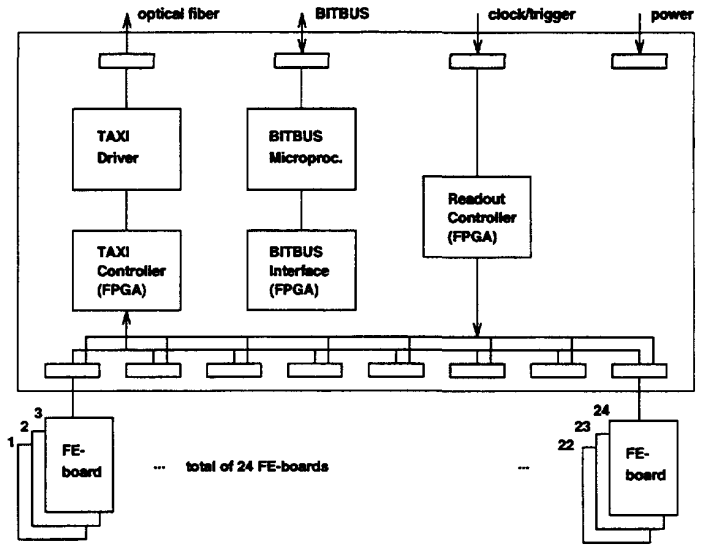

Fig. 7: Schematic layout of one CT board. Up to 768 pads are read out by one CT board.

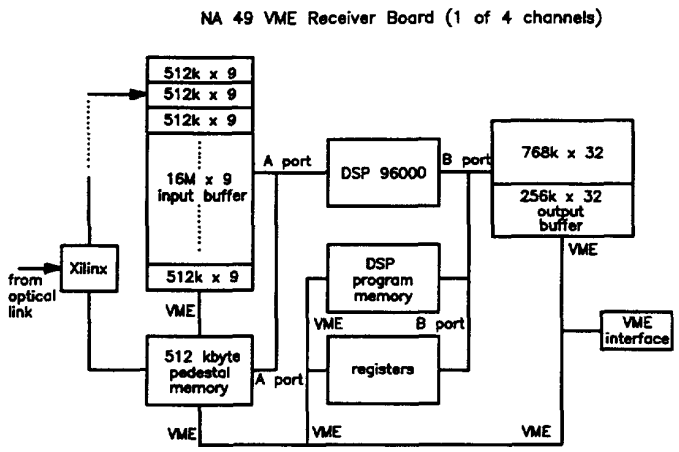

Fig. 8: Schematic layout of one receiver channel. VME access to memory on the board is indicated, as is access by each of the two external ports of the DSP, A and B. Each receiver VME board comprises four such channels.

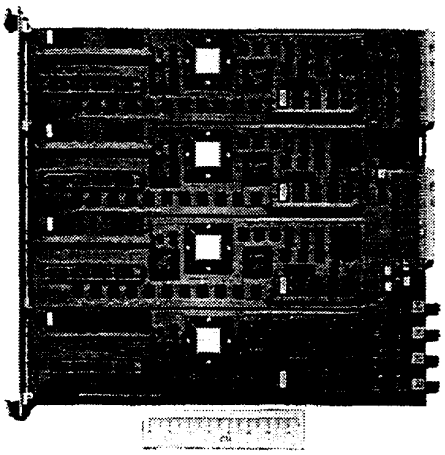

Fig. 9: Photograph of the NA49 receiver board. It carries 4 receiver daughter boards. The central chip is the Motorola DSP 96000 processor. The two large connectors on the right plug into the VME backplane. The small connectors on the lower right connect into the fiber links from the CT boards.

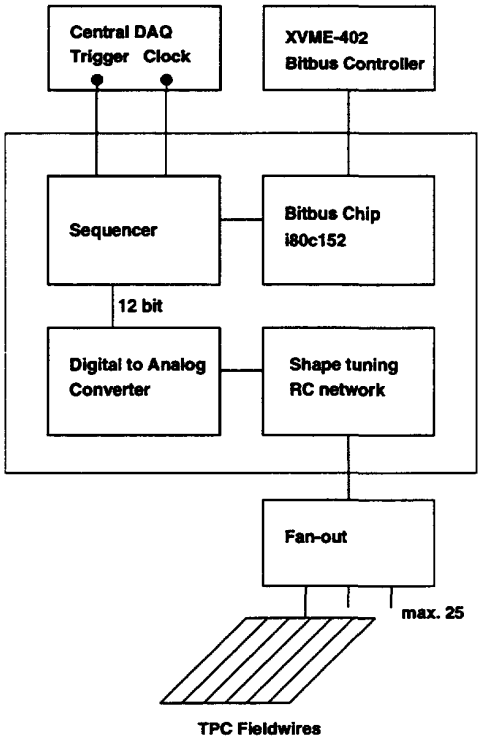

Fig. 10: Schematic diagram of the NA49 calibration pulser electronics. One of these pulser boards is used per TPC detector, driving field wire planes of up to 25 sectors.

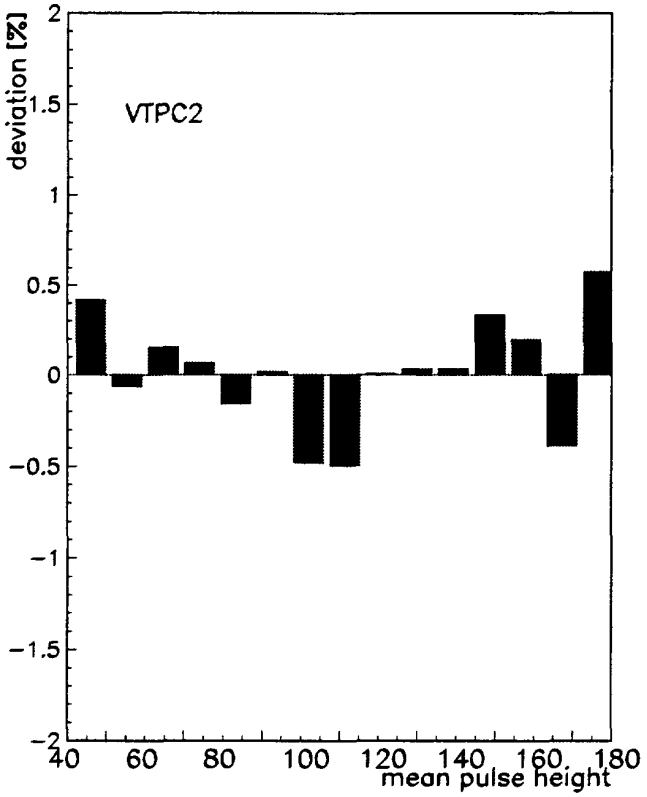

Fig. 11: Linearity determination of electronics in the VTPC2 detector. Deviations from a straight line fit averaged over all electronics channels are less than < 0.6 % . Statistical fluctuations are low (< 0.03 %); variations can be explained by differential non-linearities of the ADC [18].

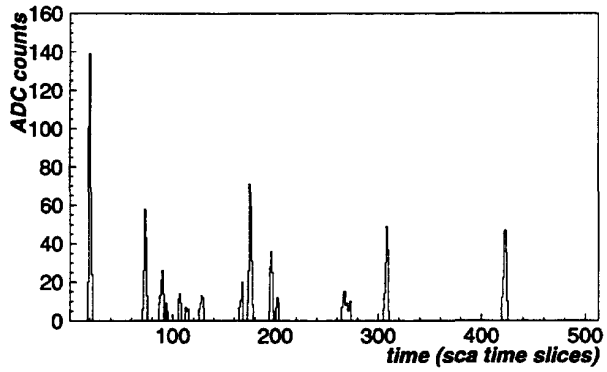

Fig. 12: ADC output as measured on one pad after pedestal subtraction. One time slice equals 100 ns.

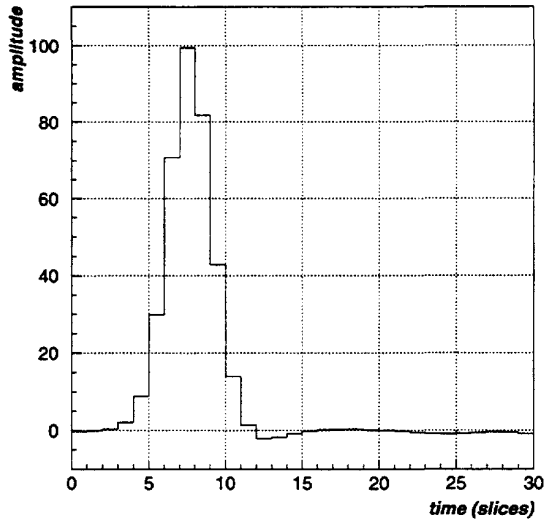

Fig. 13: Pulse shape measured for high-resolution (HR) pads in the MTPC averaged over many events of similar amplitude and similar phase with respect to the time slice. The undershoot following the pulse is caused by the tail correction circuit. One time slice equals 100 ns.

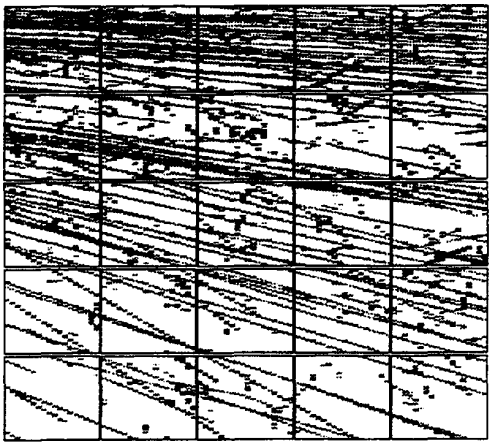

Fig. 14: Raw data display of MTPCR showing integrated charge between time buckets 224 and 288 (approximately at beam height). The beam is incident from the left and the target resides approximately 9 m upstream of the front face of the TPC.