Continuous Diagnostics for Powered Superconducting Circuits

T. Podzorny[®], M. J. Bednarek[®], M. B. B. Christensen[®], D. Calcoen[®], R. Denz[®], J. Ludwin[®], J. Steckert[®], and J. Uythoven[®]

Abstract-Monitoring the electrical properties of superconducting devices in their unpowered state has proven essential for commissioning and fault diagnosis during LHC machine operation. Furthermore, continuous diagnostics of powered superconducting circuits in an operational or test environment has the potential to further improve the understanding of existing and possibly ageing facilities. In this paper, we demonstrate that the injection of a very low power and arbitrary stimulus allows continuous monitoring of the electrical properties of a superconducting magnet through all phases of powering. We compare the performance of this novel measurement system in three different states of a superconducting magnet: unpowered, during current ramping, and at a steady operating current. In addition, we compare the new method with the currently used diagnostics of the LHC superconducting magnets for the unpowered devices. Our results indicate that the presented method provides comparable results to the reference system, while allowing continuous probing of the energized superconducting device over extended periods of time.

Index Terms—Accelerator magnets, impedance, measurement and testing.

I. INTRODUCTION

I MPEDANCE measurements have a wide range of applications in various domains, particularly in diagnostics. An obvious example is the electronics industry, where impedance analysis is used to characterize electronic components and materials, serving as an essential tool for quality assurance. Impedance characterization as a function of frequency provides essential insight into battery health monitoring. In medical imaging, electrical impedance tomography enables real-time imaging of the lungs, breast, and brain, while bioimpedance analysis allows the assessment of body composition and tissue health.

Monitoring the electrical properties of superconducting devices in a de-energized state has proved essential for commissioning and fault diagnosis during the operation of the LHC

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T. Podzorny, M. J. Bednarek, D. Calcoen, R. Denz, J. Steckert, and J. Uythoven are with CERN, 1211 Geneva, Switzerland (e-mail: tomasz.podzorny@ cern.ch).

M. J. Bednarek is with the European Organization for Nuclear Research, 1211 Geneva, Switzerland, and also with Aalborg University, 9220 Aalborg, Denmark.

J. Ludwin is with the Institute of Nuclear Physics, Polish Academy of Sciences, 31-342 Krakow, Poland.

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machine [1], [2], [3], [4], [5], [6]. Regular and ad-hoc measurement campaigns have become vital for the electrical quality assurance of the LHC's superconducting circuits. These campaigns have been particularly important for confirming electrical faults and deciding whether to initiate repair actions, especially those involving the opening of the cryogenic assembly. Recent work by Janitschke et al. [7], [8] suggests that comprehensive models of operating superconducting magnets and routine monitoring could facilitate early detection of non-conformities in superconducting circuits. Ludwin et al. [9] showed that impedance monitoring during a quench of the superconducting magnet can improve the diagnostics of these elements.

Continuous impedance monitoring as a function of frequency in powered superconducting circuits, particularly during different operating phases, has the potential to further improve our understanding of the effects occurring in these circuits. These changes are anticipated because, during powering, phenomena such as persistent currents and magnetization, interstrand and inter-filament coupling currents, and eddy currents in the conductor occur [10], [11]. These effects depend on the magnetic field amplitude, and are known to directly influence AC losses, and thus by extension impedance. While AC loss has been studied extensively, a comprehensive exploration of impedance dynamics in superconducting circuits remains limited. Furthermore, previous studies have demonstrated that impedance changes, like those from helium permittivity shifts during heating, can be used for quench detection [12]. Beyond research applications, continuous impedance monitoring could also prove useful for preventive maintenance and early detection of emerging issues in large and aging facilities [13]. In this paper, we present a method and measurement system to facilitate research in these areas. The system allows for accurate, continuous monitoring of the impedance of superconducting circuits without the need to modify standard powering and protection schemes. Consequently, this technique is applicable to any superconducting device equipped with voltage taps for instrumentation.

II. IMPEDANCE MEASUREMENT IN POWERED CIRCUITS

Measuring the impedance of powered superconducting circuits presents significant challenges, primarily due to the need to ensure compatibility between the measurement signal and both the powering and quench detection systems. Standard impedance analyzers cannot isolate the magnet impedance from

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Fig. 1. Simplified block diagram of the measurement system. Note that only the ADC channels required for probing the impedance of half the magnet are shown. Line color coding: Ethernet, Timing Pulse, SPI and power converter communication, and internal (black); dashed lines indicate clock signals.

the combined system impedance of both the magnet and power converter impedances. They typically use signal levels that are relatively high compared to the feedback loop settings of power sources and the thresholds of quench detection systems. In addition, these analyzers often lack galvanic insulation and require a single-ended configuration with a connected ground terminal. Thorough characterization of a superconducting device requires either steady-state conditions or instantaneous impedance measurements over the bandwidth of interest, the latter being critical for real-time impedance measurements. However, typical impedance analyzers sweep the test signal across the bandwidth. Consequently, these factors limit the applicability of conventional impedance analyzers mostly to non-powered circuits.

In previous work, we proposed a method for monitoring the impedance of powered superconducting circuits [14], [15]. This innovative system has been designed to allow impedance measurements to be made without requiring modifications to standard powering and protection schemes, and is applicable to any superconducting device equipped with instrumentation voltage taps. It builds upon the foundational technologies of the Universal Quench Detection System (UQDS) [16], [17] and the Ethernet-enabled Data Acquisition System (EDAQ) [18], [19]. This system uses a new differential probing topology that allows the impedance effect of the power converter to be isolated from the magnet impedance measurements. The original implementation exclusively allowed one-shot measurements, limiting acquisition to approximately 650 ms in duration when sampled at a rate of 400 kHz.

A simplified overview of the implemented hardware chain, the probing topology, and the details of the data acquisition system is shown in Fig. 1. The AC-coupled stimulus injection front-end interfaces with two halves of the magnet using the middle and outer voltage taps. The probing configuration is designed to cancel the effective signal across the entire coil, thus isolating the effect of the power converter impedance on the measurement. This also ensures that the stimuli are not visible to the power converter instrumentation, thereby minimizing the impact on its operational feedback loop. The stimulus signal consists of a configurable number of superimposed sine waves. The phases of each of the sinusoids are optimized to maximise the power delivered while limiting amplitude peaks. The system measures voltage and current via dedicated AC-coupled channels optimized for bandwidth and input signal range. The responses obtained from the voltage and current instrumentation modules are processed to estimate their phase and amplitude at the selected frequencies using least squares estimation. The ratio of the estimated complex signals provides an estimate of the impedance at each of the selected frequencies [14], [15]. In general, this probing methodology can be applied to any powered device with exposed voltage taps and symmetric impedance. However, in this implementation, the limited maximum output current (90 mA) impairs the ability to measure low-impedance devices (e.g., a superconducting cable) due to the challenge of inducing a measurable voltage drop.

To enable continuous monitoring and analysis of dynamic changes in the properties of a superconducting device, we upgraded the data acquisition scheme. The data acquisition system consists of two functional blocks. The Field Programmable Gate Array (FPGA) block handles stimulus generation, free-running data sampling, and record memory that stores the collected samples. The microcontroller (MCU) block manages an Ethernet stack to transmit collected samples to an upstream server,

interfaces with the FPGA block, and controls the collection of samples in the FPGA record memory. This record memory consists of 32 registers (to accommodate up to 32 separate ADC channels), each with a word length of 32 bits. Nominally, the designed acquisition system allows for sampling the full record memory at a rate of 10 kHz. By optimizing the firmware, sampling rates of up to 15 kHz have been achieved. However, such a sampling rate is insufficient for high frequency impedance measurements, as it effectively limits the observable bandwidth to below 7.5 kHz. To overcome this limitation, we introduced an interleaver sub-module in the FPGA. As the impedance measurement system only uses 4 of the 32 channels available on the UQDS platform, the interleaver allows the recording memory to be segmented into 8 blocks (in the case of 4 channels used), each of which stores subsequent samples of the 4 channels. This improvement has increased the continuous sampling rate to a maximum of 120 kHz, effectively allowing impedance to be measured up to 60 kHz. In the presented implementation, it is important to note that higher sample rates increase the probability of missed samples. As previously discussed, the update frequency of the FPGA's record memory is governed by the MCU's sample clock, while the sampling frequency is controlled directly by the FPGA. Due to the lack of synchronization between these two clocks, the MCU may update the record memory before new ADC samples are available, resulting in duplicate samples. More critically, if the FPGA's sampling clock outpaces the MCU's update rate, samples may be entirely missed. To address these challenges and minimize the effects of non-uniform sampling, two strategies are employed: 1) The FPGA sampling frequency is set to the highest possible integer multiple of the MCU sampling frequency, up to a maximum of 500 kHz. This ensures that in event of a missed sample, the acquired sample will be spaced closer in time than if the two clocks were designed to operate at theoretical equal frequencies. To reduce aliasing effects, the ADC sampling in the FPGA is followed by an anti-aliasing filter that limits the bandwidth to half the MCU sampling rate. 2) Each sample of the four channels in the record memory is accompanied by a sample clock counter. This allows sampling irregularities to be detected and accounted for in post-processing when estimating the impedance [14], [15].

III. MEASUREMENTS AND VALIDATION

A series of measurements on the superconducting magnets under different operating conditions qualified the measurement method and equipment. Comparison with the system used for recurrent measurements of the LHC superconducting magnets served as a reference and allowed for calibration of the system in unpowered conditions [2] [4]. The impedance of one half of an MQXFS [20] quadruple magnet as a function of frequency for the reference measurements in the unpowered and two different powering scenarios is shown in Fig. 2. The MQXFS magnet was at a temperature of 4.5 K during the tests. The powering systems were disconnected during the reference measurements. The reference system used a single-frequency sinusoidal signal with an amplitude of 8 V. The frequency was swept from 1 Hz to 1 MHz with 20 points per decade. The developed system

Fig. 2. Comparison of impedance measurements obtained with the reference system and the differential system. The number in parentheses represents the number of samples used to compute the estimate for each corresponding trace.

operated in continuous acquisition mode with a sampling frequency of 100 kHz, using a 100 mV stimulus signal composed of 10 logarithmically spaced frequencies ranging from 1 kHz to 40 kHz. Despite the relatively sparse frequency coverage, the proposed method showed good agreement with the reference system.

For powered tests, the magnet was connected to a power converter regulating the current via the applied voltage. The quench protection systems remained active throughout the tests, and no false positives occurred. The distinct phases of the powering tests demonstrated that the impedance measurement does not interfere with the operation of the superconducting circuits. The average magnitude and phase of the acquired impedance during the current ramp from 1200 A to 2000 A, and during a steady current of 2000 A, are shown in Fig. 2. Both measurements are derived from several million samples. Although, the MQXFS magnet is rated for a nominal current of over 16 kA, these initial measurements were conducted at significantly lower currents. This precaution was taken to ensure safety, as the interaction between the injected stimuli and the quench detection systems was a subject of tests in the same measurement campaign. The measured impedance across these tests showed a high degree of consistency. To highlight the differences between the measurements, the relative magnitude compared to the reference system is shown in Fig. 3. Differences between the systems began to appear at higher frequencies in the impedance spectrum. These

Fig. 3. Comparison of the relative magnitude of the estimated impedances. Relative to the reference system measurements.

Fig. 4. Continuous impedance (magnitude) over time for each of the stimuli frequencies. Measured during a current ramp from 1200A to 2000A of two halves of an MQXFS magnet.

differences are attributed to variations in stray capacitance in the measurement setups, differences in the instrumentation cabling used, and the impact of mutual inductance, which depends on the probing topology [15]. A detailed evolution of the impedance magnitude during the current ramp from 1200 to 2000 A is shown in Fig. 4. The measurement serves as an example of a continuous and real-time impedance monitoring in the 1 kHz to 40 kHz spectrum over 80 seconds. The impedance evolution is shown second by second for each of the two halves of the magnet. Importantly, all associated systems operated nominally during continuous impedance acquisition. From Fig. 4, a significant amount of noise is evident. This noise could be reduced in future test campaigns by increasing the stimulus voltage, using a lower-noise power converter, or applying noise reduction techniques. Additionally, within the present noise level, no discernible change in impedance is observed during the current ramp from 1200 A to 2000 A. This suggests that future measurements should target a broader current range and incorporate noise reduction techniques to better capture any potential impedance variations.

IV. CONCLUSION

The demonstrated impedance measurement system enables a novel approach to monitoring superconducting devices in their operational state. In particular, the system is applicable to most superconducting magnets that have multiple voltage taps embedded in their structure. Importantly, the system showed no interference with powering and protection systems during testing, while providing measurement accuracy equivalent to the reference system under unpowered conditions. The newly introduced modifications allow for continuous impedance monitoring of the magnet over extended periods of time. A critical aspect of this system is its ability to capture the full bandwidth of interest in real time, allowing accurate tracking of impedance evolution during magnet powering.

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