The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

Design and construction of the Outer Tracker for the Phase-2 Upgrade

Irene Zoi for the CMS Tracker Group

Abstract

The High Luminosity LHC (HL-LHC) is expected to deliver an integrated luminosity of $3000 - 4000$ fb^{-1} after 10 years of operation with peak instantaneous luminosities reaching about $5 - 7.5 \times 10^{34}$cm^{-2}s^{-1}. During Long Shutdown 3, several components of the CMS detector will undergo major changes, called the Phase-2 upgrade, to be able to operate in the challenging environment of the HL-LHC. The current CMS silicon strip tracker will be replaced with a new detector. The Phase-2 Outer Tracker (OT) will have higher radiation tolerance, higher granularity, and the capability to handle higher data rates compared to the current system. Another key feature of the OT will be to provide tracking information to the Level-1 (L1) trigger, allowing trigger rates to be kept at a sustainable level without sacrificing physics potential. In this paper, the design of the CMS Phase-2 Outer Tracker, the technological choices, and the quality assurance (QA) procedures used to ensure the functionality of the modules are reported. Moreover, the results with kick-off modules used for validating and finalizing the hybrids design before the start of the production are presented.

Presented at *Pixel2024 Eleventh International Workshop on Semiconductor Pixel Detectors for Particles and Imaging*

Design and construction of the Outer Tracker for the Phase-2 Upgrade

I. Zoi on behalf of the CMS Tracker Group

Fermi National Accelerator Laboratory,
Batavia, IL, USA

E-mail: irene.zoi@cern.ch

ABSTRACT: The High Luminosity LHC (HL-LHC) is expected to deliver an integrated luminosity of $3000 - 4000$ fb^{-1} after 10 years of operation with peak instantaneous luminosities reaching about $5 - 7.5 \times 10^{34}$cm^{-2}s^{-1}. During Long Shutdown 3, several components of the CMS detector will undergo major changes, called the Phase-2 upgrade, to be able to operate in the challenging environment of the HL-LHC. The current CMS silicon strip tracker will be replaced with a new detector. The Phase-2 Outer Tracker (OT) will have higher radiation tolerance, higher granularity, and the capability to handle higher data rates compared to the current system. Another key feature of the OT will be to provide tracking information to the Level-1 (L1) trigger, allowing trigger rates to be kept at a sustainable level without sacrificing physics potential. In this paper, the design of the CMS Phase-2 Outer Tracker, the technological choices, and the quality assurance (QA) procedures used to ensure the functionality of the modules are reported. Moreover, the results with kick-off modules used for validating and finalizing the hybrids design before the start of the production are presented.

KEYWORDS: Radiation-hard detectors, Si microstrip and pad detectors, Solid state detectors, Particle tracking detectors (Solid-state detectors), Detector design and construction technologies and materials

Contents

1 Introduction

The Large Hadron Collider (LHC) [1] will be upgraded to the High-Luminosity LHC (HL-LHC) [2] during the LHC Long Shutdown 3 (LS3). The maximum instantaneous luminosity will be increased reaching up to $7.5 \times 10^{34} \mathrm{cm}^{-2} \mathrm{s}^{-1}$ and in the 10 years of data taking a total luminosity of $3000 - 4000 \ \mathrm{fb}^{-1}$ will be collected.

The Compact Muon Solenoid (CMS) detector [3] was initially designed for instantaneous luminosities of $1 \times 10^{34} \mathrm{cm}^{-2} \mathrm{s}^{-1}$ and an average of 20 to 30 simultaneous proton-proton collisions per bunch crossing (pileup). At the HL-LHC the pileup will increase to up to 200 collisions per bunch crossing. To cope with the increased pileup and radiation damage and to maintain high physics performance, the CMS detector will be significantly updated [4] as part of the so-called Phase-2 upgrade and the current silicon tracker will be entirely replaced. In particular, the outer strip tracker will have an unacceptable performance degradation beyond about $1000 \ \mathrm{fb}^{-1}$ [5]. This paper describes the key features of the new Phase-2 Outer Tracker (OT) modules.

In the CMS experiment, the amount of data received by the detector is too large to be completely stored on disk and a two-level trigger decision system is used. The first level, or Level-1 (L1) trigger, [6], based on custom-made fast electronics, decides at 40 MHz which events are interesting enough to be read out from the detector for further processing, based on inputs from some of the CMS sub-detectors. Simulations show that by using the current L1-trigger strategy, based on calorimeters and muon detectors, the overall trigger rates would be well above the allowed maximum L1 rate in Phase-2 of 750 kHz, implying a reduction in reconstruction performance. Instead, by including tracking information at L1 it will be possible to maintain trigger rates while maximising the physics potential of the upgraded CMS detector at the HL-LHC. An Outer Tracker p_T-module has two closely spaced silicon sensors read out by the same electronics. The 3.8 T solenoidal magnetic field of CMS allows to discriminate on particle transverse momentum (p_T) based on the curvature of their trajectories: only particles with high p_T (small curvature) will produce two closely separated hits on the two sensors, and generate a track segment, called a *stub*, which is identified by the module front-end electronics. The spacing between the two sensors depends on the location of

the module in the detector and has been optimized based on simulations to guarantee, in addition to a programmable acceptance window in the front-end ASICs, a consistent p_T threshold across the entire Outer Tracker volume [5]. A target p_T threshold of just under 2 GeV is sufficient to allow transmission of the stubs to the off-detector electronics at the full 40 MHz bunch crossing rate. Once the global L1 decision is made, the entire detector is read out at full granularity, including the Outer Tracker hits and clusters information. This data is buffered on detector for up to 12.5 μs before it is sent to the central Data Acquisition (DAQ) system to contribute to the second level trigger. The p_T-modules come in two different flavors: strip-strip (2S) and pixel-strip (PS) modules, which will be described in Section 2 and Section 3, respectively.

Another key improvement in the OT design is the reduction of the material budget compared to the current detector. This is achieved through the use of bi-phase CO_2 cooling, which allows for small-diameter low-mass tubing. Additional reductions are accomplished with DC/DC converters, improved service routing, and the tilted layout of a section of the barrel.

2   2S modules

2S modules are composed of two strip sensors with dimensions of $\sim 10 \times 10$ cm^2 divided into two rows of 5 cm long strips with a pitch of 90 μm. The design of the 2S module is shown in Fig. 1. For each row, both strip sensors are read out by 8 CMS Binary Chips (CBC) [9] which also reconstruct the stubs. Stubs and hit data are sent at 320 MHz to the Concentrator Integrated Circuit (CIC) [10], which aggregates data from the CBCs and performs clustering and zero suppression of the triggered data. Data are then sent to the Low Power GigaBit Transceiver (LpGBT) [11]. The LpGBT receives stubs and triggered data from the two halves of the module and sends them at 5.12 Gb/s to the Versatile TRansceiver plus (VTRx+) [12] which converts the data into an optical signal and transmits it to the back-end electronics. Fast commands (i.e. L1 accept, clock, reset) and slow commands are sent via fiber optics by the back-end electronics to the VTRx+ at 2.56 Gb/s, converted into an electrical signal, and passed to the LpGBT. The programming of the front-end chips is done via I2C using the LpGBT I2C functionality.
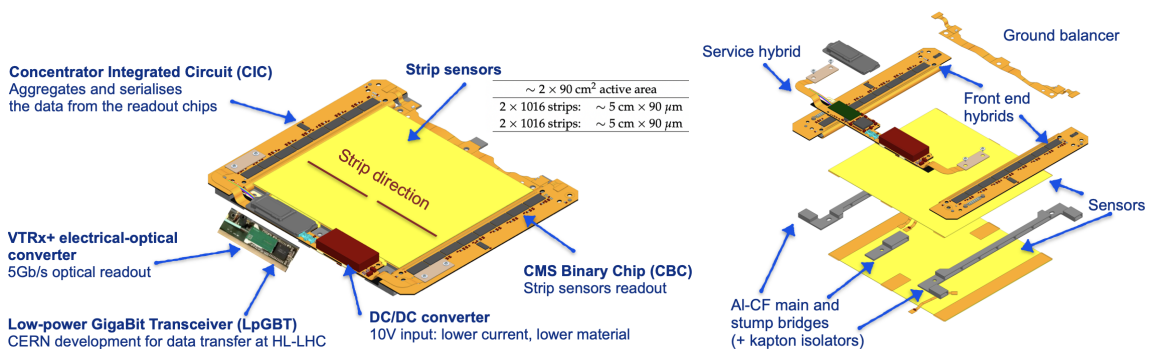

Figure 1. 2S module design (left) and exploded view (right).

The CBC and CIC ASICs are bump-bonded to Front-End Hybrids (FEH) which are located on the two sides of the module. The FEH is folded on itself and features wire-bonding pads for

the two sides of the module, allowing the CBC to read out signals from the top and the bottom strip sensors. Adjacent to the strips, the Service Hybrid (SEH) hosts the LpGBT and the VTRx+. On the same hybrid, a two-stage DC/DC conversion is used to transform the 10 V input to the voltages used to power the ASICs on the module. This feature reduces the current flowing to the modules, allowing for a smaller cross-section for the low voltage cables and therefore reducing the material in the tracking volume. A ground balancer is placed on the opposite side of the module to equalize ground and powering lines between the two FEHs. Strip sensor separation is provided by Aluminum-Carbon Fiber (Al-CF) bridges that are produced for 1.8 mm and 4.0 mm module thicknesses.

3 PS modules

PS modules are instead composed of one strip sensor and one macro-pixel sensor. A sketch of the PS module is shown in Fig. 2. The pixelated sensor (PS-p), located on the bottom side of the module, is 5×10 cm^2 in size. The PS-p features macro-pixels of ~ 1.5 mm $\times 100$ μm and is read out by 16 Macro Pixel ASICs (MPA) [14] bump-bonded to it. The strip sensor (PS-s) has the same dimensions, featuring two rows of 2.4 cm long strips with a pitch of 100 μm. Short Strip ASICs (SSA) [15] read out the strip sensor (8 per side) and send clustered hits to their respective MPAs which are then responsible for comparing them with pixel clusters in order to form stubs. MPAs then transmit strip and pixel clusters to the CIC once a L1 trigger is received. In PS modules, zero suppression and clustering are done by the MPA.
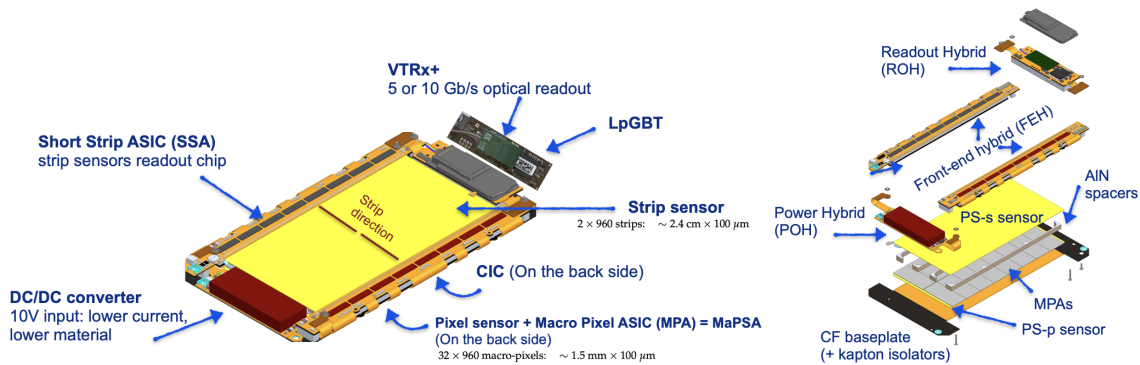

Figure 2. PS module design (left) and exploded view (right).

The rest of the readout chain is the same as on the 2S modules: data from the 8 MPAs reading one half of the module go to a CIC, which aggregates and forwards them to the LpGBT. Data are transmitted optically to and from the back-end electronics using the VTRx+. To cope with higher data rates in some parts of the detector, the PS module can be operated with the CIC transferring data at 640 MHz and the LpGBT operating at 10.24 Gb/s. Where lower data rates are expected, the PS module will operate at 5.12 Gb/s. SSA and CIC ASICs are located on the left and right front-end hybrids (FEH), while the LpGBT and VTRx+ are on the readout hybrid (ROH). PS modules are also equipped with a power hybrid (POH) hosting the DC/DC converters.

PS modules will be produced with three sensor separations, 1.6 mm, 2.6 mm, and 4.0 mm provided by aluminum nitride (AlN) spacers.

4 Module qualification and design finalization

More than 60 2S and 30 PS prototypes have been assembled across multiple production sites, allowing them to verify assembly procedures and control processes. Several tests have been performed on these devices to verify their functionality, both in the laboratory and with particle beams, both before and after irradiation up to end of life fluences. A complete set of quality control tests is implemented for the modules and their components [16, 17]. Module production sites are
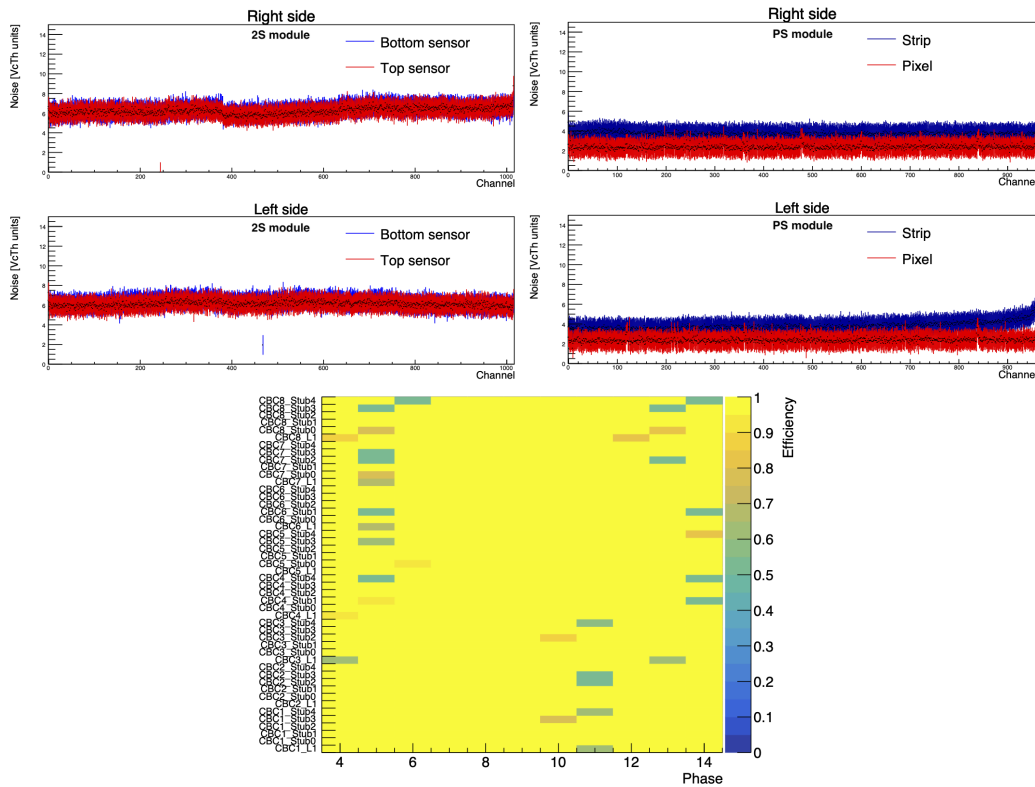

Figure 3. Top: an example of a noise measurement for each channel of a 2S (left) and a PS (right) module. Bottom: a scan of the CIC sampling phases on all 48 CBC data lanes on a 2S FEH. The phase steps are about 390 ps, corresponding to 1/16 of two 320 MHz clock cycles. Sampling phases where communication is error-free (yellow) and where errors are detected (non-yellow) are shown. A wide range of phases providing reliable communication is visible.

being equipped with dedicated test stands and burn-in setups for module qualification. All modules are required to go through multiple thermal cycles from room temperature to operation temperature (around -35°C) over 24 hours to screen for early-life failures. During this time modules will also undergo various calibrations, including noise measurements, communication tests between module ASICs and verification of the stub logic functionality. Examples of these measurements are shown in Fig. 3. Based on the results, the module will be graded and its characteristics stored in the

production database. These data will be then used to identify the best modules to be installed in the detector.

A dedicated set of prototypes, called *kick-off* modules, has been used to validate and finalize the design of the hybrids before the start of the production. In particular, two different layouts for the PS-POH and 2S-SEH were produced: a common ground plane variant that had a single ground layer for DC outputs and switching power currents (Common Plane), and a split plane variant that implemented separate DC ground and switching current ground layers, linked at a common point (Split Plane) [18]. Moreover, the introduction of a grounding balancer (GB) directly connecting the ground levels between the two 2S FEH, and the removal of an additional 'zigzag' powering tail (ZZ) connecting the PS-POH and the PS-ROH were investigated. For this exercise 21 2S modules and 14 PS modules were produced among the different assembly centers.
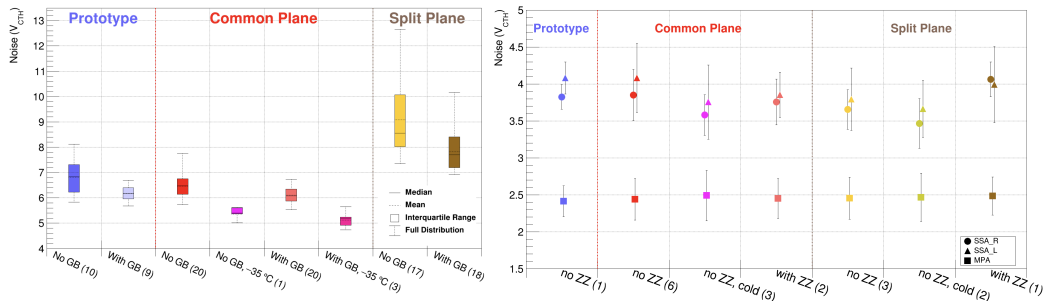

Figure 4. Noise measurements with prototype and kick-off modules. The left (right) plot features 2S (PS) modules. Left: the measurement on 2S modules were performed at -350 V bias voltage, either at room temperature or at -35°C, where indicated. Common Plane and Split Plane refers to the Service Hybrid version used in the kick-off modules. The boxes represent all individual channel noise measurements and include measurements from several modules; the numbers of modules are indicated in parentheses. Right: the measurements on PS modules were performed at varying bias voltages all above full depletion, either at room temperature or below -20°C (cold), and with or without the zigzag-cable (ZZ). The symbols represent the mean (the bars represent one standard deviation of the distribution) of all channels grouped by hybrid and sensor; the numbers of modules are indicated in the parentheses. SSA_L and SSA_R refers to measurements of the strip sensor connected to the SSA chips of the left or right hybrid, respectively. MPA refers to measurements of the pixel sensor connected to the MPA chips.

The results of the studies conducted on the kick-off modules are presented in Fig. 4. The Common Plane grounding scheme was selected as the final module design for both 2S and PS modules. This design demonstrated improved noise performance for 2S modules, while no significant performance differences were observed for PS modules. The production 2S modules will include a ground balancer, as illustrated in Fig. 1, whereas the production PS modules will omit the powering tail connecting the PS-POH and the PS-ROH.

5   Conclusions

The CMS Phase-2 Outer Tracker will provide excellent tracking performance at the HL-LHC thanks to an increased granularity, a reduced material budget and an increased radiation hardness. Moreover, it will be able to identify hits from high-p_T tracks on detector and provide this information

to the L1-trigger system. Several production centers in Europe, the US, and Asia will be involved in the multi-step assembly of more than 13 000 modules required for the Outer Tracker. Numerous prototypes have been built to fine-tune the assembly lines and testing procedures for the module production, which is expected to start in 2025. The studies performed on kick-off modules have allowed the validation and finalization of the module design before the start of production.

References

[1] L. Evans and P. Bryant, *LHC machine*, **JINST 3 (2008) S08001**.

[2] G. Apollinari et al., *High-Luminosity Large Hadron Collider (HL-LHC): Preliminary Design Report*, **CERN-2015-005**, (2015).

[3] CMS Collaboration, *The CMS Experiment at the CERN LHC*, **JINST 3 (2008) S08004**.

[4] CMS Collaboration, *Technical Proposal for the Phase-II Upgrade of the CMS Detector*, **CERN-LHCC-2015-010**, **LHCC-P-008**, **CMS-TDR-15-02**, CERN, Geneva (2015).

[5] CMS Collaboration, *The Phase-2 Upgrade of the CMS Tracker*, **CERN-LHCC-2017-009**, **CMS-TDR-014**, (2017).

[6] CMS Collaboration, *The Phase-2 Upgrade of the CMS Level-1 Trigger*, **CERN-LHCC-2020-004**, **CMS-TDR-021**, (2020).

[7] W. Adam et al., *Selection of the silicon sensor thickness for the Phase-2 upgrade of the CMS Outer Tracker*, **JINST 16 (2021) P11028**.

[8] CMS Collaboration, *CMS Technical Design Report for the Pixel Detector Upgrade*, **CERN-LHCC-2012-016**, **CMS-TDR-11**, (2012).

[9] M. L. Prydderch et al., *CBC3: a CMS microstrip readout ASIC with logic for track-trigger modules at HL-LHC*, **PoS (TWEPP2017) 001**, (2018).

[10] B. Nodari et al., *A 65 nm Data Concentration ASIC for the CMS Outer Tracker Detector Upgrade at HL-LHC*, **PoS (TWEPP2018) 099**, (2019).

[11] P. Moreira, S. Baron, S. Biereigel, J. Carvalho, B. Faes, M. Firlej et al., *lpGBT documentation: release*, Tech. Rep. http://cds.cern.ch/record/2809058, lpGBT Design Team, Geneva (2022).

[12] J. Troska et al., *The VTRx+, an optical link module for data transmission at HL-LHC*, **PoS (TWEPP2017) 048**, (2017).

[13] F. Ravera, *The CMS Outer Tracker for the High Luminosity LHC*, **JPS Conf. Proc. 42, 011010 (2024)**.

[14] D. Ceresa et al., *The Design and simulation of a 65 nm Macro-Pixel Readout ASIC (MPA) for the Pixel-Strip (PS) module of the CMS Outer Tracker detector at the HL-LHC*, **PoS (TWEPP2017) 032**, (2017).

[15] A. Caratelli et al., *Short-Strip ASIC (SSA): A 65 nm silicon-strip readout ASIC for the Pixel-Strip (PS) module of the CMS Outer Tracker detector upgrade at HL-LHC*, **PoS (TWEPP2017) 031**, (2018).

[16] K. Damanakis, *Silicon sensors for the Phase-2 upgrade of the CMS Outer Tracker; status and early results from the production phase*, **NIM A 1040 (2022) 167034**.

[17] G. Blanchot et al., *Hybrids acceptance tools for the CMS Phase-2 tracker upgrade*, **JINST 17 (2022) C06008**.

[18] G. Blanchot, *Hybrids pre-production results for the CMS Outer Tracker Phase-2 Upgrade*, [CMS-CR-2024-281](#).