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The services chain for the upgrade of the Inner Tracker Pixel detector of the ATLAS experiment. Full services from pixel modules to optical readout for the Outer Barrel sub-system

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Abstract: For the high-luminosity upgrade of the ATLAS Inner Tracking detector, a new pixel detector will be installed to increase bandwidth and to cope with higher radiation, among other challenges. In this contribution, the design aspects and qualification of the data transmission from pixel modules to optical readout are presented. A focus is put on the data cable bundles and their performance for one of the Pixel sub-systems, the Outer Barrel. The development of a custom system for production testing of the bundles is discussed. Finally, in preparation of the detector integration, developments regarding functionality and connectivity testing are analyzed.

Keywords: Detection of defects; Particle tracking detectors; Special cables

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1 Introduction

A major upgrade of the ATLAS experiment [1] is required to cope with the conditions expected at the High Luminosity Large Hadron Collider [2] at CERN. The new Inner Tracker (ITk) Pixel detector of the upgrade, will be composed of an Inner System, two Endcaps, and an Outer Barrel (OB). The OB will include 4,472 pixel modules, arranged on two main types of modular local support (LLS) structures (figure 1), the longerons and the inclined half rings. In total, 158 LLSs will form the OB.

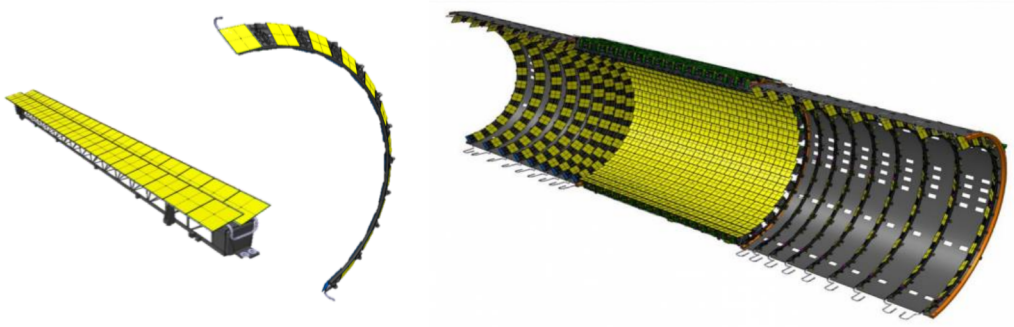

Figure 1. From left to right, a longeron, an inclined half ring and half layer of the OB featuring longerons at the middle part and two inclined units, one at each end, fitted with inclined half rings.

As the design of the different detector components has been completed, focus is shifting to activities such as production quality control (QC) and detector integration.

2 The ITk OB services

Depending on the specific location within the OB, the infrastructure required to support monitoring, powering and communication with the detector electronics (referred to as services) varies due to electrical and mechanical constraints of the different regions. There are 14 different flavours of pigtails

that are connecting the modules via a single Flexible Printed Circuit (FPC) connector and a surface mount technology (SMT) terminal on the module side. On the other end, each pigtail connects to one of 8 types of the Patch Panel Zero (PP0) printed circuit boards (PCB) using a custom Z-ray interposer on the PP0 side (figure 2). The PP0 is responsible for the local distribution of power and data signals for up to 14 modules as well as hosting the MOPS [3] chip which is the main tool of the detector control system (DCS). Power, DCS and data signals come to the PP0s through the type-1 power and type-1 data bundles. The type-1 power bundles bring the Power and DCS signals from the PP1 connector at the edges of the ITk. The type-1 data bundles bring the data signals from and to the optosystem [4] where the electro-optical translation takes place and from where optical fibers link the detector system to the back-end.

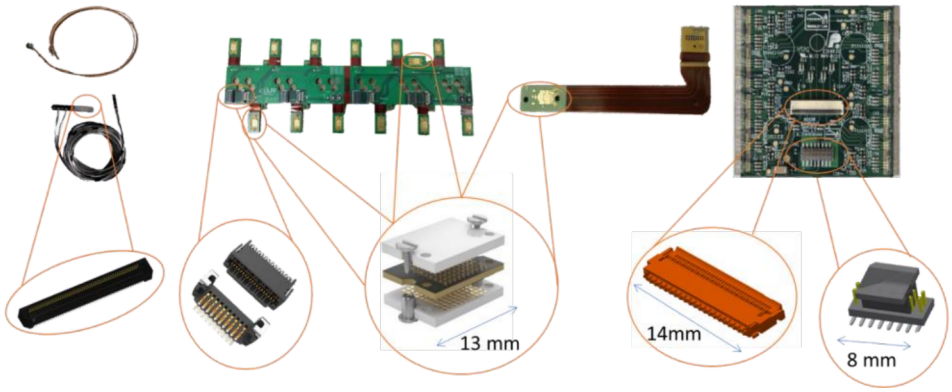

Figure 2. From left to right, type-1 power and type-1 data bundles, a PP0, a pigtail and the pixel module. The connectors indicated from left to right are the SAMTEC ERF8-050, SAMTEC UEC5 UCC8, SAMTEC Z-RAY custom interposer, MOLEX 502598-3993, SAMTEC FTM-108-02.

3 ITk OB command and data transmission

The high-speed data links between the optosystem and the front-end (FE) Application Specific Integrated Circuits (ASICs) on the pixel modules is one of the most critical components of the OB. These links are of two types: the downlink or command (CMD) signals which are used to configure and control the FE ASICs and the uplinks or Data signals which are the outputs of the FE ASICs with all the particle hit information. The reason why these links are critical is their length which reaches beyond 6 m from ASIC to ASIC for certain areas of the detector and the speed of the communication which is 1.28 Gb/s for the Data.

The CMD and Data are treated in an identical way through the services. Both types of links are served by differential pairs for the full length. The requirement is to have a uniform impedance of 100 Ohms ±10% and a maximum of 20 dB of insertion loss for the full chain at 640 MHz. The insertion loss requirement comes mainly from the pre-emphasis and equalization capabilities of the ASICs at the two ends of the Data path.

The CMD signals begin at the optosystem and specifically the lpGBT [5]. The signalling adopted by the lpGBT transmitters is the CERN low Power signalling (CLPS) which is operating at 600 mV of nominal common mode voltage and a configurable 200–800 mV of differential amplitude. The lpGBT transmitters also feature several modes and levels of pre-emphasis. The CMD signals

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travel along the services before they reach the modules. At the module level, there is an SMT termination resistor of 100 Ohms and 4 FE ASICs listening to the same CMD signal through 100 nF AC-coupling capacitors.

The Data signals begin at the FE ASIC on the module, the ITkPix, developed by the RD53 Collaboration [6]. The ITkPix ASICs contain current mode logic differential output drivers with programmable pre-emphasis. The Data signals go through 8.2 nF AC-coupling capacitors (1 nF in the prototype and pre-production version of the modules) travel through the services and finally reach the optosystem. At the optosystem, the GBCR [7] ASIC is the receiver, provides configurable equalization and re-timing facilities and transmits the processed signals to the lpGBT inputs. The number of Data links per module differs between one and two depending on the bandwidth required to serve the data generated which in turn depends on the location in the detector.

4 Type-1 data bundle QC

The ITk OB type-1 data bundles consist of three main parts. The termination board(s) towards the PP0 side, up to 24 individual shielded twinax cables and the termination board towards the optosystem side. In order to guarantee that all of the bundles reserved to be used for detector integration can perform their expected function with zero lost channels, a chain of QC and quality assurance steps were planned and developed.

The most important QC step, arguably, is the electrical test of the assembled type-1 data bundles after they have been received from the supplier. The electrical test system was developed with a conflicting set of requirements in mind: it is easy to use and with a throughput of 1 bundle tested per few minutes. It does not need specialized equipment beyond what is found in a standard electronics lab. It is able to detect defects of the termination board to cable soldering joints but also of the cables themselves. It was inexpensive and fast to develop and finally it is capable of testing all different flavours of type-1 data bundles with no need for any operator input.

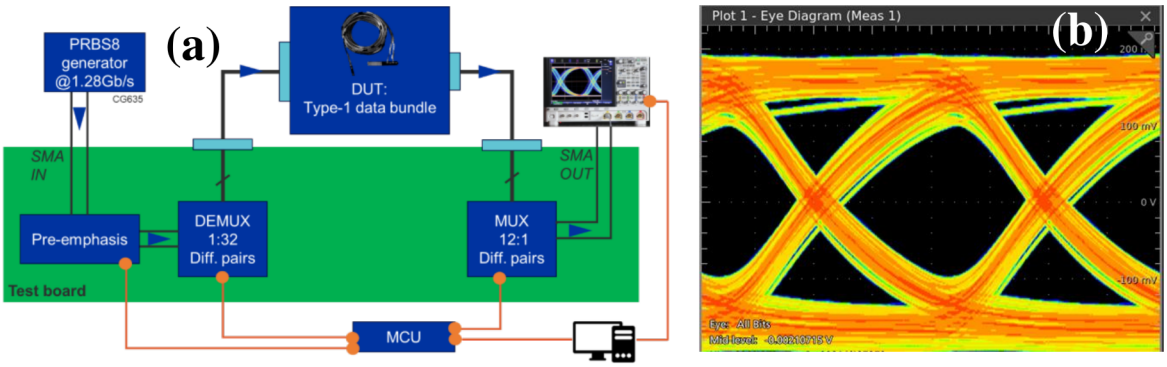

Figure 3. (a) Block diagram of the electrical QC test system of the type-1 data bundles. (b) eye diagram captured with the test system, using as the device under test (DUT) a cable with 14 dB insertion loss at 640 MHz.

The system that was developed can be seen in figure 3a. It is based on multiple levels of the HD3SS3415R differential switch for the MUX and DEMUX blocks as well as the DS25BR120 LVDS buffer with pre-emphasis for the required signal boosting. The system can be agnostic with respect to the flavor of bundle that has been connected to it. The test signal is set to be PRBS8 1.28 GB/s to match the maximum speed required to pass through these bundles. The test software

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running on a computer connected to a microcontroller (MCU) board controls the pre-emphasis, mux and demux blocks and switches through all the possible configurations in order to register the eye width and eye height for each of them. If eye width and height are above a set threshold for all the pin configurations that correspond to a known bundle flavor then the bundle passes the test. The criteria for the minimum eye width and height are set by using a number of worst-case bundles (6 m long) extracting the average and standard deviation of the width and height and using the 3σ rule to detect outliers which would indicate a bad line.

5 Connectivity tester of the Data and CMD paths

During System Testing activities, as well as when planning the QC of the LLSs and detector integration testing and QC, it became evident that efforts would be significantly reduced and time could be saved by having the capability to verify the connectivity of the full chain of services without powering and communicating with the modules. The operating procedure for detector components asks for a dew point of $-60\,^{\circ}\mathrm{C}$ before powering which, starting from room conditions, takes about 5 h to reach in the related QC setups. This means that any issue along the services e.g. insufficient insertion of pigtail at FPC connector of the module, contamination or misplacement of the z-ray connectors at the PP0 etc. would result in >5 h of time loss since it would call for opening the environmental enclosure, finding and fixing the issue and then drying the volume inside the enclosure again.

To achieve this, a custom device, called type-1 data connectivity tester (T1DCT) was developed with the capability to connect to the type-1 data bundle in place of the optosystem and inform the operator of the health of all the DATA and CMD paths from the type-1 data bundle end all the way to the module. The T1DCT is a handheld, battery-powered device, with a teensy 4.1 board at its heart. This board is based on an Arm® Cortex®-M7 MCU by NXP. The necessary multiplexing in order to test the different lines is made possible with the ADG706 16-channel multiplexers by Texas Instruments.

The type-1 data connector towards the optosystem has a fixed mapping. There can be up to 8 CMD and up to 24 Data lines routed from each Optoboard in the optosystem to the modules through the services depending on the different system flavours. These appear at fixed pins of the type-1 data connector and are not interchangeable. The T1DCT was designed with the idea of it being agnostic with respect to the flavours of hardware connected to it (requiring no input) and simply searches for healthy, meaning without shorts or opens, routed lines at the level of the type-1 data connector and informs its operator of the number and identification of the ones it found.

5.1 Connectivity testing of CMD path

Any healthy, routed CMD line from type-1 data connector to the module can be represented by the equivalent circuit in figure 4. In DC, all CMD lines appear as a resistor $R = R_\pi + R_t$ where R_π the parasitic resistance along the services on the forward and return path and R_t the termination resistor on the module. The T1DCT measures the resistance of all the different possible CMD lines and healthy lines are readily identifiable in the range of 100 to 130 Ω.

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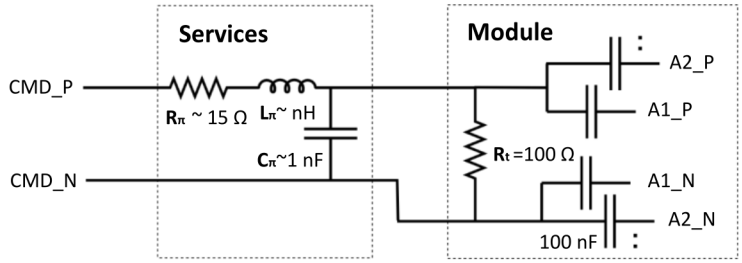

Figure 4. Equivalent circuit of the CMD path from the type-1 data connector to the module. ITkPix receivers (after A1_P, A1_N etc.) do not affect the circuit behavior in DC and are not included.

5.2 Connectivity testing of Data path

Any healthy, routed Data line from type-1 data connector to the module can be represented by the equivalent circuit in figure 5. Unlike the CMD path, the Data path in DC appears as an open circuit because of the on-module AC-coupling capacitors C before the termination resistors in the FE ASIC drivers. In the drivers, there are also the ESD protection diodes and the MOSFETs that normally drive the outputs of the ASIC. When $V_A - V_B$ is small and the ASIC is not powered, diodes and MOSFETs are off and the circuit can be simplified by excluding them.

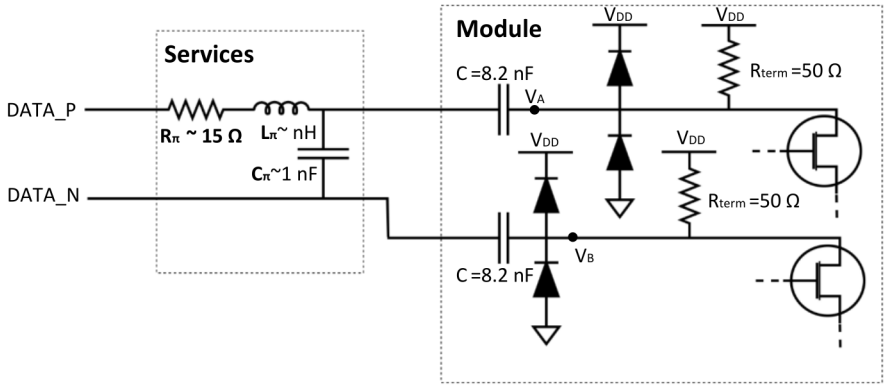

Figure 5. Equivalent circuit of the Data path from the type-1 data connector to the module. Circuit elements at MOSFET Gate and Source are not relevant for the analysis here and are not included.

Assuming a tester circuit with a voltage source V_o, a switch and a series resistor R_{test} that induces a step response of the circuit with the above condition, the system can be represented as in figure 6a. Its step response can then be analytically calculated as follows:

$$I(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t}, \quad s_{1,2} = -\frac{R}{2L_\pi} \pm \sqrt{\left(\frac{R}{2L_\pi}\right)^2 - \frac{1}{LC_t}} \tag{5.1}$$

$$\text{for} \quad R > \frac{2L}{\sqrt{L_\pi (C_t)}}, \quad R \gg R_{\text{term}}, \quad R = R_{\text{test}} + R_\pi, \quad C_t \approx C_\pi + \frac{C}{2}$$

Equation (5.1) can be further simplified to $I(t) \approx A_1 e^{s_1 t}$, since the s_1 exponent will dominate the response. Finally, for $R \gg \frac{2L}{\sqrt{L_\pi (C_t)}}$, $s_1 \to -\frac{1}{RC_t}$. This means that by choosing an appropriately large resistor R_{test}, in our case 10 kΩ, the dynamics of the whole circuit are like a simple RC filter,

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with the effects of L_π, R_{term} being negligible (figure 6b). The T1DCT was then designed to employ a 555 timer integrated circuit in order to charge and discharge (sequence of step responses) for some cycles the detector circuit with the aforementioned R_{test}, and the frequency of the resulting waveform is proportional to $\frac{1}{C_t}$. This way, we have effectively converted C_t to frequency which is then measured by the tester's MCU. As an example, a Data path not routed at all in the type-1 data bundle, disconnected at the level of the PP0 or properly connected down to the module can be distinguished as "zero", C_π or $C_\pi + \frac{C}{2}$ capacitance respectively.

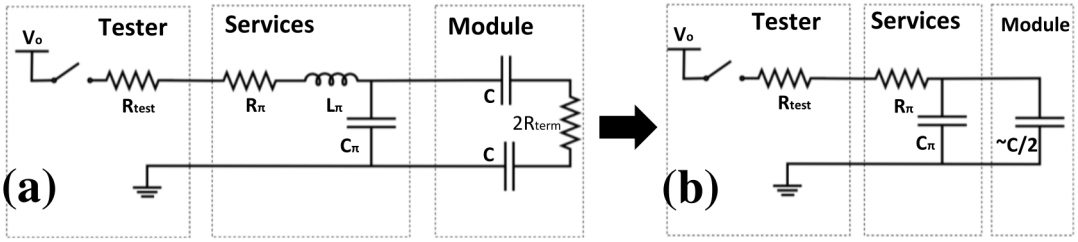

Figure 6. (a)Simplified equivalent circuit for the Data path, with a tester circuit connected to it for inducing a step response. (b) Further simplified equivalent circuit for the Data path, when $R \gg \frac{2L}{\sqrt{L_\pi(C_t)}}$.

6 Conclusion

The ATLAS ITk OB will soon start to come together. It is a complex system comprising of dozens of different parts, with a long and convoluted services chain. A simple, yet effective electrical QC system for production was developed and presented here for a critical component of the services, the type-1 data bundles. Finally, a unique need of being able to test electrical connectivity of the full services chain without performing functionality testing gave rise to the development of a tool, the T1DCT, which is based on resistance and capacitance measurements.

References

[1] ATLAS collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, 2008 *JINST* **3** S08003.

[2] G. Arduini et al., *High Luminosity LHC: challenges and plans*, 2016 *JINST* **11** C12081.

[3] R. Ahmad, *The Monitoring of Pixel System (MOPS) chip for the Detector Control System of the ATLAS ITk Pixel Detector*, *J. Phys. Conf. Ser.* **2374** (2022) 012094.

[4] L. Franconi, *The Opto-electrical conversion system for the data transmission chain of the ATLAS ITk Pixel detector upgrade for the HL-LHC*, *J. Phys. Conf. Ser.* **2374** (2022) 012105.

[5] lpGBT Team, *lpGBT Manual*, CERN (2024) [https://lpgbt.web.cern.ch/lpgbt/v1/].

[6] F. Loddo et al., *RD53 pixel chips for the ATLAS and CMS Phase-2 upgrades at HL-LHC*, *Nucl. Instrum. Meth. A* **1067** (2024) 169682.

[7] L. Zhang et al., *The design and test results of A Giga-Bit Cable Receiver (GBCR) for the ATLAS Inner Tracker Pixel Detector*, 2023 *JINST* **18** C03005 [arXiv:2301.13399].

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