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Improvement in the Design and Performance of the Monopix2 Reticle-Scale DMAPS

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"LF-Monopix2" and "TJ-Monopix2" are the second generation of "Monopix" Depleted Monolithic Active Pixel Sensor prototypes fabricated in 150 nm and 180 nm CMOS processes, respectively. Both devices implement a fully functional column-drain read-out architecture at a reticle-size scale, but differ on the concept used for pixel design. LF-Monopix2 has each pixel's full front-end and read-out circuitry placed and isolated inside a charge collection node of a size comparable to the pixel area. TJ-Monopix2 separates all electronics from its small collection electrode within the pixel and uses process modifications to enhance its charge collection capabilities. The chips inherited and improved radiation-hard designs tested in their direct predecessors, while also reducing their pixel sizes and increasing their active column lengths to 1.7 centimeters.
An overview of the design and latest test results of unirradiated Monopix2 chips are presented. Their front-end performance was quantified according to their response to injected test pulses or radioactive sources. Moreover, a successfully thinned-down and fully depleted LF-Monopix2 showed a high and uniform in-time detection efficiency on a test beam campaign.

KEYWORDS: Semiconductor Detectors, Radiation-Hard CMOS Sensors, Depleted Monolithic Active Pixel Sensors, Radiation Damage.

1. Introduction

Multiple particle collider experiments intend to use large areas of semiconductor tracker systems based on radiation-hard pixel detectors with high-rate capability. By integrating sensor and readout electronics in one silicon piece, a monolithic active pixel sensor designed in a commercial CMOS process could reduce the material budget and production complexity of the devices used for that purpose [1]. With an increasing accessibility to CMOS imaging technology, multiple research efforts have been dedicated in the last decade to the development of radiation-hard versions of this concept as an alternative to the standard hybrid pixel approach. These novel detectors, known as "Depleted Monolithic Active Pixel Sensors" (DMAPS), have their radiation tolerance enhanced through technology add-ons and careful design allowing them to be biased with high voltages [2–4] and/or collect charge through drift in a highly resistive silicon substrate [5–7].

The goal of the "Monopix" DMAPS line [8, 9] is the development of radiation-hard monolithic CMOS sensors that (1) integrate all signal processing and digital read-out electronics within each pixel cell and (2) are read-out with a fast synchronous "column-drain" architecture [10, 11]. Two different technologies and pixel layout concepts were chosen to implement these features: "LF-Monopix" uses a 150 nm CMOS process and locates all pixel circuitry within a large charge collection electrode, while "TJ-Monopix" was designed in a 180 nm CMOS process and it has all pixel electronics separated from its small electrode. In these devices, electronics and sensor have been designed to meet the requirements of the outer layers of the ATLAS Inner Tracker (ITk) at the HL-LHC [12]. Hence, the chips are expected to handle an event readout rate of $\sim 1\,\mathrm{MHz/mm^2}$ within a time window of 25 ns, be radiation tolerant up to a Total Ionising Dose (TID) of 80 Mrad and have a detection efficiency $> 98.5\%$ after a Non-Ionizing Energy Loss (NIEL) fluence of $10^{15}\,\mathrm{n_{eq}/cm^2}$. The first Monopix chips ("LF-Monopix1" and "TJ-Monopix1") were fully functional and intensively measured in order to characterize their performance, identify and fix possible design drawbacks and prove their radiation hardness [13–19].

The second and latest Monopix prototypes ("LF-Monopix2" and "TJ-Monopix2") implement optimized versions of the best performing features tested in their predecessors. The dimensions of both chips are at reticle size scale ($\geq 2\,\mathrm{cm^2}$) and they have a synchronous read-out operating in a 1.7 cm-long pixel column. Specific details for each design will be given throughout the text, but other features common to both (LF-/TJ-)Monopix2 chips are:

- An injection circuit for characterization, where a negative digital pulse is sent into each pixel to toggle two reference voltages connected to a capacitor (C_{inj}), hence injecting a charge proportional to the voltage difference into the amplifier.
- A local (4-/3-)bit current tuning DAC (TDAC) that can be used to adjust the threshold of the discriminator of each pixel in order to reduce the global threshold dispersion of the front-end.
- Time stamping of every leading (LE) and trailing edge (TE) of the discriminated signal of a pixel with a (6-/7-)bit counter running at a frequency of 40 MHz. The difference between these values is known as Time-Over-Threshold (ToT) and it has a non-linear proportionality with the input charge.

This article presents design features and improvements of the Monopix2 chips, as well as a partial characterization of their performance before irradiation.

2. LF-Monopix2

2.1 Description of the chip

LF-Monopix2 is a DMAPS designed in a 150 nm CMOS process from LFoundry [20]. The device (as depicted in Fig. 1) has a total area of $1.8\,\mathrm{cm^2}$, out of which 82% corresponds to an active matrix of 56×340 pixels. The remaining space is occupied by decoupling capacitors, pads, guard rings, end-of-column and periphery logic. It uses a Czochralski-grown p-type silicon substrate with a resisitivity $> 2\,\mathrm{k\Omega \cdot cm}$ as support and sensitive material. After wafer processing (TAIKO backgrinding, plasma etching, accceptor ion implantantion and metallization), it was possible to thin LF-Monopix2 chips down to 100 µm. These samples could also be depleted through a negative bias voltage applied to their outermost guard ring, while showing a leakage current $< 1\,\mathrm{\mu A/cm^2}$ during operation.

The pixels have a size of $150 \times 50\,\mathrm{\mu m^2}$, a value 40% smaller than in the first prototype. Their layout follows the "large collection electrode" approach shown in Fig. 2, where full CMOS-capable electronics are placed and isolated within a high-voltage compatible n-type implant used as charge collection node. This design provides a strong and uniform electric field across the pixel, which results in short drift paths and a high collection efficiency that minimize the probability of charge trapping after irradiation. On the other hand, the junction between the collection node and p-type well isolating in-pixel electronics contributes significantly to the overall detector capacitance (C_{det})

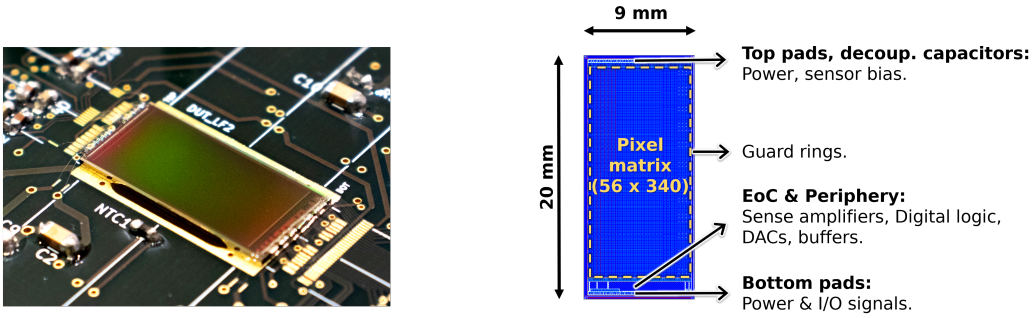

Fig. 1. The LF-Monopix2 DMAPS and its chip layout.

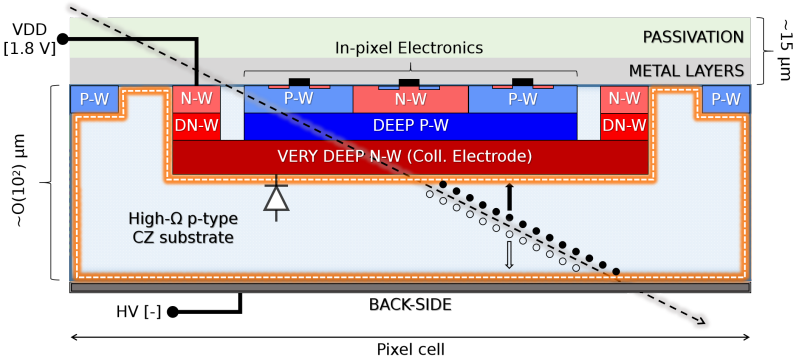

Fig. 2. Schematic cross-section of the "large collection electrode" pixel design implemented in LF-Monopix. The depletable volume is delimited by white dashed lines.

of ~ 250 fF. A value of this magnitude requires special design efforts to deal with effects like a large equivalent noise charge (ENC), the possibility of switching digital signals coupling to the collection electrode, or a slow rise time during amplification.

The core front-end design of LF-Monopix2 (present in ~ 57% of the matrix) uses a combination of charge sensitive amplifier (CSA) and discriminator that was available in its predecessor [21] and proved to be fast (threshold overdrive ~ 400 e^- [15]) and radiation-hard (up to a TID of 100 Mrad and NIEL fluence of 1×10^{15} n_{eq}/cm^2 [13, 19]). The amplifier, labeled "CSA 1", uses an NMOS transistor as input of a single-staged folded cascode structure. Moreover, the discriminator consists of a self-biased amplifier with a CMOS inverter at its output stage. The ENC of this front-end in LF-Monopix2 was measured to be ~ 100 e^- [17], an improvement of 30% with respect to the first prototype thanks to the reduction in C_{det} associated with the smaller pixel size. Besides, its analog power consumption (measured at default DAC settings) was 28 µW/pixel (~ 370 mW/cm^2).

Even though the main front-end was expected to benefit from the reduction of detector capacitance in LF-Monopix2, some additional variations aiming to further improve the gain and time response were also included in a fraction of the chip for testing. The first one, consists in reducing the feedback capacitance (C_f) of the front-end with CSA 1 from 5 to 1.5 fF. The second and third one, correspond to two new CSAs with a telescopic cascode structure, C_f = 1.5 fF and fixed (CSA 2) or adjustable (CSA 3) currents flowing into the input transistor.

The untuned threshold dispersion varied between 350 and 800 e^- depending on the front-end design. Nevertheless, this value could be successfully tuned down to ~ 100 e^- in all cases by using the 4-bit local TDAC [19].

2.2 *Improvement of the sensor's breakdown voltage*

LF-Monopix2 features the guard-ring layout illustrated in Fig. 3. It was inspired by the outcome from comparative measurements of different guard-ring configurations in passive sensor test structures fabricated in the same technology and resistivity as both LF-Monopix chips [22, 23]. These studies indicated that the breakdown voltage of unirradiated sensors can benefit from (1) the use of deep n-type implants in the n-ring, (2) an increase in the distance between the n-ring and the closest guard-ring to the matrix and (3) the use of combined n- and p-type implants for the guard-rings. The latter two modifications were the main changes in the guard-ring design of LF-Monopix2 with respect to that of its predecessor. Their implementation resulted in an increase of the chip's breakdown voltage of ~ 200 V, as shown in Fig. 4 through I-V curves measured in 100 µm thick samples. Measurements in multiple devices indicate that the breakdown voltage before irradiation can vary between sensors from 460 to 500 V.

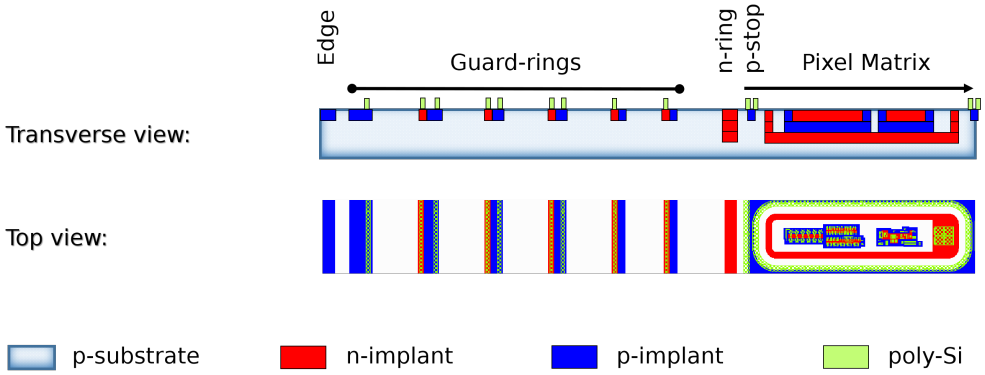

Fig. 3. Guard-ring design of LF-Monopix2.

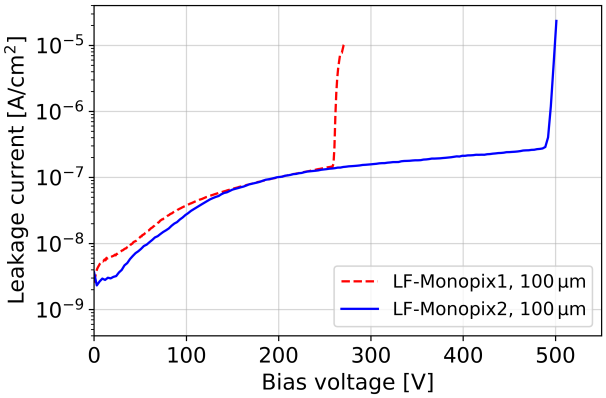

Fig. 4. I-V curves of 100 µm thick LF-Monopix1 and LF-Monopix2 devices. The leakage current was divided by the total area of every chip.

2.3 Measurement of the injection capacitance

The injection capacitance of LF-Monopix2 was measured in order to use reference pulses to calibrate the ToT response of each pixel to collected charge. In the first place, a scan across the whole range of injection voltage amplitudes was carried out in small steps and the resulting ToT distributions were recorded for each of them. In the second place, the chip was exposed to characteristic fluorescent X-rays from molybdenum and silver targets ionized by a radioactive ^{241}Am source. A significant fraction of these photons have an energy corresponding to the characteristic K_α transition of an electron to the innermost energy shell of each material: $K_\alpha \sim 17.4$ keV for Mo and $K_\alpha \sim 22.1$ keV for Ag. The most intense peak in each pixel's ToT distribution was fitted with a gaussian function, and its mean value was associated with the amount of charge created in silicon by the absorbed K_α X-rays. In the end, this mean ToT value was used to trace-back the voltage that caused the same pixel response in the first measurement, and the ratio between charge created and injected voltage resulted in the capacitance value. The distributions of C_{inj} values calculated individually for $\sim 10^4$ pixels are shown in Fig. 5 and 6 for the molybdenum and silver targets, respectively. An average of the measured capacitances results in a $C_{inj} \sim 2.73$ fF. This value is larger than the ~ 2 fF expected from post-layout simulations during design, but the same discrepancy was observed in LF-Monopix1 [24] and it could be explained by an imprecise modeling of the custom-made capacitor in software.

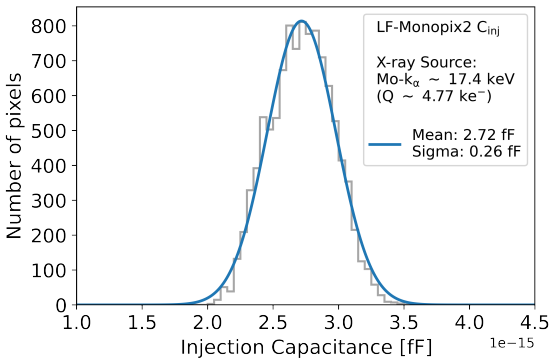

Fig. 5. Injection capacitance measured in LF-Monopix2 with molybdenum's K_α characteristic X-rays as reference.

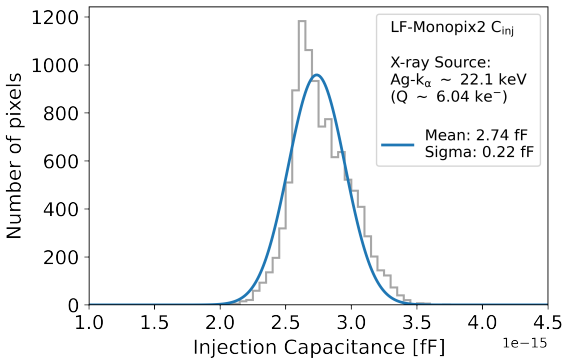

Fig. 6. Injection capacitance measured in LF-Monopix2 with silver's K_α characteristic X-rays as reference.

2.4 Measurement and improvement of the gain of the front-ends

A distribution of the gain of each front-end design was measured by calculating the slopes of linear fits to single pixel thresholds at four different global threshold voltages. In order to minimize the influence of the local tuning circuitry on the measured gains, the scans were carried out with all TDAC values set to the unbiased condition of the discriminator. The results for every front-end configuration are shown in Fig. 7. For CSA 1, the use of a feedback capacitance of 5 fF results in a gain of (13.2 ± 0.4) μV/e$^-$, while a smaller capacitance of 1.5 fF increases this value to (25.7 ± 1.5) μV/e$^-$. The front-ends with new CSA designs use only a feedback capacitance of 1.5 fF, and their measured gains were (22.6 ± 1.0) μV/e$^-$ for CSA 2 and (29.6 ± 2.1) μV/e$^-$ for CSA 3.

2.5 Test beam results for thin sensors before irradiation

LF-Monopix2 chips with a thickness of 100 μm were biased and read-out while exposed to 5 GeV and 2.5 GeV electron beams at the DESY II [25] and ELSA [26] accelerator facilities, respectively. The detection efficiency and timing performance of the devices were quantified using a EUDET-type

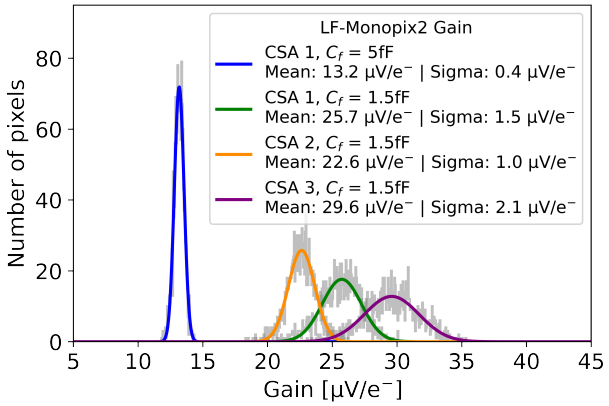

Fig. 7. Gain of the multiple front-end designs implemented in LF-Monopix2.

telescope [27] for particle tracking and a FE-I4 chip [28] as timing reference plane. Each region with a common front-end in the chip was operated at a mean threshold of 2 ke^- for a comparison of the detection time between different designs. Furthermore, multiple bias and threshold voltages were set to the largest region of the matrix with a common front-end (CSA 1, with C_f = 5 fF) to evaluate the efficiencies with respect to those parameters. For all cases, the tuned threshold distributions had a dispersion of 100 e^-.

A scan across different bias voltages was used to determine the value at which the sensor reaches full depletion. After a calibration of the individual ToT response of single pixel hits into charge, the overall charge distribution measured in the active region was fitted with a convolution of Landau and Gaussian functions. The most probable values (MPV) extracted for each voltage step were used to estimate the width of the depleted region, under the assumption of a charge per unit length of 71 $e^-/\mu m$ created by the energy loss of 5 GeV electrons traversing an 85 μm thick silicon layer. Fig. 8 shows the most probable signals observed in two different LF-Monopix2 samples with respect to the applied bias voltage. The depletion plateau started at a value between 15 and 20 V, in agreement with the manufacturer's claim of a substrate resistivity larger than 2 $k\Omega \cdot cm$. In addition to that, both chips concurred well with one another in their depletion profile before reaching the plateau, as expected from samples diced from the same silicon wafer.

Since approximately 15 μm of the chip's total thickness correspond to passivation and metal layers, the maximum depletion width expected in a 100 μm thick chip would be close to 85 μm. In reality though, the average silicon width in each sensor can be up to 10 μm smaller than the thinning target value after backside processing due to additional removal during etching and the total thickness variation (TTV) across the wafer. The full depletion widths were (83.5 ± 2.4) μm for the first sample and (76.4 ± 2.4) μm for the second one, where the uncertainty of each measurement is mainly due to the ToT resolution. These values are still within the TTV range measured in wafers of this thickness after processing (∼ 6 μm), and the MPVs recorded were more than three times larger than the chip's minimum operational threshold.

The hit detection efficiency of a fully depleted device was quantified for $\sim 10^4$ pixels at a threshold of (2040 ± 104) e^-. The data were analyzed using the python-based "BTA" software [29] and projected onto the 2 × 2 pixel array shown in Fig. 9. The resulting efficiency is uniform across the whole pixel area, and its mean value of 99.6% is in very good agreement with the one reported for an unirradiated LF-Monopix1 of similar characteristics [17].

The time-walk of a hit pixel corresponds to the time difference between the rising edge of its CSA signal above threshold and the start of charge collection. This quantity was recorded in beam for every hit using the timestamps of the leading edge of the output of the discriminator and the

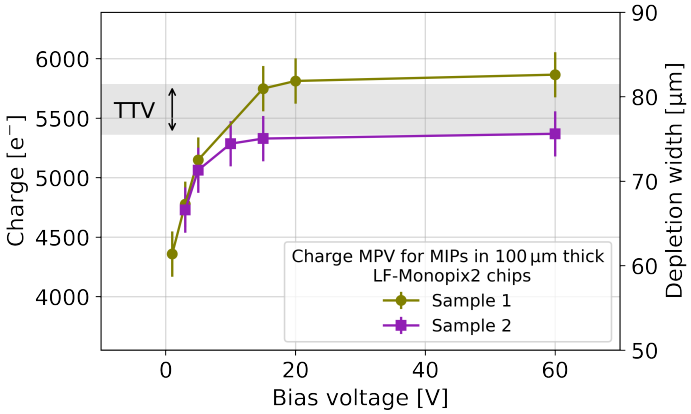

Fig. 8. Most probable charge signals created by the passage of 5 GeV e⁻ through 100 µm thick unirradiated LF-Monopix samples as a function of the applied bias voltage. The height of the shaded region in the vertical axis corresponds to the average total thickness variation in backside processed LF-Monopix2 wafers.

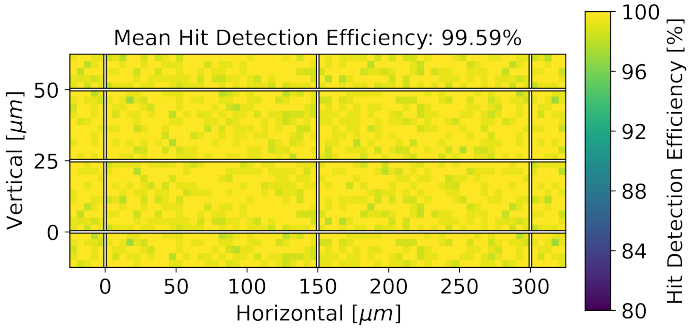

Fig. 9. Hit detection efficiency map of a 100 µm thick LF-Monopix2 (data from ~ 10^4 pixels projected onto a 2×2 pixel array). The chip was exposed to a 5 GeV e⁻ beam. Threshold: 2 ke⁻. Bias voltage: 60 *V*.

signal of a scintillator used as trigger for all devices. Though the latter was sampled with a resolution of 1.56 ns, the resolution of the measurement was limited by the 40 MHz clock used in the chip. Fig. 10 shows (for two front-ends with CSA 1, but different C_f) the dependence of the time-walk of pixels with the largest signal in every recorded event (also known as "seed pixels") with respect to the total ToT. In these distributions, an event was considered to be "in-time" if its time-walk was within the first 25 ns. 99.43% of all efficient events were in-time for the front-end with C_f = 5 fF, representing an improvement of 2% with respect to the value measured in the same front-end in LF-Monopix1. This change can be mainly attributed to the reduction in detector capacitance due to a smaller collection node. For the front-ends with C_f = 1.5 fF, their larger gain reduced the rise time of the CSA signal, and therefore a percentage of more than 99.8% of all events were recorded in-time.

Using the time-walk measurements, it was possible to apply an additional criterion to the selection of efficient events so that only those with seed pixels registered within 25 ns were considered. Hit and in-time detection efficiencies were calculated for the front-end with CSA 1 and C_f = 5 fF, with respect to the bias voltage applied to the sensor (Fig. 11) and its mean threshold (Fig. 12). As a reference for the improvement in LF-Monopix2, the dotted line in the plots corresponds to the mean in-time efficiency of 97.2% measured for the same front-end in an unirradiated LF-Monopix1 chip with similar depletion and a threshold close to 2 ke⁻.

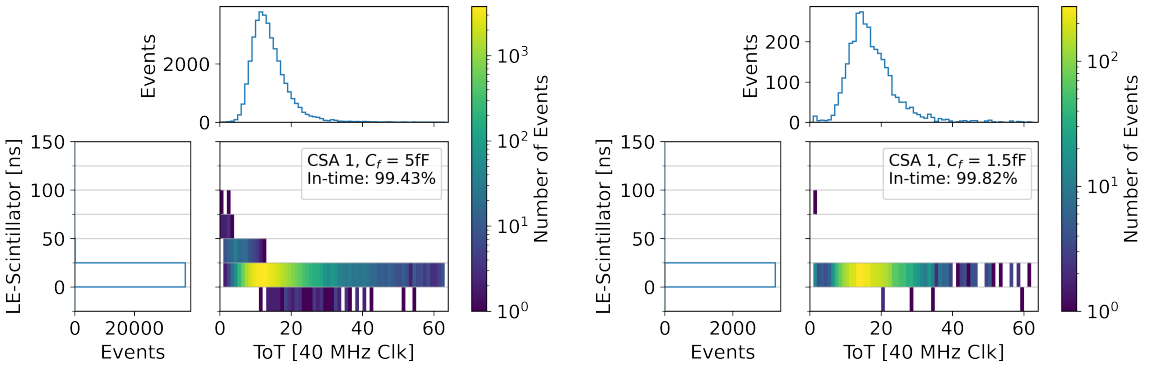

Fig. 10. Time-walk of seed pixel hits recorded in a 100 µm thick LF-Monopix2 with CSA 1 and feedback capacitance of (Left) 5 fF or (Right) 1.5 fF. The projections of both axes include all ToT or time bins. The chip was exposed to a 5 GeV e^- beam. Threshold: 2 ke^-. Bias voltage: 60 *V*.

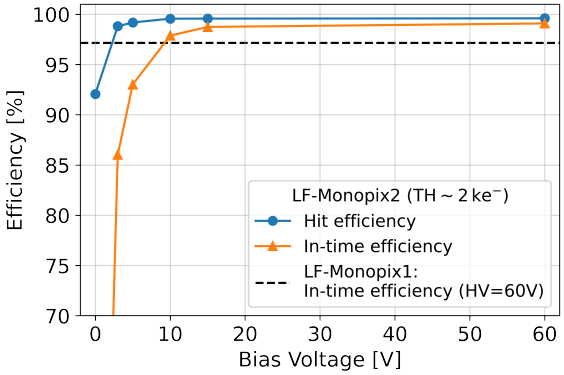

Fig. 11. Hit and in-time detection efficiencies measured with respect to the bias voltage applied to a 100 µm thick unirradiated LF-Monopix2. Front-end: CSA 1 with C_f = 5 fF. Threshold: 2 ke^-.

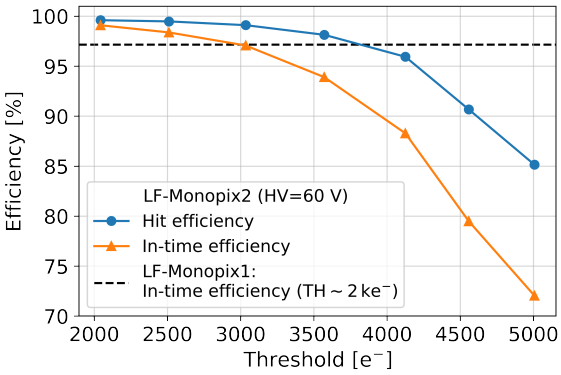

Fig. 12. Hit and in-time detection efficiencies measured with respect to the mean threshold of a 100 µm thick unirradiated LF-Monopix2. Front-end: CSA 1 with C_f = 5 fF. Bias voltage: 60 *V*.

For the overall hit detection, an efficiency larger than 98.5% could be reached at (1) a voltage above 3 *V* for a 2 ke^- threshold, or (2) a threshold below ~ 3.3 ke^- in a fully depleted sensor. Moreover, the in-time efficiency at full depletion was 99.1% for a threshold of 2 ke^-. Since almost all events were recorded within 25 ns for the front-ends with smaller C_f = 1.5 fF, their in-time efficiency would be practically the same as the hit detection one at the lowest threshold setting: 99.6%. The percentage of in-time events drops faster than the overall detected ones for lower bias voltages, since the number of hits with a smaller input charge (and a signal shaping time larger than 25 ns) increases as the lower end of the distribution gets closer to the threshold. On the other hand, the decrease of in-time efficiency for larger thresholds occurs because, for a given input charge, the time that the CSA signal takes to go above discrimination increases as the threshold voltage does. Based on these measurements and the previous characterization of changes in the front-end and sensor in LF-Monopix1 after X-ray and neutron irradiation [17, 19], LF-Monopix2 is expected to improve the already high radiation-hardness of its predecessor.

3. TJ-Monopix2

3.1 Description of the chip

TJ-Monopix2 is a DMAPS fabricated in a modified 180 nm CMOS process from Tower Semiconductor [30]. Its pixel concept and front-end were derived from the ALPIDE chip [31] and substantially optimized for improved radiation hardness. The device (as depicted in Fig. 13) has a total area of 4 cm^2, out of which 72% corresponds to an active matrix of 512×512 pixels. The remaining space is occupied by decoupling capacitors, pads, guard rings, end-of-column and periphery logic. The chip's sensitive volume can be either a high-resistivity ($\sim 1\,k\Omega \cdot cm$) p-type epitaxial layer grown on a highly doped p-substrate, or a highly resistive ($> 3\,k\Omega \cdot cm$) Czochralski-grown p-substrate.

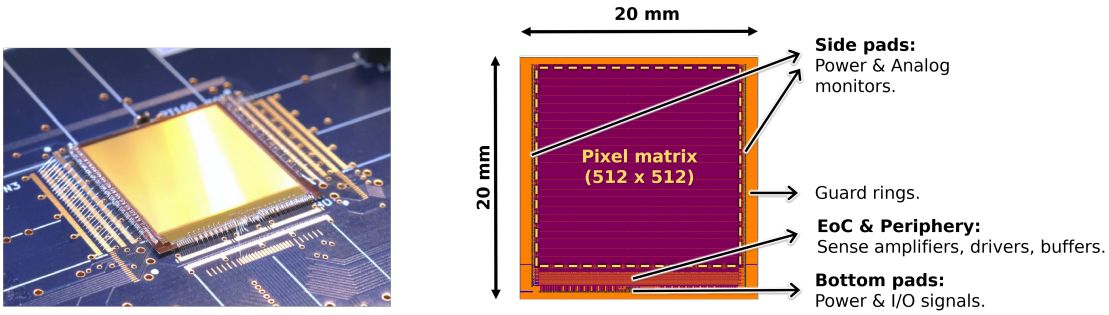

Fig. 13. The TJ-Monopix2 DMAPS and its chip layout.

The pixels have a size of $33.04 \times 33.04\ \mu m^2$. Their layout follows the "small collection electrode" approach, where a small ($\sim 2 \times 2\ \mu m^2$) n-type implant at the center of the pixel is used for charge collection while all CMOS electronics are placed at a distance from it and isolated within p-type wells. The main advantage of a small electrode design is its very small detector capacitance ($C_{det} < 5$ fF), which in turn translates into a large and fast voltage input signal. Under those conditions, an open-loop voltage amplifier is preferred to the charge sensitive amplifiers used in other particle detectors, since the original signal-to-noise ratio is large enough to require only a second stage amplification before discrimination, the circuit is very compact and it has a low power consumption of $\sim 1\ \mu W$/pixel ($\sim 90\ mW/cm^2$).

In the standard imaging process (shown in Fig. 14), a p-type epitaxial layer with a resistivity of $1\,k\Omega \cdot cm$ can be partially depleted close to the collection node by applying small voltages at both the p-well shielding the pixel electronics and the p-substrate. Charges created in the small depleted region can be collected by drift, but those in the rest of the volume would be relegated to move only by diffusion. This approach is not suitable for high radiation environments, where charges moving slowly by diffusion or those with very long drift paths have a higher probability to be trapped by bulk damage induced defects.

As a first attempt to improve the radiation-hardness of the standard process, a low-dose n-type layer between the p-well and p-type sensitive volume was added to the matrix. The purpose of this modification was to extend the depletion region across the whole pixel area and form a potential minimum towards the electrode that could enhance the collection of distant charges [7]. After a successful proof-of-concept in a small sensor [32], this modification was taken into account for the pixel designs of TJ-Monopix1 [9] and a similar chip with an asynchronous read-out architecture called MALTA [33]. Test beam campaigns in the first versions of both chips showed a significant loss of hit detection efficiency after a NIEL fluence of $10^{15}\ n_{eq}/cm^2$ [14, 16, 34]. Two main factors

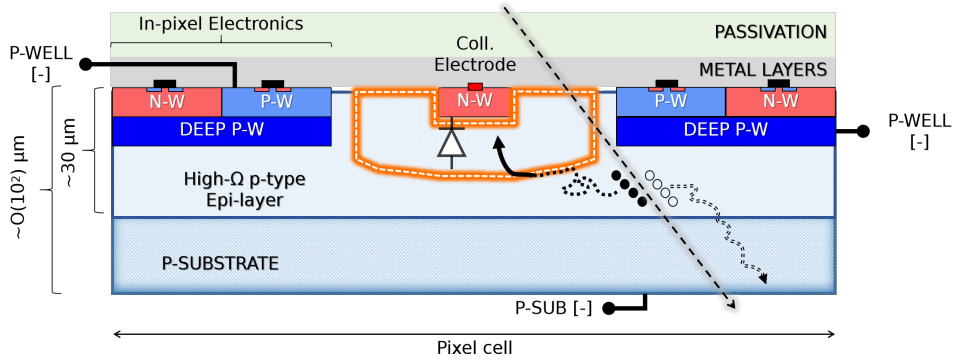

Fig. 14. Schematic cross-section of a "small collection electrode" pixel design implemented in the standard imaging process. Only a fraction of the p-type epitaxial layer close to the collection node (similar to the one delimited with white lines) can be depleted.

were identified as the causes of this performance: An inefficient charge collection at the pixel corners and a high limit to the minimum operational threshold ($> 450\,e^-$) caused by an asymmetric ENC distribution linked to random telegraph signal (RTS) noise.

The observation of detection efficiency patterns correlated to the location of the deep p-well implant in the pixel motivated a set of TCAD simulations that looked at possible improvements in charge collection through additional modifications to the implants [35]. These studies suggested two new possible process variants that would enhance the lateral field towards the collection node at the pixel edges: (1) creating a gap in the n-layer (n-gap) or (2) introducing an additional deep p-well implant below the existing one (extra deep p-well). The two features were included in a second submission of the TJ-Monopix1 chip, which was also produced in both epitaxial- and Czochralski-grown substrates (Fig.15). After neutron irradiation, samples from the new modified versions showed a significant increase in detection efficiency with respect to the original design [18]. Moreover, the improved charge collection also benefited from a larger achievable depletion volume (and hence, charge signal) in the Czochralski substrate. All of these improvements to the small electrode design are also available in the TJ-Monopix2 chips.

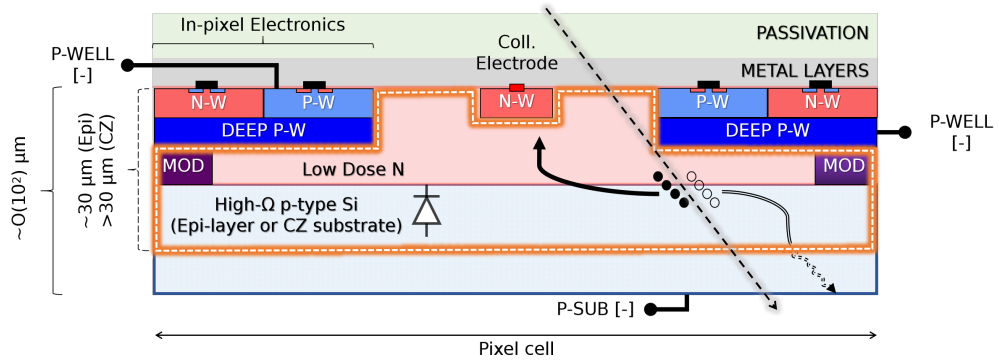

Fig. 15. Schematic cross-section of one of the "modified small collection electrode" pixel designs implemented in TJ-Monopix. The low dose n-type layer enables a uniform depletion of a p-type epitaxial layer (up to ~ 30 µm) or Czochralski substrate (larger than 30 µm). Either deep p-type implants or a gap in the n-layer at the pixel edges (MOD) enhance the lateral component of the electric field. The depletable volume is delimited by white dashed lines.

3.2 Improvement of the front-end

As mentioned earlier, the ENC distribution of TJ-Monopix1 showed a long tail towards higher charge values, which was linked to RTS noise caused by charge trapping or release at the gate interface of small transistors in the front-end. This effect limited substantially the minimum operational threshold of the chip at a reasonable noise rate. Since the magnitude of the currents associated with RTS at a gate is inversely proportional to its area, a plausible solution to minimize the sensitivity to this type of noise was to increase the size of two small transistors. This idea was successfully tested in a small test chip [36]. Hence, the dimensions of transistors responsible for the coupling capacitance and preamplifier voltage gain stage of the front-end of TJ-Monopix2 were enlarged in order to increase the signal-to-noise ratio by a factor of 3 and reduce its RTS noise component [37].

The positive effects of the changes in the TJ-Monopix2 front-end are illustrated in the ENC (Fig. 16) and threshold (Fig. 17) distributions obtained from injection scans in both versions of TJ-Monopix. In comparison to previously reported measurements [17], these scans synchronized the timestamp clock distribution across the column with the injection pulse for a more reliable sampling of the s-curves. For the ENC, its mean value was reduced by a factor of 3 in the latest prototype and the long tail due to RTS noise towards the high end of the distribution is gone. Besides, the untuned threshold dispersion in TJ-Monopix2 ($\sim 13\,e^-$) is about 60% smaller than the one in its predecessor, and thanks to the changes in ENC a minimum operational threshold of $\sim 160\,e^-$ can be reached. Moreover, the dispersion can be tuned down to $\sim 5\,e^-$ with the 3-bit local tuning DAC.

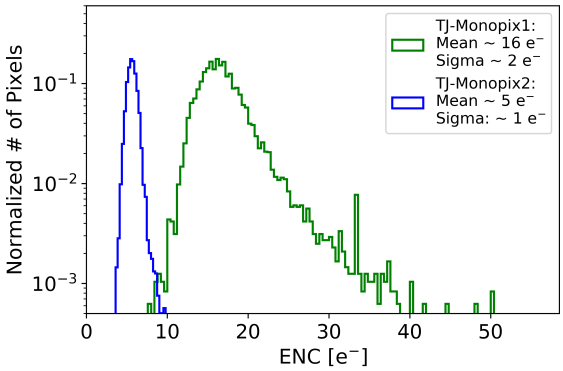

Fig. 16. ENC in TJ-Monopix1 and TJ-Monopix2. The mean and dispersion values were obtained from a gaussian fit to the data.

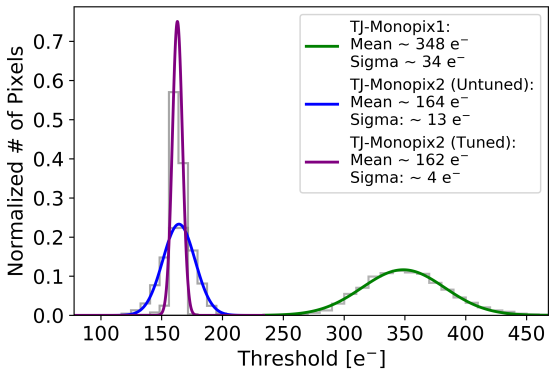

Fig. 17. Threshold distributions in TJ-Monopix1 and TJ-Monopix2. Only the TJ-Monopix2 front-end counts with local threshold tuning circuitry.

Given the significant improvement of the front-end, it is reasonable to expect that future charge collection measurements in TJ-Monopix2 devices with a Czochralski substrate and pixel edge modifications result in uniform high detection efficiencies.

4. Conclusions

The latest Monopix DMAPS prototypes, LF-Monopix2 and TJ-Monopix2, have a fully functional and fast synchronous read-out operating in a 1.7 cm-long pixel column. In addition to that, initial tests on unirradiated samples show promising improvements in their sensor and front-end performance with respect to their predecessors, as summarized in Table I.

LF-Monopix2 was successfully thinned and backside processed down to a thickness of 100 µm. Its sensor can be fully depleted before irradiation with a bias voltage > 20 V, a value reliably distant from its improved breakdown voltage of at least 460 V. Test beam measurements showed an uniform

	LF-Monopix1	**LF-Monopix2**	**TJ-Monopix1**	**TJ-Monopix2**
CMOS process	LFoundry 150 nm		Tower Semiconductor 180 nm	
DMAPS type	Large electrode design		Small electrode design	
P-type substrate (**Resistivity** [$k\Omega \cdot cm$])	Czochralski (> 2)		Epi-layer (~ 1) or Czochralski (> 3)	
Dimensions [cm^2]	0.98×0.95	0.9×2	2×1	2×2
Matrix size [Pixels]	36×129	56×340	448×224	512×512
Pixel size [μm^2]	250×50	150×50	40×36	33.04×33.04
Active col. length [cm]	0.65	1.7	0.8	1.7
Analog power [μW/Pix] ([mW/cm^2])	~ 45 (360)	~ 28 (370)	~ 1 (70)	~ 1 (90)
Gain [$\mu V/e^-$]	~ 12 ($C_f = 5$ fF)	~ 13 ($C_f = 5$ fF) ~ 26 ($C_f = 1.5$ fF)	~ 400	~ 1200
ENC [e^-]	$\sim 150 \pm 25$	$\sim 100 \pm 15$	$\sim 16 \pm 2$ (+RTS)	$\sim 5 \pm 1$
Threshold Disp. [e^-]	~ 100	~ 100	~ 35	~ 5
Max. bias voltage [V]	260 - 300	460 - 500	50	50

Table I. Design and characteristic performance values of the Monopix DMAPS designs before irradiation.

hit detection efficiency of 99.6% and an in-time efficiency of at least 99.1% for a fully depleted chip with a tuned threshold of $\sim (2 \pm 0.1)\,ke^-$.

TJ-Monopix2 has implemented in its small electrode design well-tested process modifications that are known to increase its depletion region (Czochralski-grown substrate) and the collection efficiency of charges created at the pixel edges (n-layer gap or extra p-implant). Moreover, key transistors in its front-end were enlarged to increase its gain and avoid RTS noise, resulting in a mean ENC and untuned threshold dispersion three times smaller than the ones of its predecessor. A new 3-bit TDAC circuit can tune the threshold dispersion between pixels down to $\sim 5e^-$, allowing for a mean threshold as low as $160\,e^-$ in the chip.

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