Production of flex circuits for the ATLAS ITk Pixel Outer Barrel

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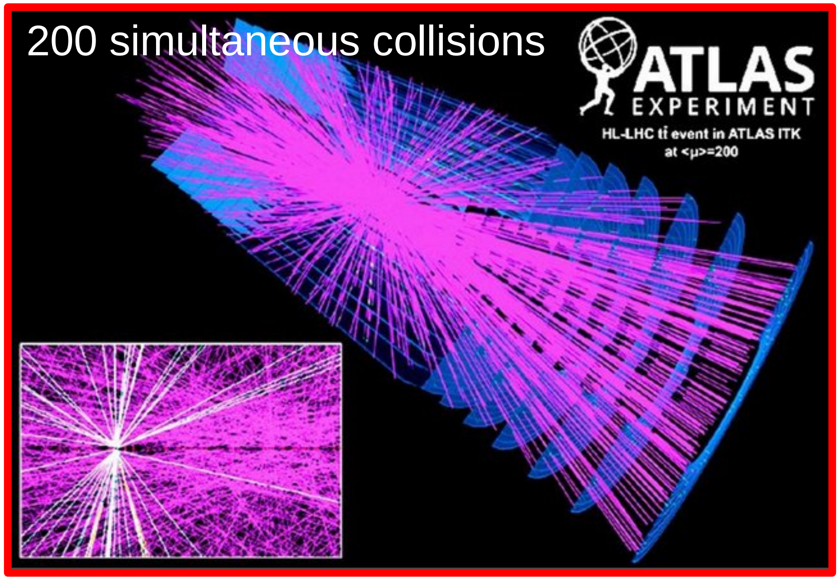
The ATLAS Inner Tracker upgrade

- The Inner Tracker (ITk) @HL-LHC:
  - Increased radiation hardness. TID=1MGy, fluence= $2x10^{16}$ n_{eq} cm^{-2}
  - Higher granularity (smaller pixels).
  - Faster readout.
  - Reduction of material.
  - Extended coverage up to |η| < 4.0.



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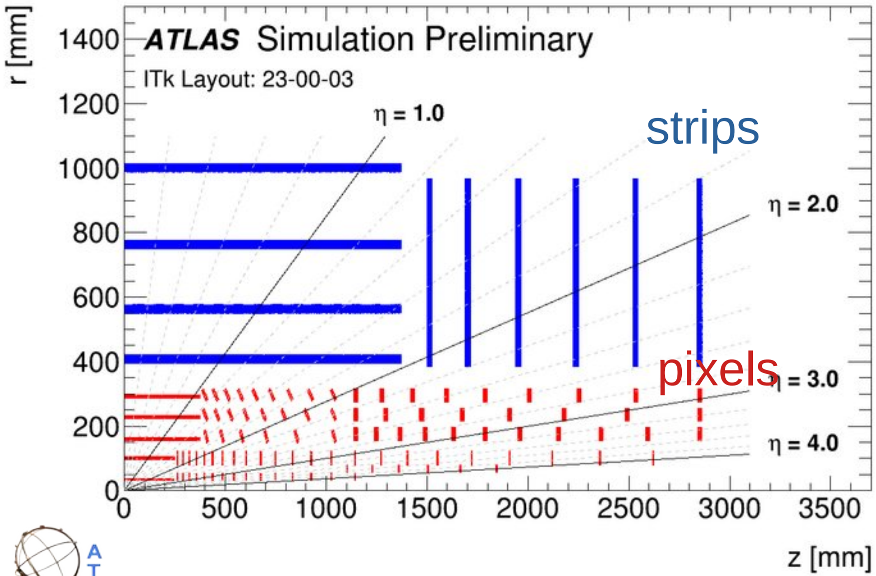

ITk-Pixel

- Reduced pixel pitch: *50x50 μm²*
- Five barrel layers with inclined sensors at |η| > 1.4 to reduce the material budget.
- Endcap rings to improve coverage.

ITk-Strip

- Four barrel layers and six endcap disks.

The ATLAS Inner Tracker upgrade

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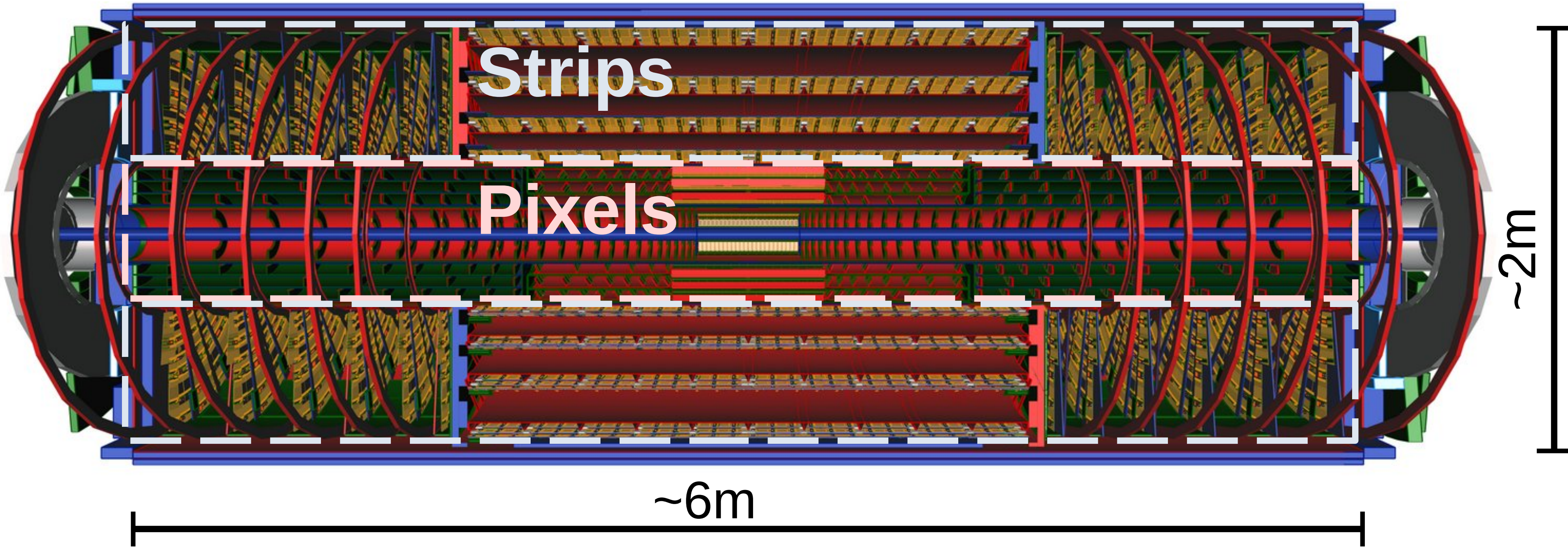
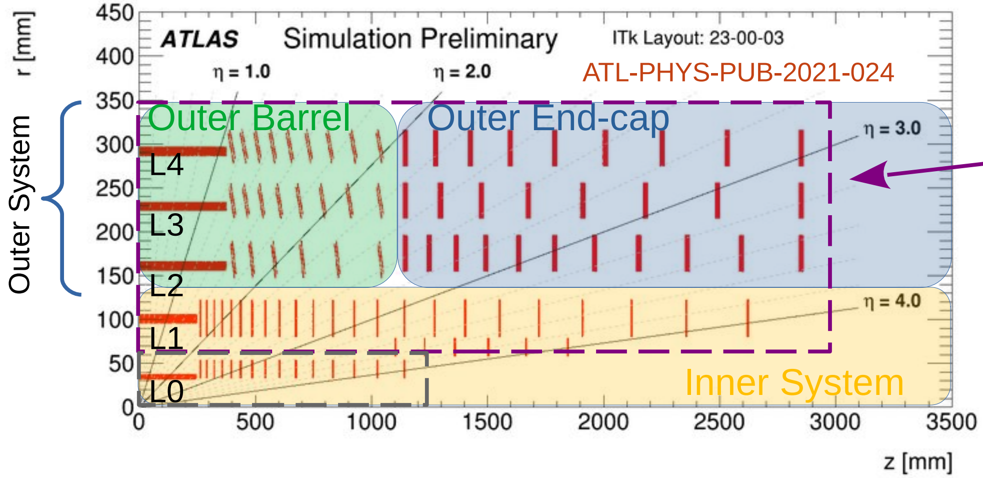
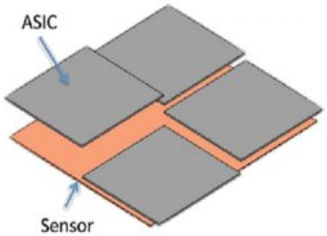
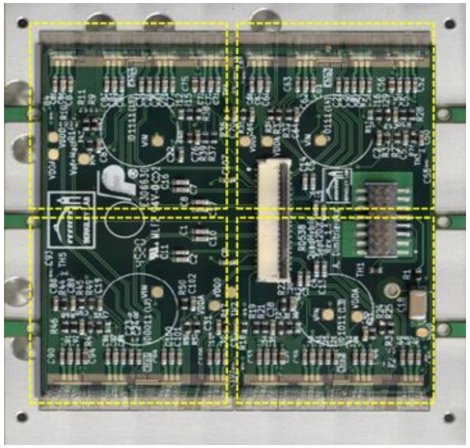


ITk (ID)	Area (m^2)	# Modules	# Channels (M)
Pixels	13 (1.6)	9164 (2000)	5100 (92)
Strips	165 (61)	17888 (4088)	60 (6.3)

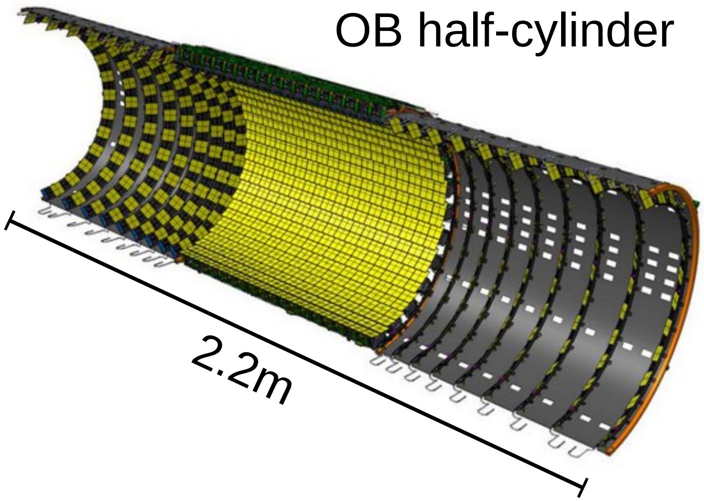


L1-4 planar quad module
(single sensor)





- **Pixel outer barrel (OB), 3 co-axial cylinders** :
  - ~50% of ITk Pixel modules, ~5k modules.



ITk-OB on-detector services design

Physics constraints

- Low material budget → thin copper.

Electrical constraints

- High speed data → controlled impedance traces, matched lengths.
- High current (6A) → thick copper.
- Resistive budget fixed → thick copper.
- 3D folding → flex-rigid PCB.
- Imposed connectors at both ends → imposed footprints.
- High voltage → clearance to deal with breakdown requirement.

Mechanical constraints

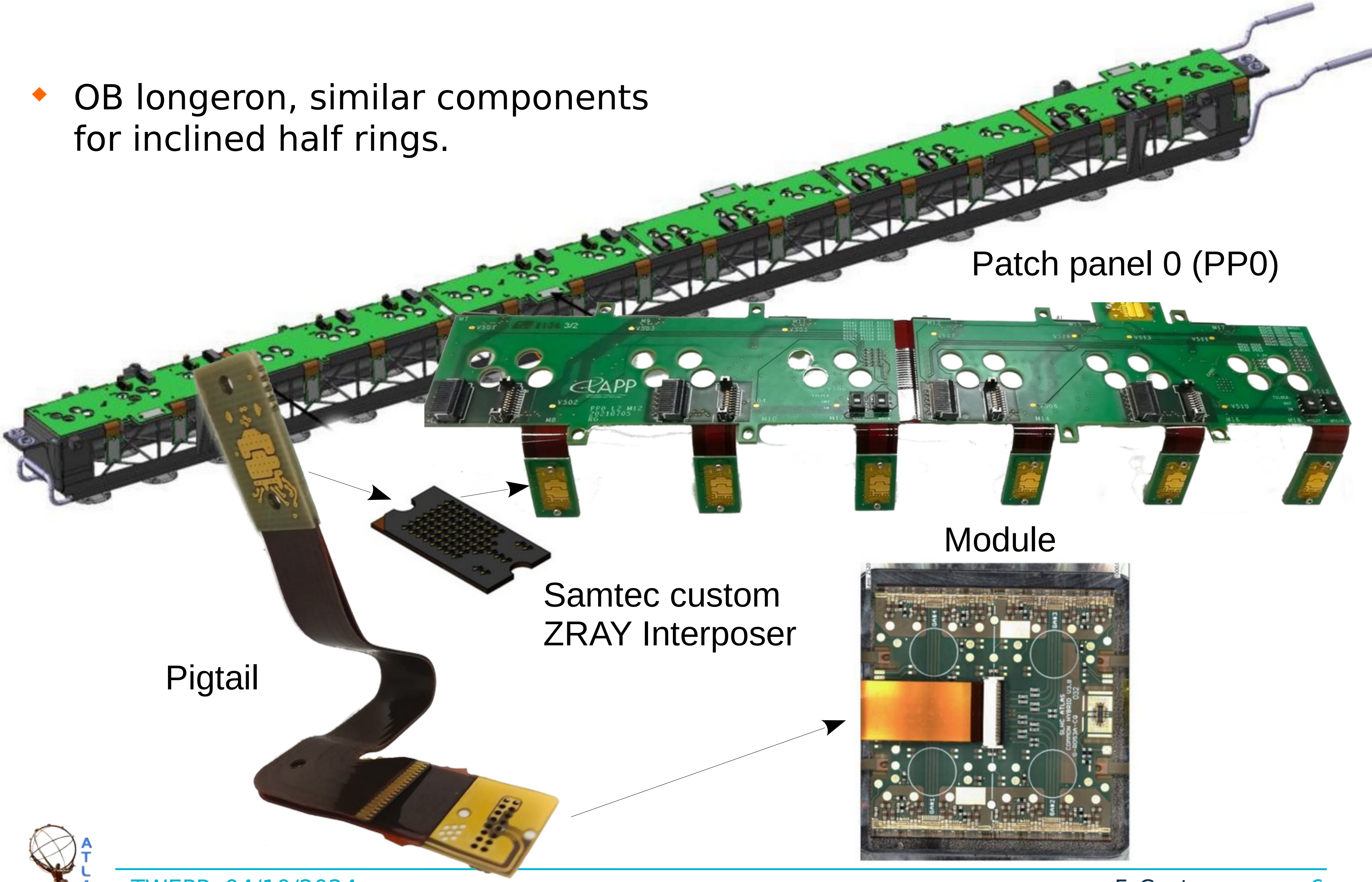
- Imposed maximum envelope.
- Bending → take bending into account for copper routing.

Manufacturing constraints

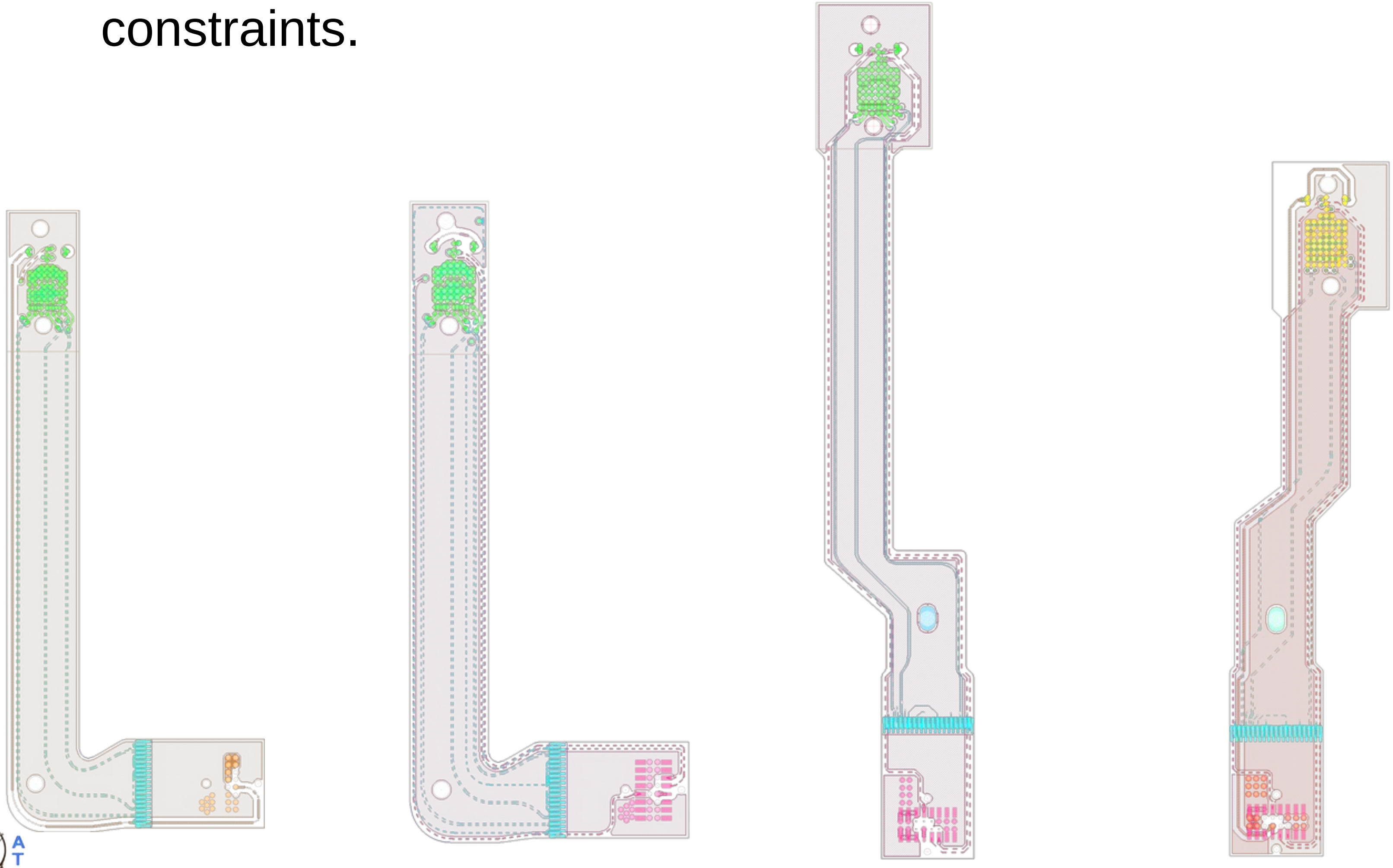
- Withstand 250 Mrad → halogen-free materials.
- NiAu finish.

ITk-OB on-detector services

- OB longeron, similar components for inclined half rings.

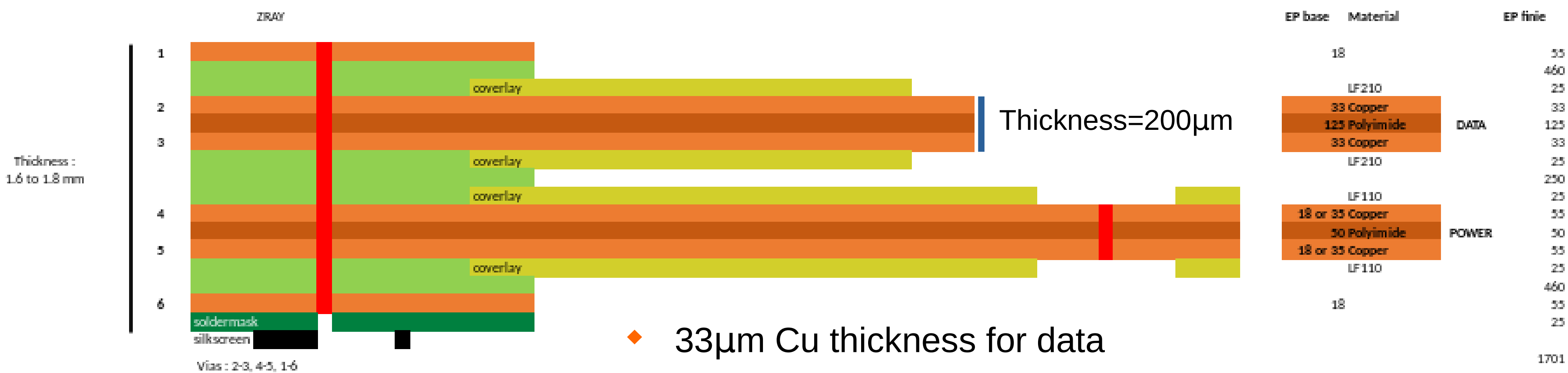


- Four outlines, to fit all layers (only bending change)
  - Special outline for last half ring only due to mechanical constraints.

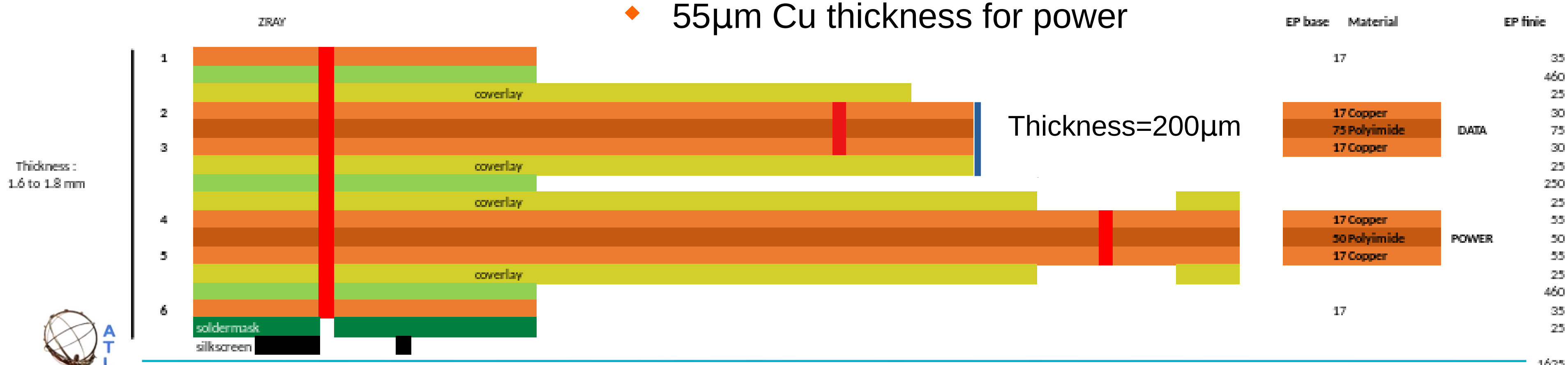


Pigtail stack-up

- Multiflex-rigid printed boards (non standard)
- 2 manufacturers → 2 close (yet different) 6L stack-ups
  - flat section → TechCI (France) (dual entry ZIF)
  - inclined section → CERN (via in flex data)



- 33µm Cu thickness for data
- 55µm Cu thickness for power



Patch Panel 0 outline

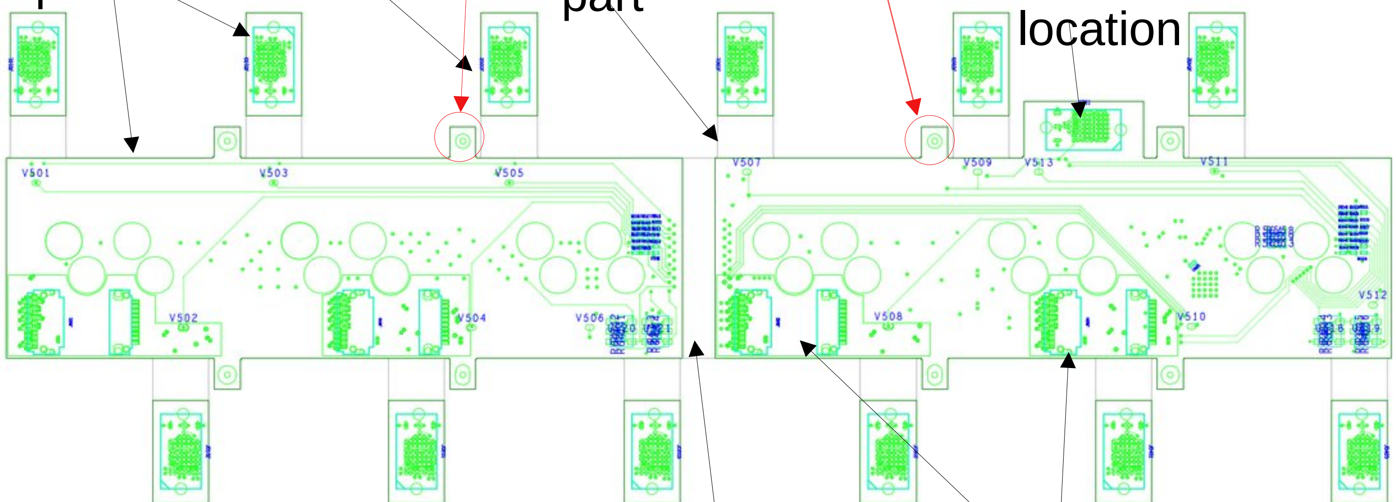
only 2 precise round holes (others are oblong)

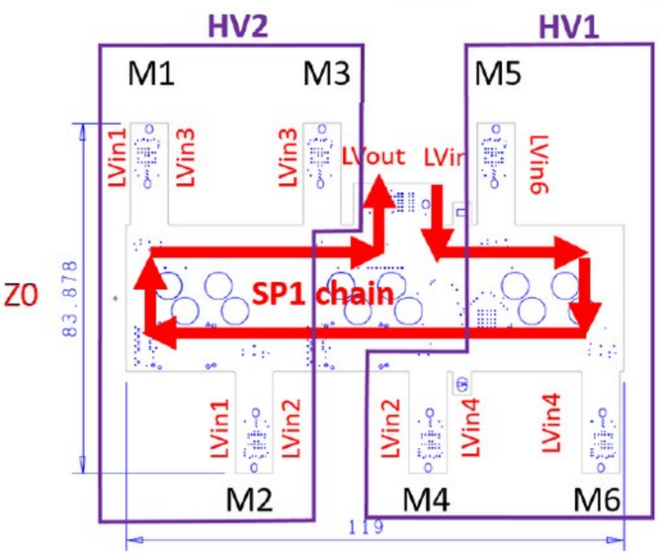
rigid part

wing

flex part

type 1 bundle location





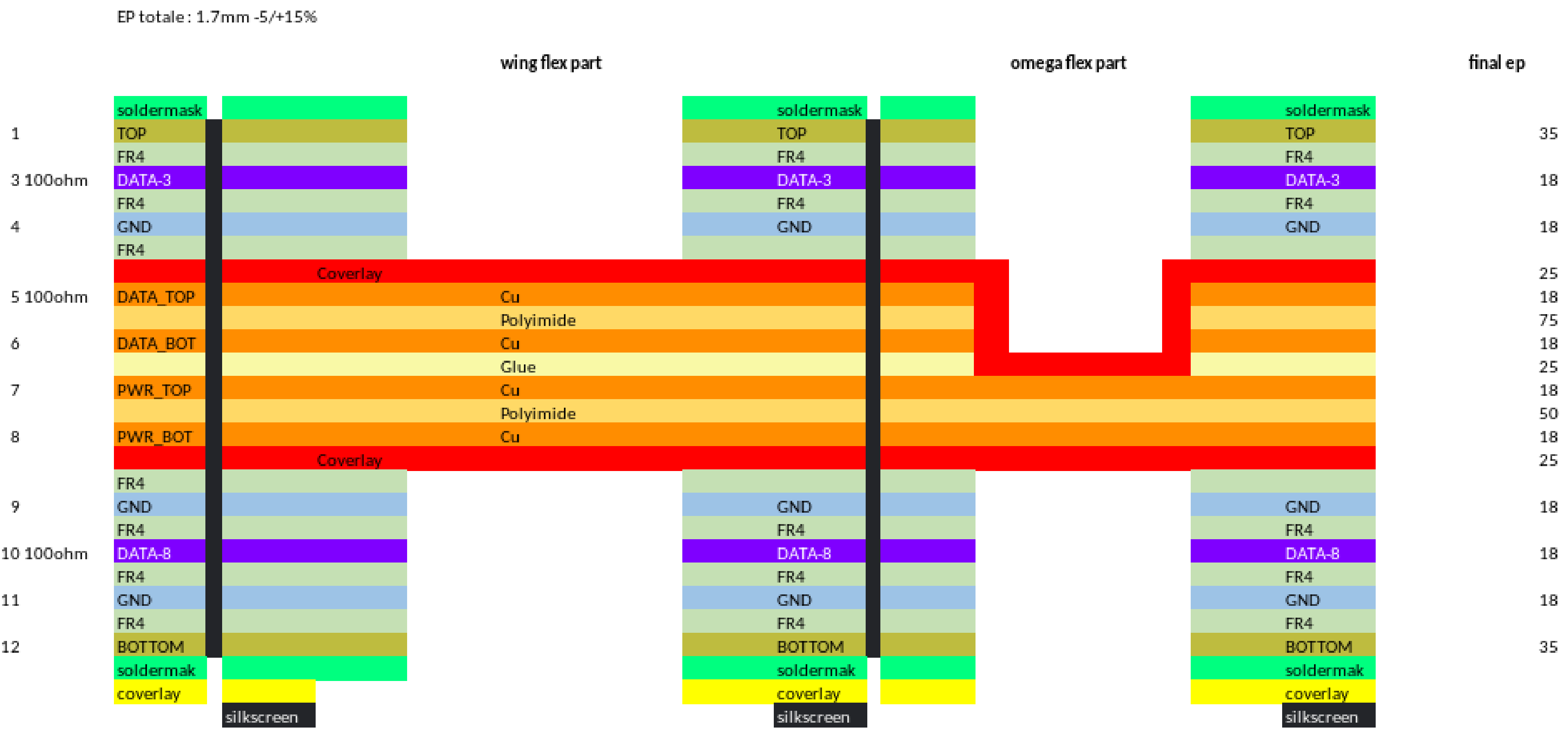
«omega» folding (flex part) to absorb mechanical stress

Ω

type 1 data connector location

Patch Panel 0 stack-up

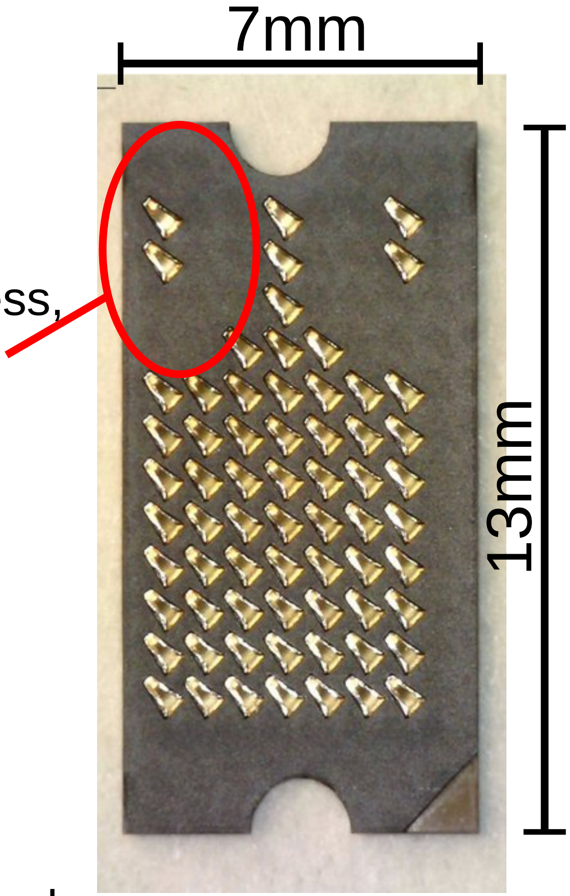
Same stackup for all flavors (except no "omega" on M6).



- 18µm Cu thickness for data and power

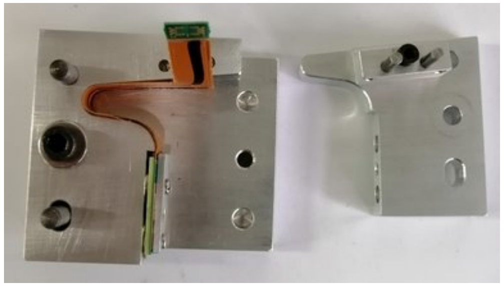
The ZRay: connection between pigtail and PP0

- **Provider**: Samtec.
- **Technology**: connector based on contact matrix.
- **Main advantages**: high density, high speed, small thickness, low contact resistance, secured by insert+screw.
- **Custom ZRay**: to solve withstanding voltage requirement.
- **Test plan**:
  - Main conventional tests: test report from Samtec.
  - HV tests: Min. breakdown voltage = 2.4kV
    safety margin > x2
  - Radiation hardness : protons & gamma up to 250MRad
    no mechanical or electrical impact.

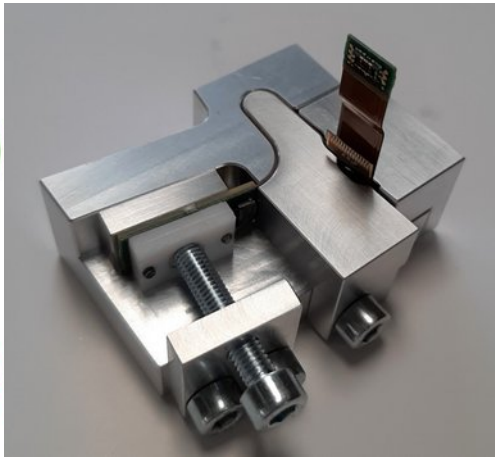


Flex circuit bending

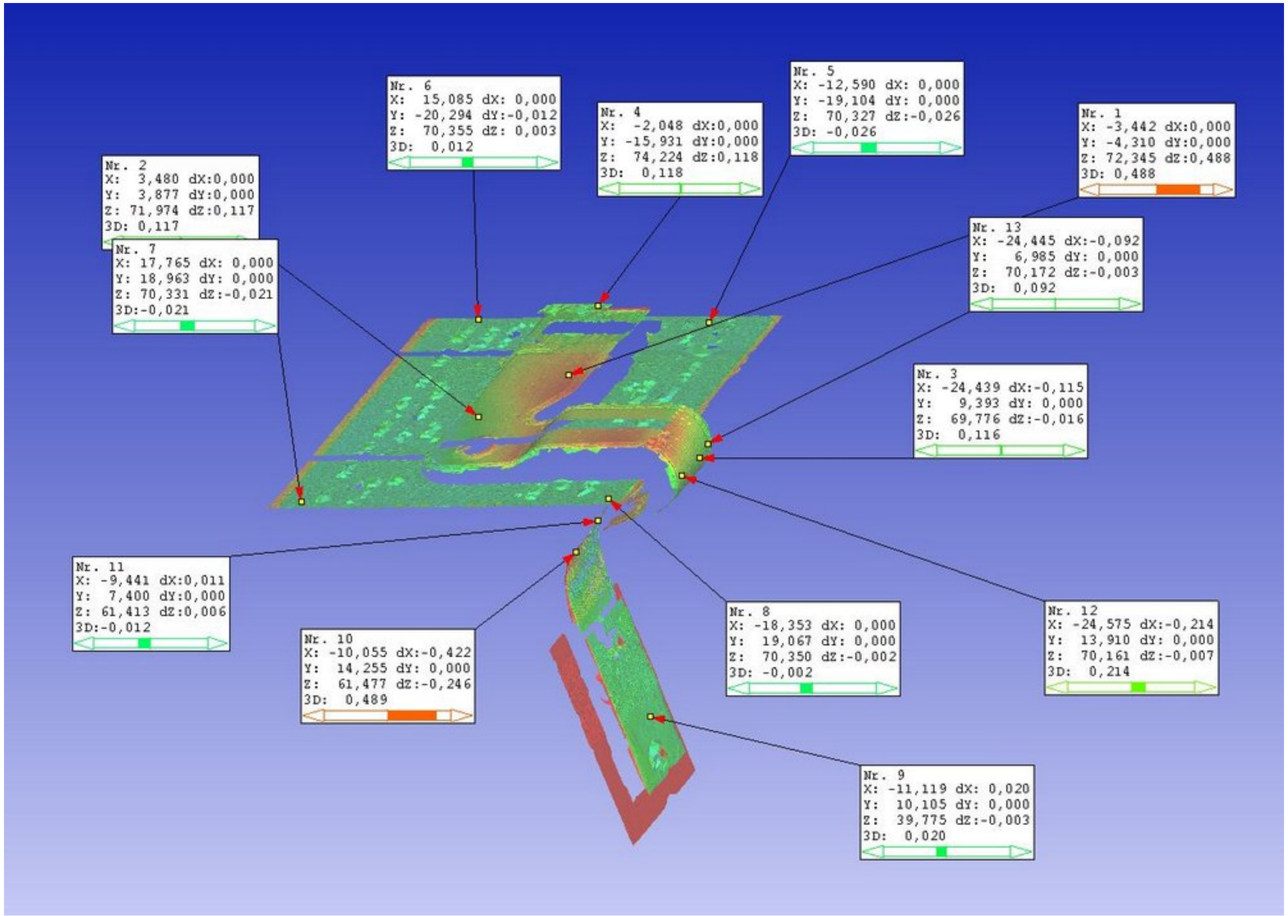
- A lot of parameters in the game: copper thickness, stack-ups and materials, angles, lengths between angles, baking temperature, baking time, cooling time, storage…
- We learned from experience that extrapolation rarely works.
  - Several prototypes and iterations needed.
  - From first prototypes to last ones, we identified compensation factors: less linear with thinner Cu layers.



- The thicker the copper layer, the stiffer the pigtail and the lower are the spring effect & long term re-opening.
- If the pigtail is stiffer, a not well controlled re-opening can bring to an higher force applied between the module and the PP0.



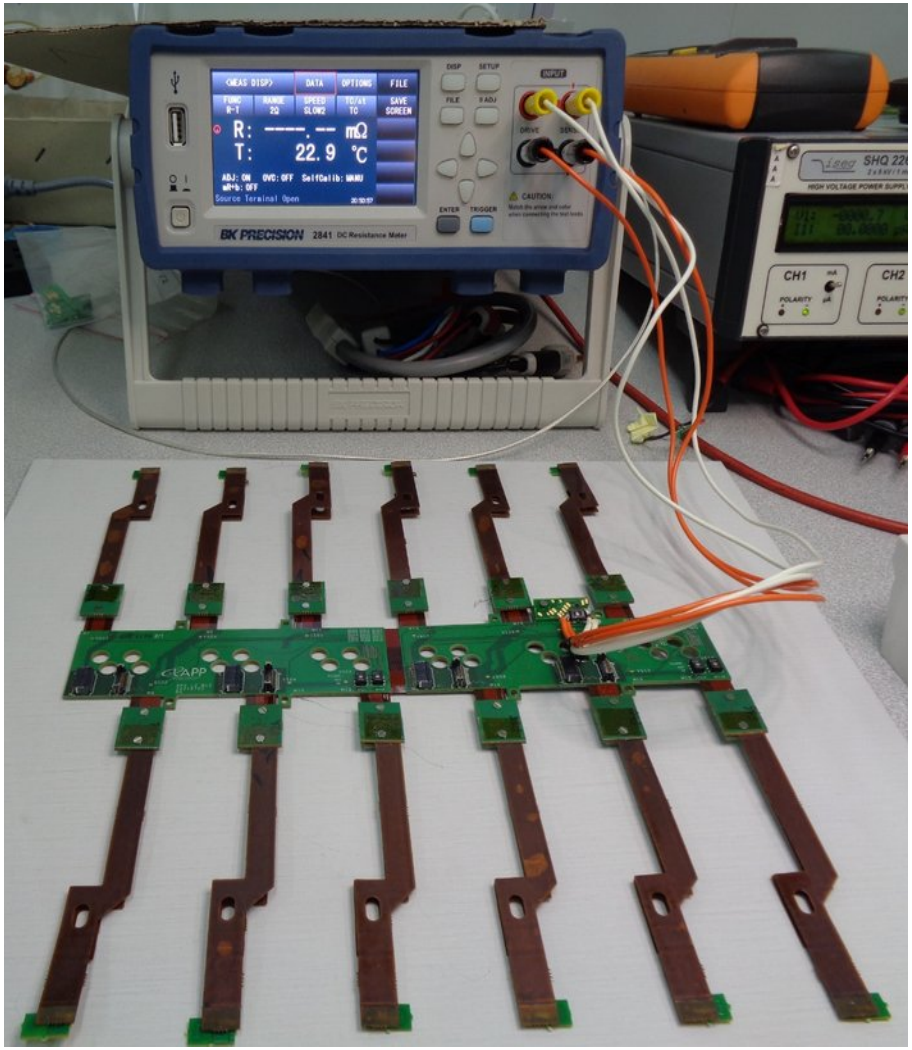
- Metrology measurement with bent pigtail locked on nominal position on module side (data+power) and on wing side.
- **Comparison with 3D CAD model**: differences less than ***500µm overall***, and less than ***100µm on critical parts***. Consistent with envelope.



- 4 wires resistance measurement of the full serial powering chain including:
  - The PCB connection to PP0
  - PP0 board
  - All pigtails with ZRay connectors
  - A PCB to short the LV line at the module side.
- Results:
  - **PP0 M6 + pigtails : 135mΩ**
  - **PP0 M12 + pigtails : 185mΩ**

To be compared to **allocated power budget:**

- **Short + long SP chains = 400mΩ**

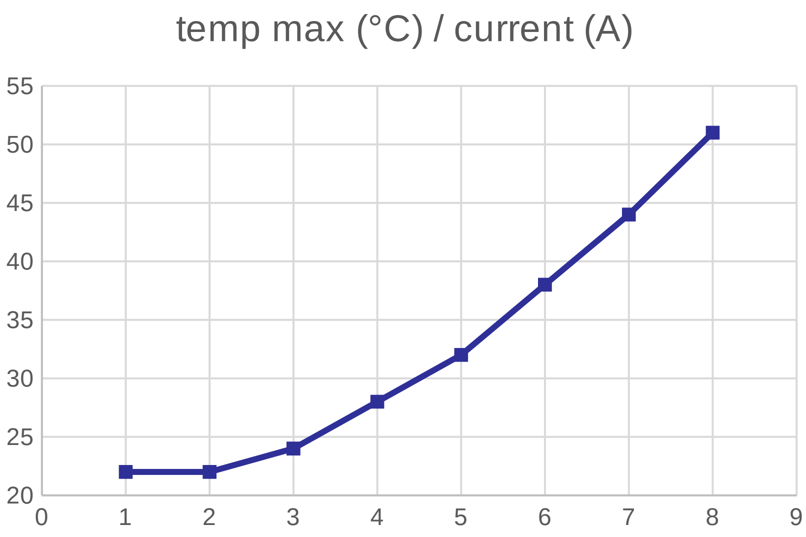


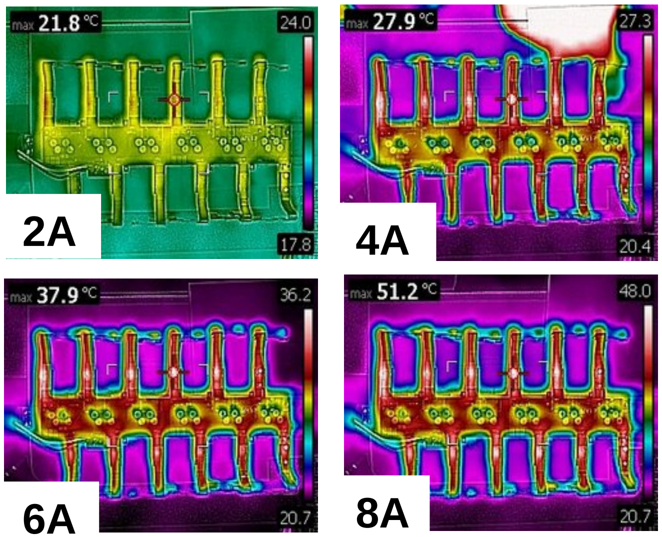
LV current vs Temperature

- On a test bench at room temperature, with no cooling, we circulated up to 8A in the full serial powering chain (in steps of 1A), waiting for the thermal equilibrium to be reached before taking a picture of the setup with a thermal camera.

- Results:
  - At 6A (expected operational current): hot spot at 38°C, temperature increase of 15°C.
  - **Temperature homogeneous** on the full surface, rigid and flex.
  - Hot spot: ZRay connector area.

- Conclusion:
  - No bottleneck in the designs.
  - Homogeneity of the PCB manufacturing.



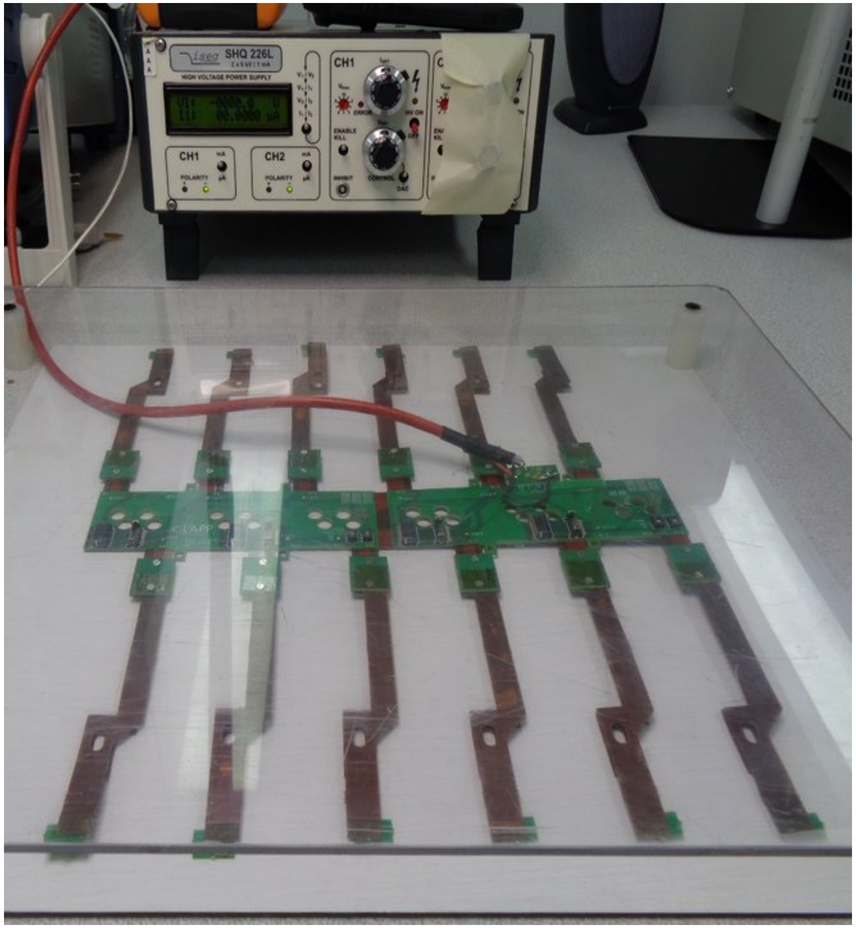


Dielectric Withstanding High Voltage

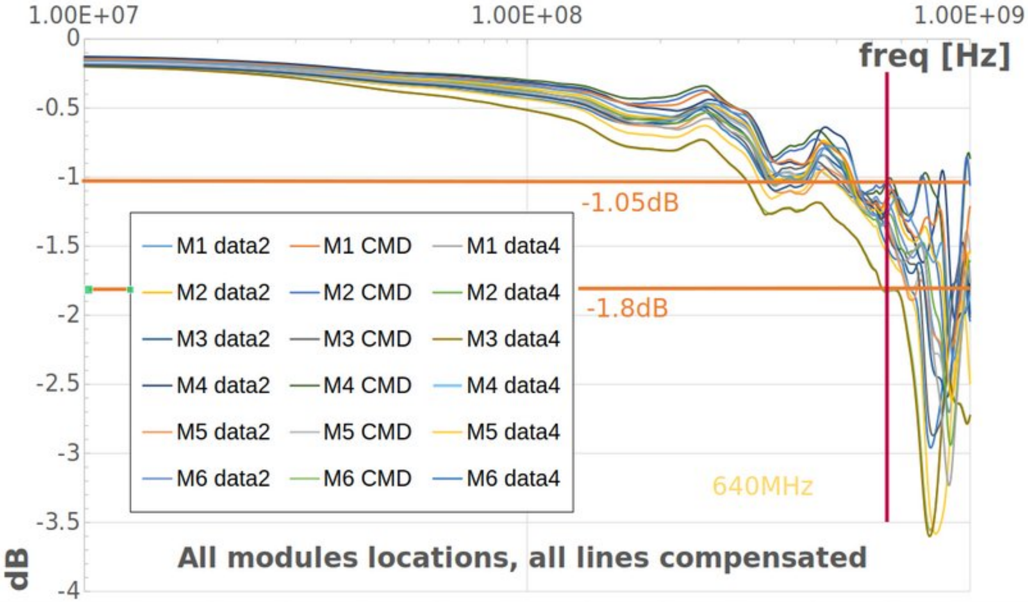
- Use the expected end-of-life operation voltage of 850V as reference.
  - 10 PP0 M6 tested at 850V for 1min
    - Leakage current: 0 – 5nA.
  - 5 PP0 M12 tested at 850V for 1min
    - Leakage current: 0 – 7nA.

Dielectric Breakdown Voltage

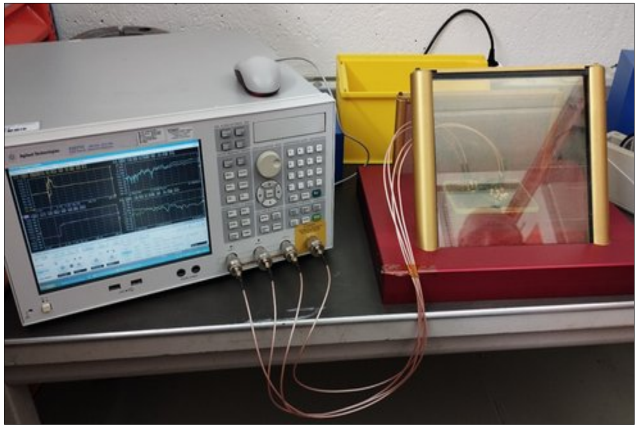
- Threshold set at 1.2kV (1.5x end-of-life operation voltage)
  - PP0 M6 breaks at 1.65 kV.
  - PP0 M12 breaks at 1.8 kV.



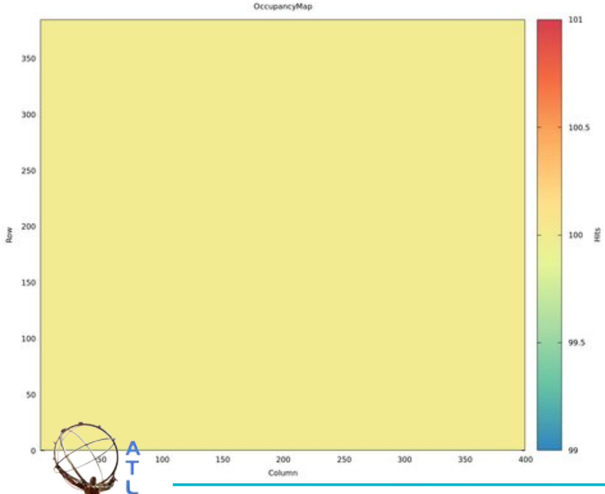
- Transmission loss (S21): TOP pigtail + PP0
  - Two differential data pairs and one CMD pair tested on all module positions.
  - Compensation applied to take into account test boards.
- Results: Averaged loss is **-1,5dB** and the maximum is **-1,8dB**.
  To be compared to the requirement of -20dB for type0+type1 total loss.

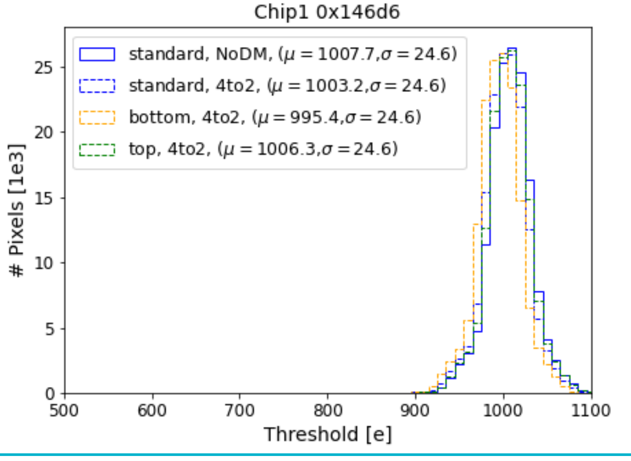


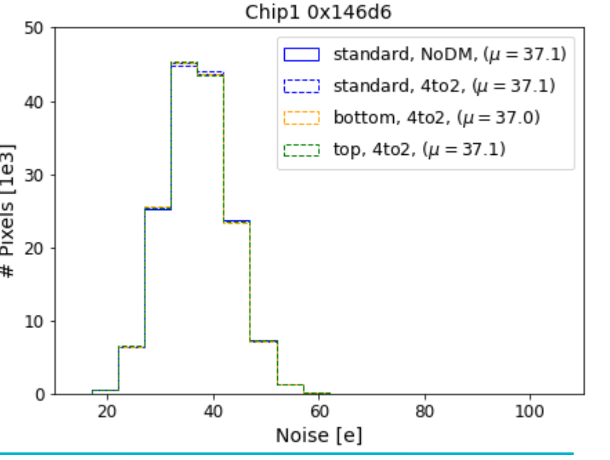
- Radiation effects were also checked.
- Pigtails irradiated 24GeV *p*, 6,63E+15 Protons/cm², TID=~1.5MGy.
- Negligible transmission loss degradation **~0.08dB**.



- Digital ITKPix v1.1 quad module
- Pigtails tested: standard OB (**reference**), pre-production BOTTOM and a TOP.
- Readout system: PC with Trenz board, YARR fw v1.4.0 w/ rx speed 1.28Gbps, YARR sw v.1.5.1.
- Results:
  - Occupancy maps for a digital and analog scans run successfully with no missing hits.
  - Threshold and noise scans with pre-production pigtails show no differences w.r.t. reference.







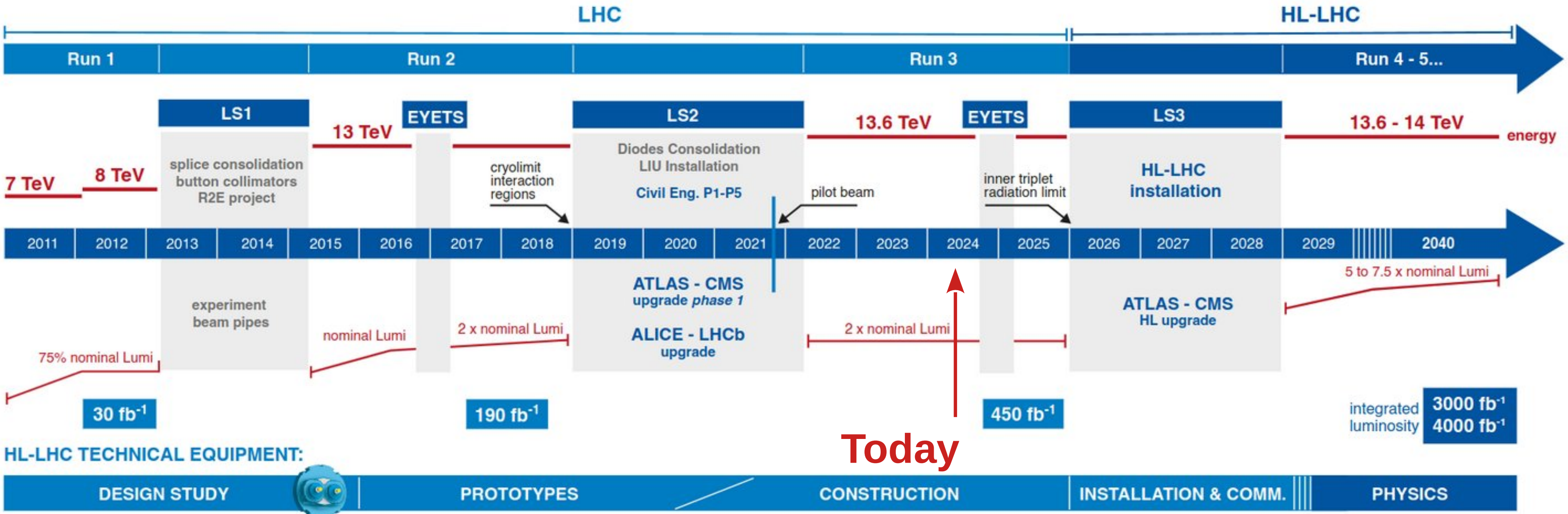
Conclusions

- The design and production of on-detector services of the ITk Pixel Outer Barrel was presented.
- The tests on the pre-production (10% of what is needed to equip the final detector) show good agreement with the requirements.
    - At LAPP, yield > 99% (one bad pigtail / 260 due to a cabling problem).
        - NB: several electrical tests already run by the manufacturer and only good items are delivered, production yield not known.
- The complex procedure of 3D bending is well under control as shown by metrology measurements.

Looking forward to starting production in the Q1 of 2025!

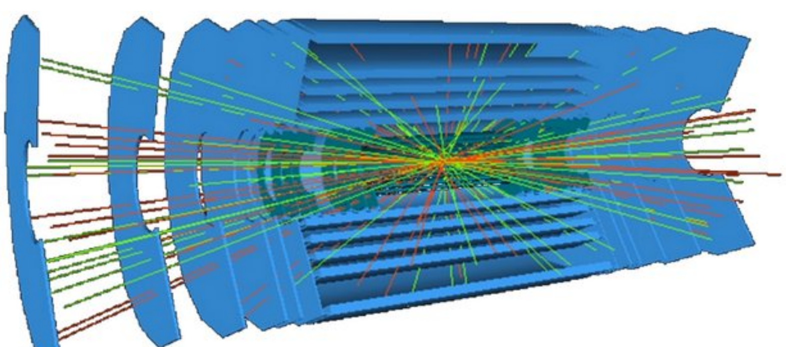
Bonus Slides

The High-Luminosity LHC Upgrade

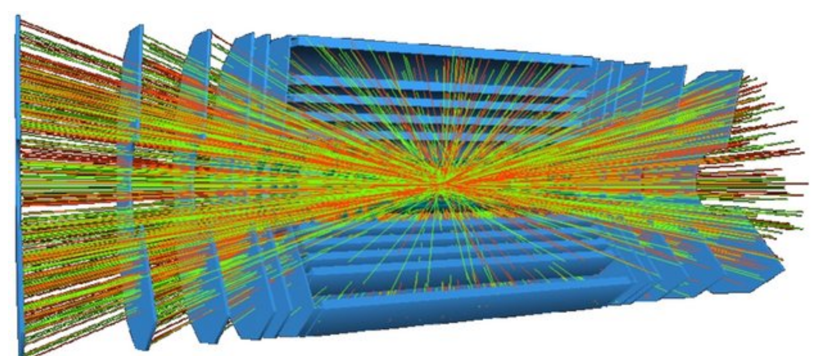


NB: discussion ongoing to extend Run3 by one year

LHC: Inner Detector (ID), made of Pixels + Strips + TRT	HL-LHC: New all-silicon Inner Tracker (ITk), made of Pixels + Strips

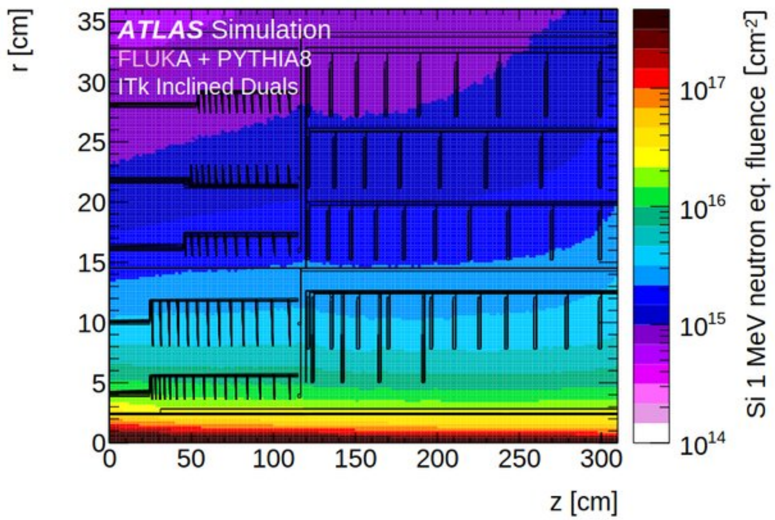


19 – 55 pileup events



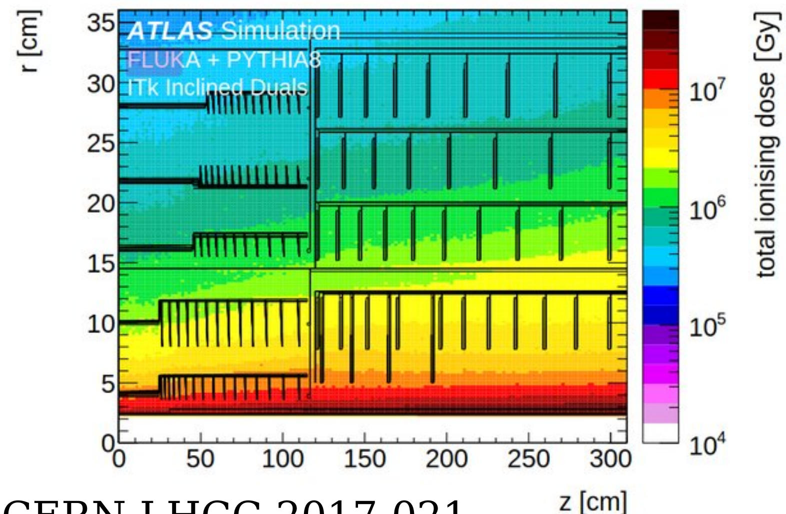
140 – 200 pileup events

- **Goal:** maintain (or improve) current ID tracking performance in the harsher HL-LHC environment.



- **Instantaneous conditions:**
  - Increased pileup, high event rate increased occupancy

- **Integrated effects:**
  - x10 increase radiation damage.
  - Particle fluence up to **2×10^{16} n_{eq} cm^{-2}** Total ionizing dose (TID) up to **1MGy**.



CERN-LHCC-2017-021

Type0 eye diagram: TOP pigtail+PP0

Tests performed on all 6 M6 PP0 module positions.
Eye diagram @1,28Gbps.

Averaged value for jitter RMS: **11ps**
Averaged value for jitter P-P: **55ps**
Averaged opening factor: **87%**
The dispersion on all measurements is very low.

These results are overestimated because test boards contributions can't be compensated for eye diagram test.

	cmd average	cmd sigma	data2 average	data2 sigma	data4 average	data4 sigma
Opening Factor	0,86716309	0,00697384	0,873722934	0,0066694	0,861210201	0,01206283
Signal / Noise	7,5449379	0,38667663	7,938089442	0,43202774	7,25173374	0,6453597
Rise Time	4,6772E-10	5,8024E-11	4,37417E-10	3,2963E-11	5,13069E-10	6,2238E-11
Fall Time	4,4577E-10	3,9224E-11	4,25195E-10	1,9668E-11	4,96741E-10	6,0744E-11
Jitter (PP)	5,6739E-11	4,6105E-12	4,70749E-11	2,4429E-12	5,54954E-11	5,3101E-12
Jitter (RMS)	1,1348E-11	9,2209E-13	9,41498E-12	4,8857E-13	1,10991E-11	1,062E-12
Cross Point (%)	49,7180062	0,20800776	49,79491194	0,14304749	49,84306772	0,22725899