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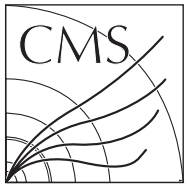

The Compact Muon Solenoid Experiment

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Data transmission performance and characterization of TEPX disks of the CMS Phase-2 Inner Tracker

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Abstract

Before starting the High-Luminosity LHC phase, the CMS detector will be substantially upgraded to cope with the significant increase in instantaneous and integrated luminosity. The entire CMS tracking detector will be replaced, and the new detector will feature increased radiation hardness, higher granularity, and the capability to handle higher data rates and longer trigger latency. In this contribution, we will present the new TEPX detector, a large forward disk detector, with a focus on the characterization of the disk printed-circuit board regarding data transmission quality, as well as the initial tests conducted on a disk prototype.

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Data transmission performance and characterization of TEPX disks of the CMS Phase-2 Inner Tracker

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Abstract: Before starting the High-Luminosity LHC phase, the CMS detector will be substantially upgraded to cope with the significant increase in instantaneous and integrated luminosity. The entire CMS tracking detector will be replaced, and the new detector will feature increased radiation hardness, higher granularity, and the capability to handle higher data rates and longer trigger latency. In this contribution, we will present the new TEPX detector, a large forward disk detector, with a focus on the characterization of the disk printed-circuit board regarding data transmission quality, as well as the initial tests conducted on a disk prototype.

Keywords: CMS, HL-LHC, TEPX, Phase-2 Upgrade

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1 Introduction

During Long Shutdown 3, the LHC will be upgraded and enter its High-Luminosity era (HL-LHC), allowing LHC experiments to greatly increase their collected data samples, enabling more precise measurements and enhancing the potential to observe rare processes. It will feature an increased instantaneous luminosity of up to $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, while the number of simultaneous proton-proton collisions per bunch crossing, called pileup, will increase to 200. This increase in instantaneous luminosity will enable the CMS experiment [1] to collect up to 4000 fb^{-1} of integrated luminosity by 2041.

In order to cope with increased data rates and overall more challenging operational conditions expected in the HL-LHC era, CMS will undergo an upgrade known as Phase-2 Upgrade, with its pixel detector completely replaced by the Inner Tracker (IT) [2], continuing its role in pushing the frontiers of particle physics. The IT will come with increased radiation tolerance, increased granularity to maintain low occupancy also in the presence of the higher number of pileup interactions, larger bandwidth to accommodate higher data rates, as well as extended coverage up to $|\eta| \approx 4$ which will improve the physics reach of the CMS experiment in the forward region [2].

The IT will be subdivided into three subdetectors: Tracker Barrel Pixel Detector (TBPX), Tracker Forward Pixel Detector (TFPX), and Tracker Endcap Pixel Detector (TEPX) (Fig. 1). The TEPX will consist of four substructures per end. Each structure consists of two so-called double-dees. Each dee is made of two printed circuit boards (PCBs) glued to carbon fiber sheets with carbon foam and titanium cooling tubes between the two sheets [3, 4]. A total of 44 modules with 2x2 CROC ASICs, bump bonded to a silicon sensor, is used to populate a dee [5, 6].

In these proceedings, threshold and noise levels of the CROCv1 modules on a standalone PCB and on a disk prototype will be described along with the calibration sequence. Furthermore, the bit error rate (BER) measurements — defined as the ratio of erroneous bits received to the total number of transmitted bits — will be presented and compared for both the standalone PCB and a disk prototype.

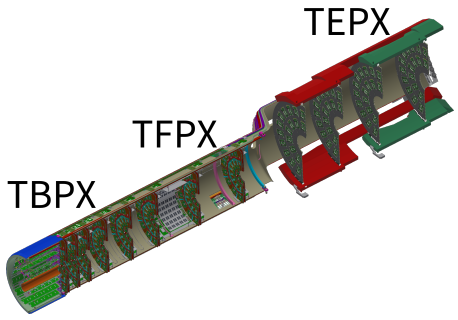


Figure 1: CMS Phase-2 Inner Tracker [2].

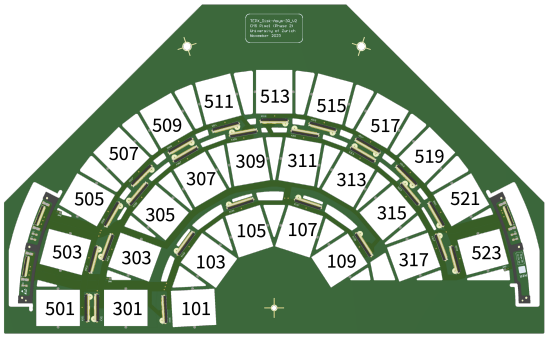


Figure 2: Asymmetric 3-ring PCB layout with position IDs indicated - one of the four dee layouts implemented in TEPX.

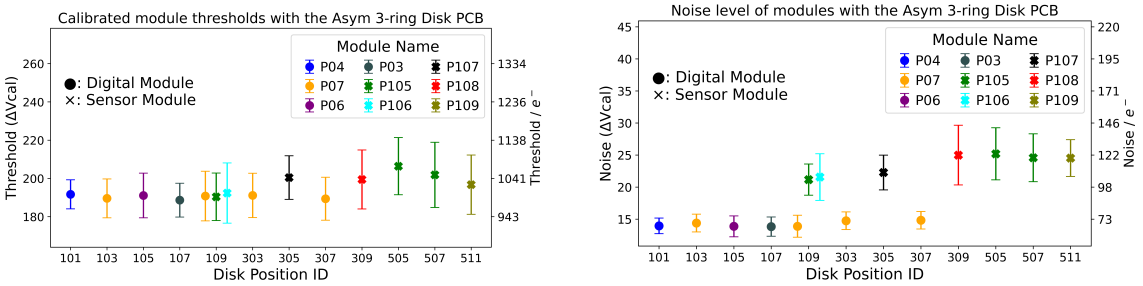
2 Threshold and noise levels of CROC modules

In order to properly operate CROC modules, they need to be calibrated by adjusting and equalizing threshold levels between pixels, as well as by masking the noisy ones. To tune the modules to the target threshold of 1000 e^- a sequence with the following steps is carried out. First, voltage tuning is performed to establish the optimal analog and digital voltage trimming settings for chip operation. The threshold is then tuned using the global threshold DAC bias (GDAC). This is done for values of 2000 e^-, 1200 e^-, and finally 1000 e^-. For the first two thresholds the pixels are trimmed to the same threshold and a combined charge-injection delay scan is performed. For all threshold steps noisy pixels are masked at the end of the procedure. After achieving the threshold target, an S-curve measurement, documented in Ref. [7], is also performed to verify that the calibration was completed as expected.

2.1 Standalone PCB

To validate the PCB performance, the tuning sequence has been repeated with modules placed in multiple different positions on the PCB. The setup for these tests consisted of the PCB that was taped to a metal plate. The PCB delivers power to the mounted modules, transmits input commands to them and the data from them to so-called portcards, which house auxiliary electronics like the low-power Gigabit Transceiver (lpGBT) and the Versatile Link Plus (VTRX+). The data are converted to an optical signal and transmitted to the back-end electronics through an optical fiber. The FC7 readout board is used to send commands to and collect data from the modules. The standalone PCB was populated with up to ten modules and placed inside a climate chamber and cooled to −40 °C.

The tests used both "digital modules", composed of only four read-out chips, and "sensor modules", which consist of a sensor flip-chip bonded to four chips. As can be seen from Fig 3, thresholds for both digital and sensor modules could be tuned to 1000 e^-, regardless of the module position on the PCB. The system displays consistent, low noise levels across all positions on the PCB. Digital modules have noise levels of around 70 e^-, while sensor modules display slightly higher noise levels of 100–120 e^-.



(a) Threshold levels per position.

(b) Noise levels per position.

Figure 3: Threshold and noise levels per position for a standalone PCB (also reported in [8]).

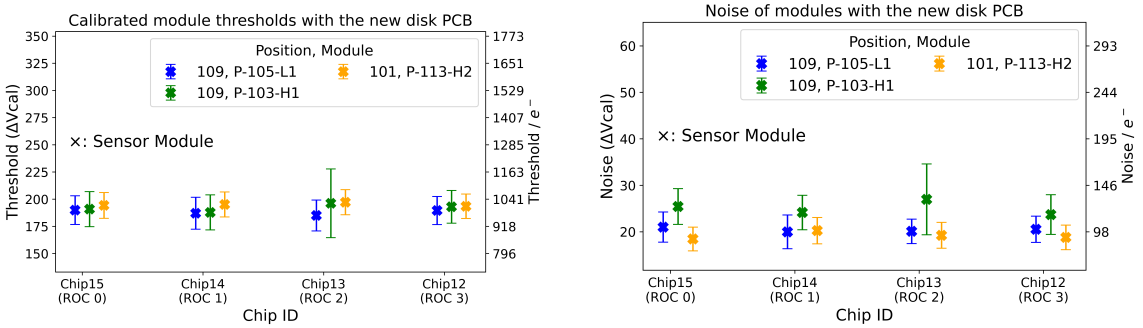
2.2 Disk prototype

For tests on the disk prototype, a similar approach was adopted and the first such results are presented in the following. The test setup for the prototype disk relies on the same readout hardware but uses CO_2 cooling, circulated though the inbuilt titanium cooling tubes, to cool the disk to −30 °C.

Results of the tuning of different sensor modules in different positions can be seen in Fig. 4. Conclusions are similar to those for the standalone PCB case: thresholds can be tuned to 1000 e^- regardless of module and position, while noise levels remain low at 90–120 e^-.

3 Bit error rate

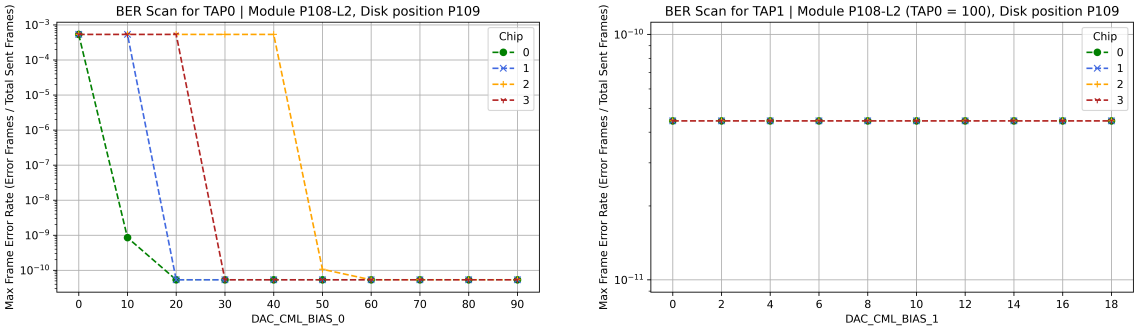
Data transmission quality is a key feature of the readout electronics in any detector, indicating the extent of data loss in transmission lines and directly impacting the overall detector performance. The CROC modules use four independent current-mode logic differential output drivers with programmable pre-emphasis for signal transmission. The signal shape can be modified by adjusting three dedicated registers, referred to as TAPs, which control the difference in voltage between the differential lines when transmitting the signal. TAP0 controls the amplitude of the base signal with 10-bit resolution , while TAP1 and TAP2 act on pre-emphasis characteristics of the transmitted



(a) Threshold levels per position.

(b) Noise levels per position.

Figure 4: Threshold and noise levels per position for the disk prototype.



(a) BER scan for TAP0.

(b) BER scan for TAP1 with TAP0 = 100.

Figure 5: An example of a BER scan of TAP0 and TAP1 with a fixed TAP0 for a standalone PCB.

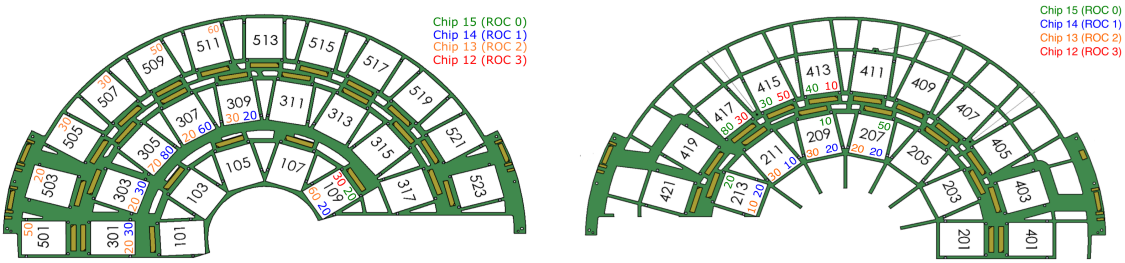
pulse with 9-bit resolution. The maximum current that each TAP can control is approximately 14 mA [2].

To determine the quality of the data transmission for TEPX, a series of BER tests have been performed to scan for the values of the TAPs where the BER goes below 10^{-10}. The BER tests consist of transmitting a series of 32-bit frames, generated using the PRBS7 algorithm, implemented in the CROC chip, from the module to the back-end. Since the PRBS7 algorithm is fully deterministic, the number of flipped bits can be inferred. The lpGBT has the ability for forward error correction which helps to reduce the BER rate [9].

3.1 Standalone PCB

An example of the BER scan for the standalone PCB is presented in Fig. 5. Each of the points corresponds to the same number of frames transmitted. In most cases this represents an upper limit for the BER as not a single erroneous frame was detected. When the frame error rate goes below 10^{-10} for a certain TAP0, this is called a saturation point. As it can be seen from the figures, the BER saturates for values of TAP0 well below 10% of the maximum. Because of the early saturation onset, a pre-emphasis in the form of TAP1 does not further improve the results.

The maps of all saturation points per disk position for the standalone PCBs are shown in Fig. 6. In all rings, saturation points are reached at TAP0 values below 100, even for the longest data lines locations at positions 109, 309, and 413 for ring 1, 3, and 4, respectively.



(a) Asymmetric 3-ring PCB.

(b) Asymmetric 2-ring PCB.

Figure 6: TAP0 saturation points for standalone PCBs.

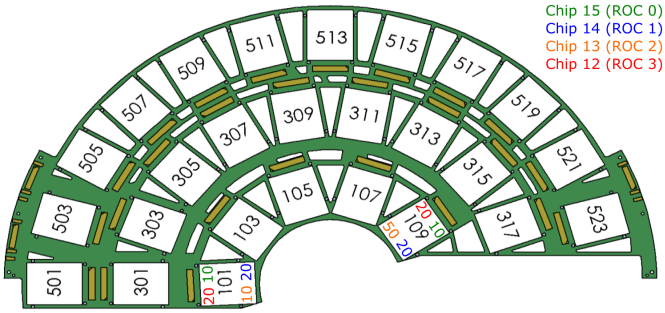


Figure 7: TAP0 saturation points for the disk prototype.

3.2 Disk prototype

The BER results for the disk prototype are very similar to those of the standalone PCB and yield the same conclusion: due to early saturation onset, a pre-emphasis is not needed. The map of the saturation point per measured position is shown in Fig. 7. When fully powering the two PCBs on each face of the disk, populated with a mix of dummy and sensor modules, BER saturation points are again reached at TAP0 values lower than 10% of the maximum. Although a limited number of measurement points is available, a direct comparison of position 109 between the standalone PCB and the disk prototype indicates very similar performance with the disk prototype results slightly better with the BER saturating at lower values of TAP0.

4 Summary

This contribution presents the data transmission performance on the TEPX dees as measured with the PCB that is used for the signal routing standalone and when attached to the first disk prototype. Several CROC modules could be tuned to a threshold of 1000 e^- on both the standalone PCB and the disk prototype across all tested positions, demonstrating consistent noise levels of approximately 70 e^- electrons for digital modules and around 100 – 120 e^- for sensor modules. A BER scan was conducted, revealing that even with the longest transmission lines, the BER saturated below 10^{-10} for less than 10% of the maximum available current. Due to this early saturation of the BER, applying an additional pre-emphasis to the signal was not necessary.

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