The Hardware implementation and Testing of the Full-function Global Common Module prototype for ATLAS Phase-II upgrade

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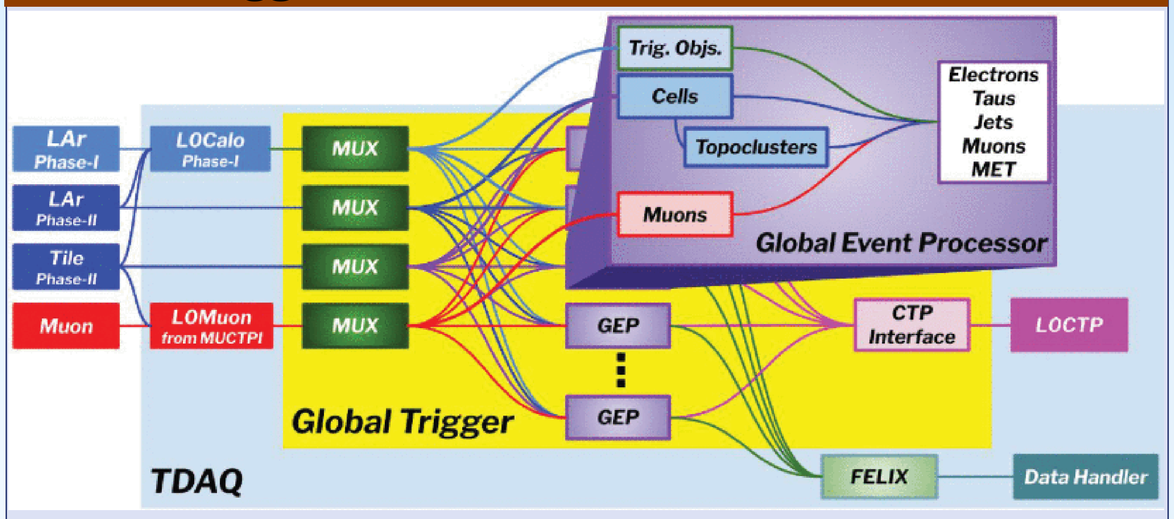
Abstract

The High Luminosity Large Hadron Collider (HL-LHC) is set to become operational in 2029, aiming to achieve instantaneous luminosities 5-7.5 times of the nominal value of the LHC. This poses significant challenges to the design of the Trigger and Data Acquisition systems. To address these challenges, a baseline architecture has been chosen for the ATLAS Phase-II upgrade, relying on a single-level hardware trigger known as the Level-0 Trigger. This trigger has a maximum rate of 1 MHz and a latency of 10 μs. The Global Trigger subsystem, the core of the Level-0 Trigger, performs complex algorithms, similar to off-line algorithms of Phase-I trigger, on full granularity calorimeter data. The Global Trigger is divided into three sublayers: the Multiplexer Processor (MUX) layer, the Global Event Processor (GEP) layer, and the Global to Central Trigger Processor interface (gCTPi). A full-function Global Common Module (GCM) hardware prototype has been designed to fulfill the requirements of all three sublayers of the Global Trigger, featuring different firmware loads. This GCM prototype, based on the ATCA form factor, incorporates two of the latest AMD (Xilinx) Versal Premium devices VP1802 and twenty Samtec 12-channel 25 Gb/s FireFly optical engines. These devices double the density of the Virtex UltraScale+ FPGA VU13P used in the previous design and include an integrated System-on-Chip (SoC) with a completely new architecture. The development of an ATCA blade with two large FPGAs and about 240 optical links running at 25 Gb/s is a very challenging task. The signal integrity, hardware design considerations, functionalities, and performance test results are presented here.

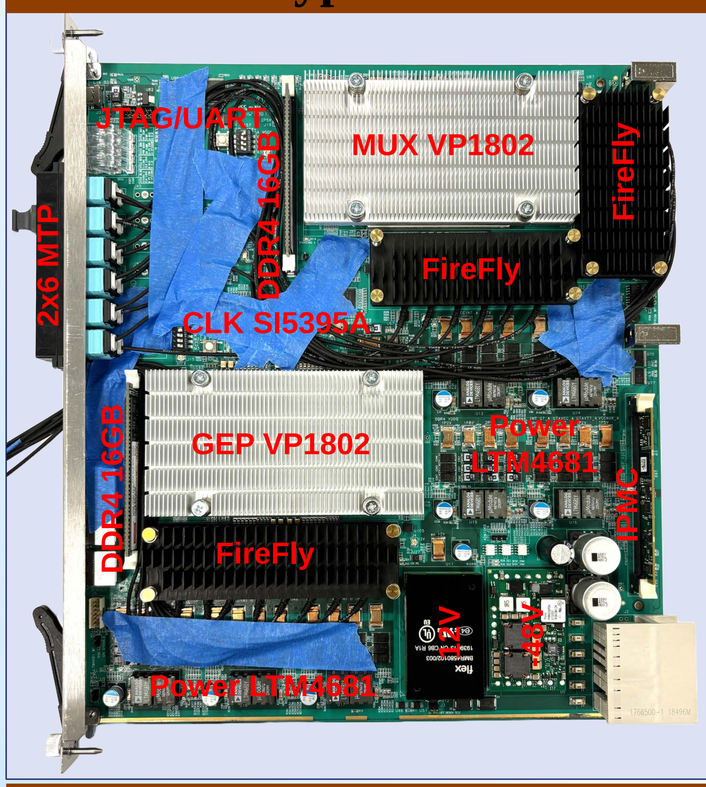
Global Trigger Architecture



The Global Trigger architecture is divided into three layers:

- ❑ MUX – Collects data from detectors (calorimeter and muon) and legacy Feature Extractor modules, time-multiplexes them bunch-crossing by bunch-crossing and sends full events to the GEP layer in a round-robin fashion.
- ❑ GEP - Receives the full event data pertaining to a particular bunch-crossing, executes complex algorithms, and sends the result TIPs (Trigger Inputs) to the gCTPi.
- ❑ gCTPi - Comprises a single node that selects and resynchronizes the TIPs from all GEP nodes before sending them to the CTP.

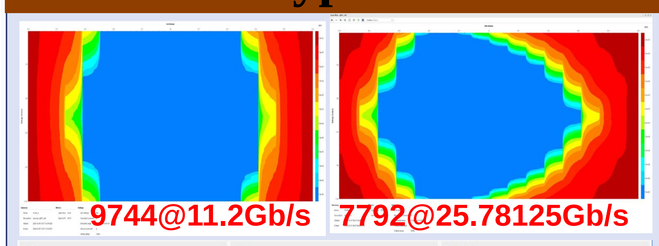
GCM Prototype v3 Hardware Design

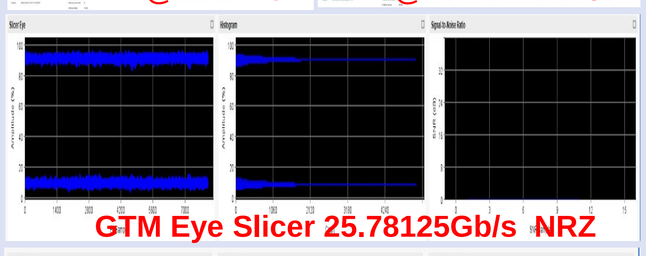


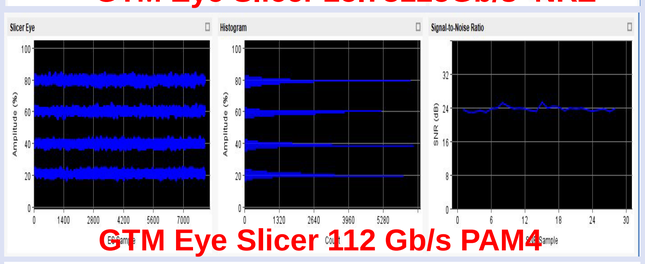
GCM is a single-slot ATCA board including:

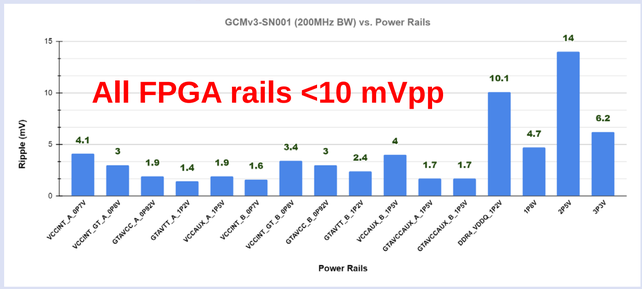
- ❑**Power Modules**: 1 PIM4328, 1 BMR458, 7 LTM4681 and 1 LTM4638.
- ❑**Versal FPGAs (APU included)**
  - 1 XCVP1802-1LSEVSVA5601 MUX
  - 1 XCVP1802-1LSEVSVA5601 GEP/gCTPi
- ❑**FireFly Modules**
  - 2 T24, 3 R24 and 1 Y12 for MUX
  - 1 T24 and 3 R24 for GEP/gCTPi
- ❑**GbE port:** IPMC, MUX and GEP
- ❑**USB-C connector:** 3 UARTs and 1 JTAG
- ❑**2 16GB VLP DDR4 UDIMM**
- ❑**2 SD card**
- ❑**2 SI5395A Clock generator**
- ❑**CERN IPMC**
- ❑**26 Layer with Backdrill and Via-In-Pad**
- ❑**EM890K Ultra-low loss PCB material**

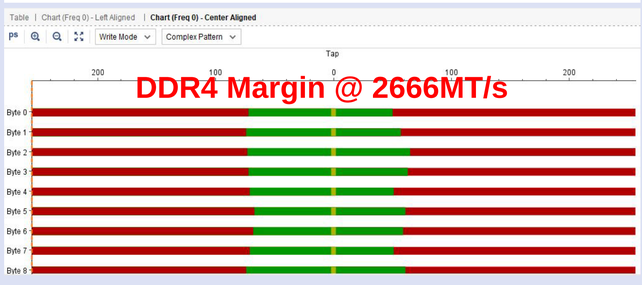
GCM Prototype v3 Test





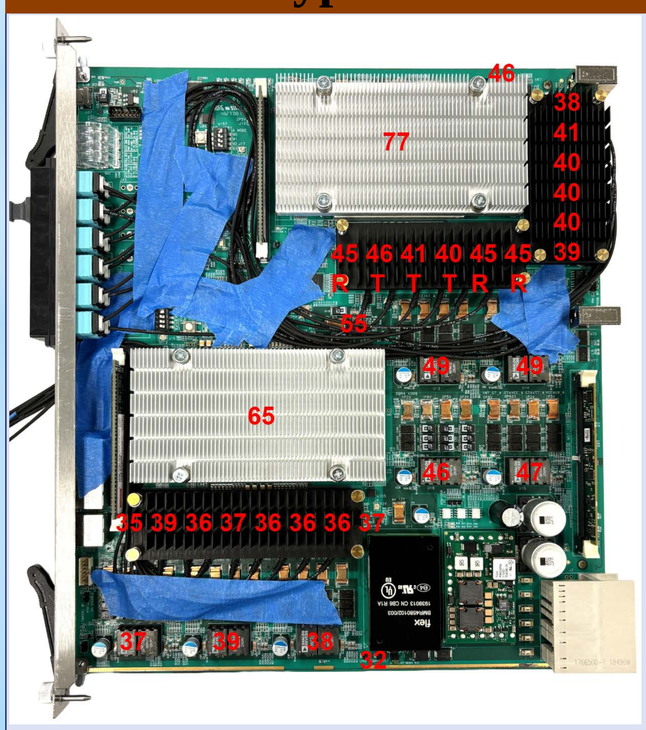


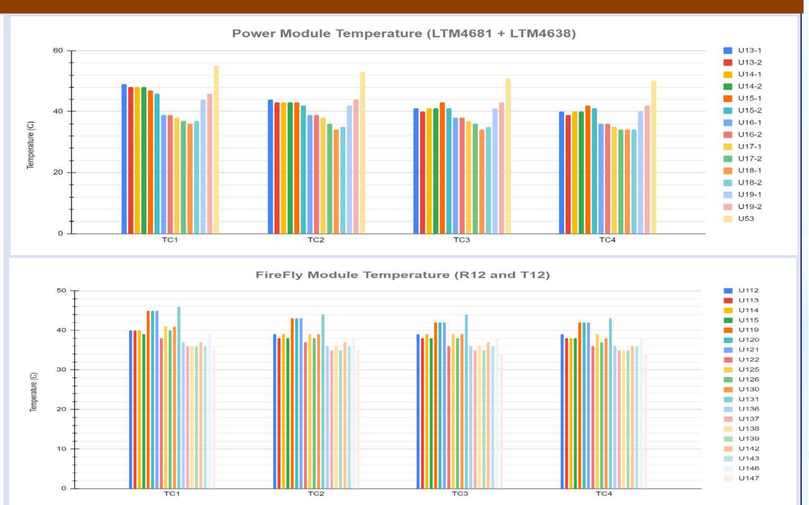


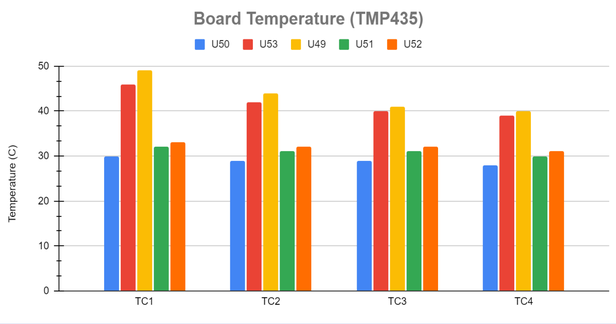


- ❑ **Functionalities have been successfully verified**:
  - ✓ Power sequence and monitoring by ADM1066
  - ✓ Power ripple and consumption
  - ✓ FTDI JTAG and UART
  - ✓ Alma Linux Boot from SD
  - ✓ SI5395A jitter and clock generator
  - ✓ GbE/I2C for monitoring and configuration
  - ✓ CERN IPMC for board management
- ❑ **MGT Performance Test:**
  - ✓ GTYP: Optical link are stable at 11.2 Gb/s and 25.78125 Gb/s.
  - ✓ GTM: All optical links are validated at 11.2 Gb/s and 25.78125 Gb/s. All onboard electrical link are stable up to 112 Gb/s at PAM4.
- ❑ **DDR4 Margin Test**
  - ✓ The DDR4 passed the test at 2666MT/s with around +/-70 ps margin

GCM Prototype v3 Power and Thermal Test







- ❑ **A dynamically configurable power consumption firmware has been developed.**
  - ✓ up to 150W/FPGA with 70% resource usage and down to 20W/FPGA with 5% resource usage
  - ✓ It can be used to simulate the different MUX and GEP firmware configurations
- ❑ **Four Typical usage case have been tested**:
  - ✓ TC1: MPV GEP (70%) + MPV GEP (70%) **~401W**
  - ✓ TC2: MPV GEP (70%) + MPV MUX(50%) **~344W**
  - ✓ TC3: MPV GEP (70%) + MPV MUX(30%) **~317W**
  - ✓ TC4: MEV GEP (50%) + MEV MUX(20%) **~275W**

Summary and Conclusion

- ❑ The GCM prototype v3 has been demonstrated all the challenging hardware technologies successfully, such as 25 Gb/s x12 FireFly optical modules, 25.78125 Gb/s NRZ and 112 Gb/s PAM4 with GTM on Versal FPGA, ~400W/board power consumption and thermal design.
- ❑ The GCM prototype v3 is currently being used for MUX and GEP firmware development.
- ❑ 5 GCM prototype v3 boards in total have been assembled and all passed the full functionality tests.
- ❑ All 5 GCM prototype v3 boards will be used for the 1/10 slice integration test for the Global Trigger system in 2025 at CERN.

2024 IEEE NSS MIC RTSD, Oct.26 –Nov. 2 2024, TAMPA , FLORIDA, USA