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DC-DC converters for the CMS MTD BTL and ECAL for HL-LHC

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Abstract: The Minimum Ionizing Particle Timing Detector (MTD) will be introduced in the Compact Muon Solenoid (CMS) experiment to measure the production time of Minimum Ionizing Particles (MIPs). Power Conversion Cards (PCCs) regulates and supplies low voltage to front end electronics of the MTD barrel, the Barrel Timing Layer (BTL). The PCCs host three radiation and magnetic field tolerant DC-DC converters. The physical height of the PCC is limited to 7 mm, having necessitated development of custom inductors and shields. Additionally, the CMS Electromagnetic Calorimeter will be upgraded. On-detector Low Voltage Regulator (LVR) cards host four DC-DC converters and one linear regulator. In these proceedings we will present both cards' designs evolution, stack-up and layout optimization, noise filtering choices and a performance evaluation.

Keywords: Analogue electronic circuits; Digital electronic circuits; Front-end electronics for detector readout; Radiation-hard electronics

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Contents

1 Introduction to minimum ionizing particle timing detector development and electromagnetic calorimeter barrel upgrade in the CMS experiment

The High Luminosity Large Hadron Collider (HL-LHC) will deliver up to 200 proton-proton interactions, with 14 TeV center-of-mass energies, over an estimated duration of 190 ps per bunch-crossing [1]. With an initial resolution of 30–40 ps, the new Minimum Ionizing Particle (MIP) Timing Detector (MTD) will measure production time of MIPs [2]. This will improve identification and event reconstruction capabilities of the CMS experiment in the increased pile-up conditions expected during HL-LHC with respect to LHC. The functional building block of MTD's Barrel Timing Layer (BTL) is called the Readout Unit (RU). Topology choices of the RU design dictated a split of the on-detector low voltage regulation unit into two Power Conversion Cards (PCCs) as shown in figure 1. The BTL design utilizes 864 PCCs, each hosting three DC-DC converters.

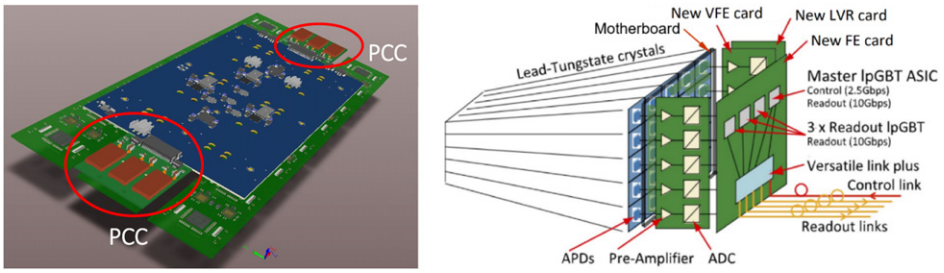

Figure 1. A picture of the 3D design of RU (left) and a schematic sketch of a RT (right).

The barrel Electromagnetic Calorimeter Barrel (EB) will undergo an upgrade of readout electronics to cope with the increased luminosity effects on the resolution of particles' energy

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measurements. The EB consists of 61200 scintillating $PbWO_4$ crystals with double Avalanche Photo Diodes (APDs) glued onto them. The crystals are organized in 5 × 5 entities, called Readout Towers (RTs), where the signals from APDs are conditioned and digitized by five Very Front End (VFE) cards. The stream of digital information pass through a Front-End (FE) card, which in legacy system implements logic for creating trigger primitives and for sending them off-detector as well as the first level of event buffers. After the upgrade the FE cards will abandon this functionality and deliver full resolution single crystal information to the back-end electronics. This change will allow for a precise match of electromagnetic showers to tracks providing a better event isolation compared to the legacy system. Consequently, implemented feature will enable the calorimeter trigger thresholds to remain at a level required for precision study of the Higgs boson [3]. The on-detector powering scheme will be changed from the use of linear regulators to DC-DC converters hosted on 2448 Low Voltage Regulator Cards (LVRs), one per RT, as shown in figure 1. The use of DC-DC converters became a solution common in other CMS sub-detectors [4] as this change improves powering efficiency and allows for thinner cabling thanks to higher input voltage transmission from the off-detector power supplies.

2 Description of the power conversion card for the CMS MTD BTL

The PCC card receives an input voltage of 8 to 12 V and regulates three separate voltages using the on-board step down DC-DC converters. There are two flavours of PCCs. One type regulates two 1.8 V outputs, powering front-end cards of the RU, and one 1.2 V powering digital ASICs hosted on the Concentrator Card (CC). The other type provides 2.5 V to the CC in order to power laser diodes in the transmission modules driving optical links.

The PCCs will operate in a magnetic field of 3.8 T while being cooled with liquid CO_2 circuits at −35 °C. Estimated radiation levels reach a fluence of $1.90 \times 10^{14}\ n_{eq}/cm^2$ and a total dose of 32 kGy at the end of the planned High Luminosity LHC (HL-LHC) programme.

Current RU design allocates the vertical space for the PCC of 7.0 mm and positions the cooling interface below the card. These constraints exclude the use of FEASTMP modules [5] and imply a custom development. The PCC has undergone several prototyping steps, following the changing design requirements of the project, each time introducing improvements to the efficiency, filtering or noise emission. The details of a single converter performance and design choices are discussed in section 4. The evolution of the PCC design is shown in figure 2.

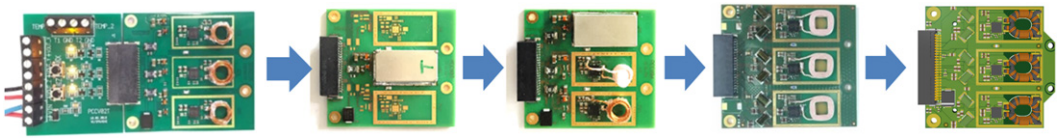

Figure 2. Pictures of the evolution of power conversion cards from the first prototype (left), using hand winded copper solenoids, to the last iteration (right) with production toroids and optimized outline.

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3 Description of the low voltage regulator for the CMS EB

The LVR card operates with an input voltage of 8 to 12 V and outputs five separate voltages using four step down DC-DC converters and one low-dropout linear regulator (LDO). The card delivers two separate 1.2 V supplies to power digital domains of the five VFEs and one FE card, and two 2.5 V supplies for the analogue part of VFEs and the laser diodes in the optical link driving transmission modules hosted by the FE card. Additionally, LVR is equipped with an 80 mA LDO powering remaining digital ASICs of the FE card at 1.5 V.

The LVRs will operate in a magnetic field of 3.8 T while being cooled with demineralized water circuits at +9 °C. The estimated radiation levels reach a fluence of 3.0×10^{14} n_{eq}/cm^2 and a total dose of 10 kGy at the end of the planned HL-LHC programme.

The EB will be partially upgraded with the new readout electronics, keeping the crystals and photo-detectors. The passive interconnections and the mechanical structures will remain unchanged. This results in mechanical constraints of the LVR card being dictated by the legacy system and the necessity of the preservation of its form factor and outline. Three prototype iterations of the card has been produced, shown in figure 3. The first prototype utilized six off the shelf FEASTMP modules [5]. The second had six custom DC-DC converters directly integrated on one printed circuit board (PCB) and implemented solenoidal coils as their main inductors. In the meantime, the forecasted current consumption of the VFE cards decreased, such that it was possible to safely reduce the number of DC-DC converters to four. Also, the power requirement on the LVR changed and for the third version includes a Low Drop-Out (LDO) linear regulator in addition to the four DC-DC converters. In this version the main inductor for the DC-DC block was changed to a toroid, offering smaller inductance loss when shielded and a reduced near field emission with respect to a solenoidal coil of similar parameters. The downside of the change is a 20% higher DC resistance and a more than twice as tall component. Detailed comparison between the two solutions is presented in section 4.

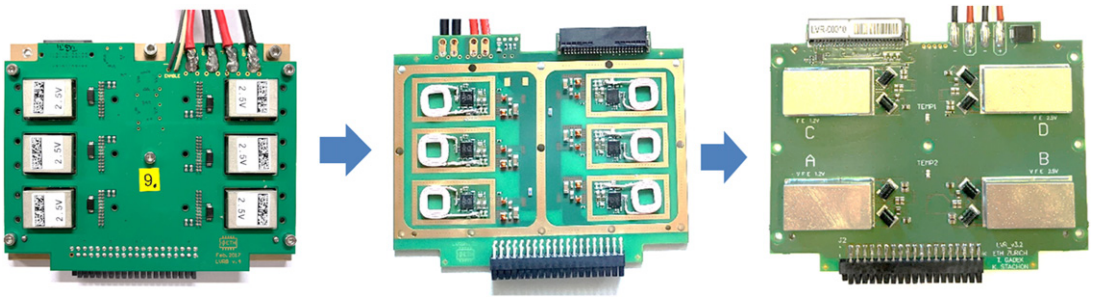

Figure 3. Pictures of the evolution of LVR cards from the first prototype (left), using FEASTMP modules, to the last iteration (right) with production toroids and optimized outline.

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4 Common DC-DC converter design block

Considering the similarities between the BTL PCC and the EB LVR cards a common DC-DC converter block has been designed, which satisfies requirements of both projects summarized in the table 1.

Table 1. Common requirements of the DC-DC conversion block and their source in brackets.

Integrated dose	32 kGy [BTL]
Luminosity	3.0×10^{14} n_{eq}/cm^2 [EB]
Magnetic field	3.8 T [BTL and EB]
Maximum length	45.0 mm [EB]
Maximum width	18.0 mm [EB]
Maximum height including PCB	7.0 mm [BTL]
Minimum operating temperature	−35 °C [BTL]
Maximum operating temperature	+30 °C [EB]
Input voltage	8 to 12 V DC [both]
Output voltages	1.2, 1.8, 2.5 V [BTL]
Max. load	3.4 A at 1.8 V [BTL]

4.1 Design solutions

The PCB build-up selected for the design of the common DC-DC converter block is a 6-layer, 1.6 mm, FR4 stack-up with outer copper layers of 70 µm offering higher electrical conductivity and better shielding performance with respect to standard 35 µm copper. Implemented layout techniques include a hermetic shielding of 300 µm thick tin-coated copper above the switching components, a double-layer via guard-rings and avoidance of through vias in the shielded region reducing the EM field leaks. Mentioned features are presented in figure 4.

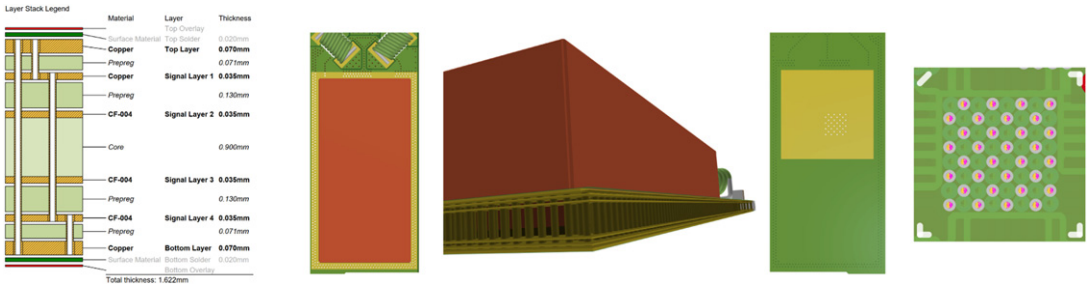

Figure 4. From the left hand side: a representation of the common converter stack-up; a top view of the converter design, showing a soldering pad all around the shield; a side view exposing double layer of via guard rings below the shield; a bottom view of the PCB; a raster of staggered blind and buried vias serving as a thermal contact under the ASIC.

Arrays of staggered blind and buried vias under the ASICs packages were implemented to improve their thermal contact towards the cooling blocks in both projects. The optimization of the

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input inductance to the input voltage decoupling capacitors has lead to switching spikes reduction. This step was necessary for reliable operation of the ASICs, which are vulnerable to input voltages exceeding 14 V. For this reason, a low series inductance capacitor of inverted geometry was placed as close as 400 µm to the input pads of the ASIC.

Initially, in order to achieve a slim design, a 1.6 mm thick solenoid was implemented as the main inductor of the converter. A 0.8 mm thick Litz wire component with eight windings offered a DC resistance below 21 mΩ and an average inductance in air of 667 nH, measured on a lot of 100 pieces with a ±5% precision impedance meter. The solenoid suffered an inductance loss of more than 37% while placed under a 3.5 mm tall shield, resulting in a corresponding 3–4% efficiency loss of the converter. In addition, the topology of the converter assumes the placement of the inductor on the side of the ASIC to reduce the overall height. This necessitated an encapsulation of the coil in order to avoid its movement or vibrations while switching nearly 4 A currents in a 3.8 T static magnetic field. As an alternative to the solenoid a flat toroid was designed to mitigate the above mentioned problems while remaining within the height constraints of the module. This change decreased the emitted magnetic field thus reduced noise emission w.r.t. solenoidal inductor. Moreover, the toroid has been designed with two additional mounting feet, such that together with the leads they create a firm fixation to the PCB via four soldering points.

The 4.4 mm high toroid's design is a 34-winding topology made of 0.6 mm copper wire, winded over a liquid crystal polymer (LCP) bobbin. Measurements on a 20-sample population of a production lot of 650 pieces one supplier show an average inductance of 407 nH at 2 MHz in air, 404 nH when shielded and a DC resistance of 26.5 mΩ. In comparison the samples provided by another supplier have a higher impedance of 446 nH and 24.2 mΩ resistance. Pictures of toroids from both companies, as well as the initially used solenoid and the final design of the common DC-DC converter block are shown in figure 5.

Figure 5. From the left hand side: a picture of a complete design of a DC-DC converter block; a photo of a Litz wire solenoid; a photo of a toroidal inductor supplied by the first supplier; a photo of a toroidal inductor supplied by the second supplier.

In total 75 LVR cards, hosting 300 DC-DC converters have been produced using the toroids provided by the first supplier. The results of typical measurements are discussed in subsection 4.2.

4.2 Performance results

The designed common DC-DC converter block is replicated four times on the LVR card and the resulting design was manufactured. Obtained near field measurements show a 53 dBm attenuation of the emitted field at the switching frequency (2 MHz), a 61 dBm of attenuation of its first

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harmonic and a complete disappearance of the second harmonic below the noise floor. Performance measurements on the lot of 20 cards show a power conversion efficiency of 70 to 85% depending on the regulated voltage, load current and the input voltage. The optimum load point was measured between 1.5 and 2.2 A taking the output filter and the test setup interconnection losses into account. Details of the typical performance measurement are shown in figure 6.

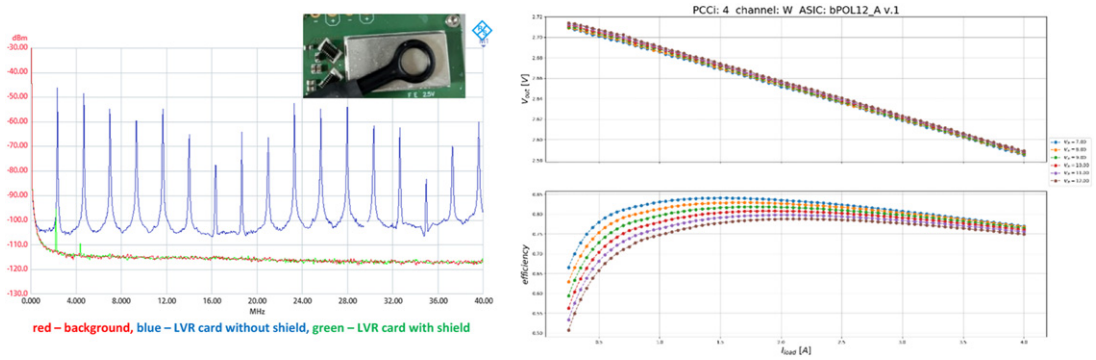

Figure 6. Measured magnetic near field emission on the produced LVR cards (left). Measured efficiency, line and load regulation of the 2.5 V output converter (right).

5 Summary

A DC-DC conversion block design has been proposed as a common solution suitable for both BTL PCC and EB LVR projects in the CMS detector. The production lot of 300 DC-DC converters on 75 LVR cards show excellent EM shielding capability and conversion efficiency meeting expectations. The designs of both cards have matured to a production ready state, offering a compact DC-DC converter design with overall height below 7 mm. The design goal has been achieved using a custom 5 mm tall copper shield and a 4.4 mm tall, LCP core, copper wire toroid.

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