



# Italian-cluster technical solutions for the Quality-Control tests to the pixel-modules of the ATLAS Inner Tracker for High Luminosity LHC

Giuseppe Carratta <sup>1</sup>\*, on behalf of the ATLAS ITk group

*Dipartimento di Fisica e Astronomia "Augusto Righi", Alma Mater Studiorum Università di Bologna, Via Irnerio 46, 40126, Bologna, Italy  
INFN - Sezione di Bologna, Viale Carlo Berti Pichat 6/2, 40127, Bologna, Italy*

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## ABSTRACT

In the era of high-luminosity LHC the instantaneous luminosity will achieve unprecedented levels, leading to the occurrence of up to 200 proton–proton interactions during a typical bunch crossing. In response to the resulting surge in occupancy, bandwidth demand, and radiation damage, the ATLAS Inner Detector is slated for replacement by an all-silicon system known as the Inner Tracker (ITk). The innermost segment of the ITk will be comprised of a pixel detector, featuring an active area spanning approximately 13 square meters. To address evolving requirements related to radiation hardness, power dissipation, and production yield, multiple silicon sensor technologies will be incorporated across the five barrel and end-cap layers.

The ITk detector will be built in different laboratories all around the world. Several institutes are actively involved in the ITk project assembling and testing pre-production modules, that have been constructed to assess their production efficiency. Testing sites perform the so-called quality control (QC) tests. The ITk community defines requirements for QC testing both prototypes and modules, and provides common software tools as well as possible technical solutions. Each laboratory must qualify for the QC activity by demonstrating the chosen solutions are compliant with requirements.

In this contribution the relevance of the QC procedures will be outlined, focusing on the custom structures and items developed by the Italian laboratories to improve the quality of the tests and to satisfy the requirements imposed by the Collaboration.

## 1. Introduction

The instantaneous luminosity of the High-Luminosity LHC will lead to up to 200 proton–proton interactions per bunch crossing. To face this challenging condition, the ATLAS Experiment [1] will upgrade its tracking detector during the Phase-II LHC shutdown. The following data-taking period is expected to start by 2029. The new all-silicon system is known as the Inner Tracker (ITk) [2]. It will include a pixel detector, featuring an active area spanning approximately 13 m<sup>2</sup>, and a strip detector extending over about 165 m<sup>2</sup>. Concentric layers will be accommodated so as to build a Barrel (5 pixel + 4 strip layers) and two Endcaps (several rings each) with extended angular coverage.

## 2. Sensor technology

The pixel detector consists of hybrid modules, which include sensor tiles bump-bonded to either one or four front-end readout chips (quadruplets or quads) mounted on a flexible printed circuit board. Single chips are grouped by three on each module (triplet). Different

modules will be installed on the ITk sub-detectors:

- **3D sensors:** used for the innermost layer, with a pitch size of 50 × 50 μm<sup>2</sup> and 25 × 100 μm<sup>2</sup>.
- **Planar sensors:** used for the outer layers with a pitch size 50 × 50 μm<sup>2</sup> and two different active thickness of 100 μm and 150 μm.

## 3. Italian cluster responsibilities

The Italian Community is responsible for the building of one of the Endcaps of the pixel tracker. The activities are distributed among various institutes:

- **Bologna:** Thermal cycles, full quality assurance, and control tests.
- **Frascati & Lecce:** Integration and loading.
- **Genova:** Assembly and tests of quads and triplets.
- **Milano:** Assembly, coating, and testing of quads and triplets.
- **Trento & Udine:** Testing of triplets (Trento) and quads (Udine).

\* Correspondence to: INFN - Sezione di Bologna, Viale Carlo Berti Pichat 6/2, 40127, Bologna, Italy.  
E-mail address: [carratta@bo.infn.it](mailto:carratta@bo.infn.it).

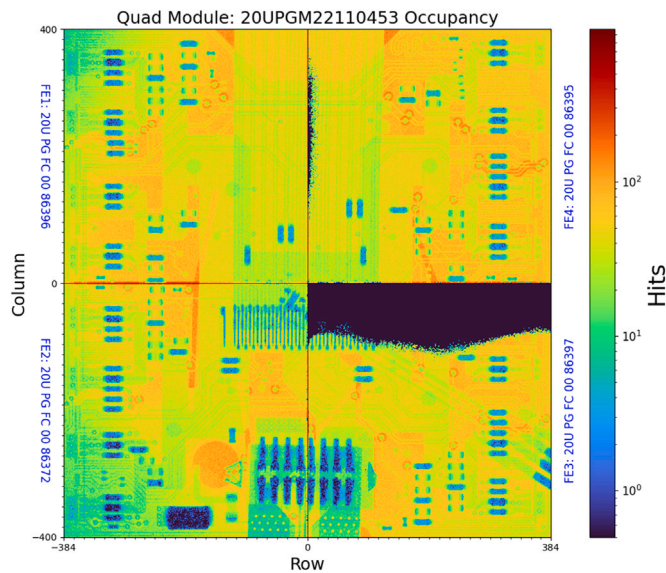


Fig. 1. Occupancy map of an X-ray scan performed on a real quad module. Two disconnected areas (in dark-blue) are visible: one on the left edge of the top-right chip, the other one in the top area of the bottom-right chip.

#### 4. Testing setup and procedures

Modules are tested at room temperature (20 °C) and operational temperatures (-15 °C for quads and -25 °C for triplets). Three types of tests are performed on each module:

- **Electrical Quality Control (QC):** Ensures that readout chips meet electrical specifications.
- **Sensor Quality Control:** Measures leakage current as a function of bias voltage and identifies the breakdown voltage, with typical values depending on sensor type.
- **Functional Tests:** Includes pixel-threshold tuning (1000 or 1500  $e^-$  depending on module type) and bump-bonding quality checks.

#### 5. Thermal cycles

Due to the thermal inertia of the cooling system, power cuts during operation will cause the detector to reach very low temperatures. To ensure the bump bonding will survive such stress, each module will be thermal-cycled (TC) between -45 °C and +40 °C ten times, with an additional cycle between -55 °C and +60 °C. TCs are performed in a dedicated climate chamber and a custom, python-based, Detector Control System (DCS) has been developed to store online parameters on a database and stop operations in case of excess humidity. X-ray scans are performed after TCs to check for possible disconnected bumps and display the functionality of unmasked pixels (Fig. 1).

#### 6. Software & hardware interlock

A DCS system based on WinCC OA and OPC Server is used by all the divisions of the Italian Cluster to monitor and control all devices. Several levels of interlocks have been implemented to protect the

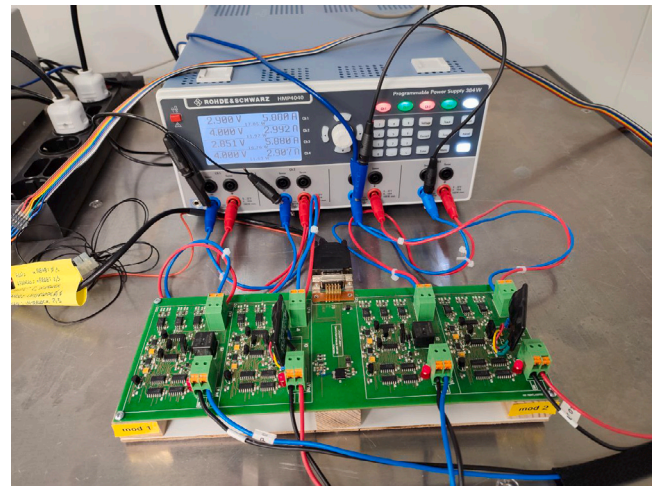


Fig. 2. Picture of the Low Voltage breaker board. Each testing station uses two channels, one for the module and the other one for the peltier. Relays on the board are either standard (first and third sections), to break power to peltiers, or solid state (second and fourth sections) to break power to the FE chips.

module from harmful conditions and potential disruption:

- **Software Interlocks:** managed by the DCS to restore safe conditions without cutting power.
- **Hardware Interlocks:** last resort safety measure. Implemented via a breaker board (Fig. 2) using standard and solid state relays.

The core of this system is an ESP32-DevKitC-VIE connected to various temperature and humidity sensors which sends data and hardware interlock status to the DCS via Wi-Fi.

#### 7. Conclusion

The technical solutions developed by the Italian Cluster for the quality control of the ITk pixel modules are crucial for ensuring good detector performance and reliability under the challenging conditions of HL-LHC. The module pre-production is in an advanced stage, and the community is almost ready to start with the final module production which should be completed in 2027.

#### Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

#### References

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