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First results on monolithic CMOS detector with internal gain

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Abstract: In this paper we report on a set of characterisations carried out on the first monolithic LGAD prototype integrated in a customised 110 nm CMOS process having a depleted active volume thickness of 48 µm. This prototype is formed by a pixel array where each pixel has a total size of 100 µm × 250 µm and includes a high-speed front-end amplifier. After describing the sensor and the electronics architecture, both laboratory and in-beam measurements are reported and described.

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Optical characterisations performed with an IR pulsed laser setup have shown a sensor internal gain of about 2.5. With the same experimental setup, the electronic jitter was found to be between 50 ps and 150 ps, depending on the signal amplitude. Moreover, the analysis of a test beam performed at the Proton Synchrotron (PS) T10 facility of CERN with 10 GeV/c protons and pions indicated that the overall detector time resolution is in the range of 234 ps to 244 ps. Further TCAD investigations, based on the doping profile extracted from $C(V)$ measurements, confirmed the multiplication gain measured on the test devices. Finally, TCAD simulations were used to tune the future doping concentration of the gain layer implant, targeting sensors with a higher avalanche gain. This adjustment is expected to enhance the timing performance of the sensors of the future productions, in order to cope with the high event rate expected in most of the near future high-energy and high-luminosity physics experiments, where the time resolution will be essential to disentangle overlapping events and it will also be crucial for Particle IDentification (PID).

Keywords: Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc); Front-end electronics for detector readout; Solid state detectors; Timing detectors

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1 Introduction

In past few years, CMOS Monolithic Active Pixel Sensors (MAPS) have widely demonstrated to meet the requirements of tracking detectors as a viable alternative to hybrid pixels in high-energy physics experiments [1–3]. Since the spatial density of particle collisions expected in near-future high-energy physics experiments will dramatically increase, silicon detectors are requested to provide also precise time information to perform an accurate reconstruction of tracks [4, 5], particle identification [6] or as beam-induced background mitigation technique (see, for instance, ref. [7]). Several experiments will face this problem, such as the next-generation heavy-ion experiment named ALICE 3 [6], which will be installed at the Large Hadron Collider (LHC) at CERN during the long shutdown 4 (2033–2034).

Recently, significant research efforts have been focused on small pixel size, low noise, and low power consumption to develop MAPS for tracking applications, but their potential in terms of time resolution has not yet been fully exploited. Therefore, to achieve good timing performance a fast charge collection is necessary, and this requires often the use of fully depleted sensors. To this end, Fully Depleted MAPS (FD-MAPS) have been developed in the ARCADIA project [8] where charge induction is due to the drift of carriers. However, this is still not sufficient to reach the optimal timing performance, as it is also needed to carefully optimise the device geometry and the related electric field shape. Sensors with small collection electrodes offer a small capacitance and a higher Signal-to-Noise Ratio (SNR), but the resulting drift paths have different lengths, limiting the time resolution. On the

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other hand, large collection electrodes show a better field uniformity with the drawback of a larger capacitance, and thus a decreased SNR. A promising solution to increase the SNR has been found by implanting a gain layer below the collection electrode, thus providing charge multiplication by impact ionization. In this way, the LGAD (Low Gain Avalanche Diode) technology [9] has been integrated in the present ARCADIA production of FD-MAPS devices produced with a commercial 110 nm CMOS Image Sensor (CIS) process provided by LFoundry.

Contrarily to traditional LGADs, which are produced on sensor-grade wafers and require dedicated readout electronics, monolithic sensors can enable to decrease the production costs and to simplify the complex assembly procedures characterising the hybrid devices.

The innovative concept of this Monolithic CMOS Avalanche Detector PIXelated (MadPix) may find application not only in the detection of charged particles in high energy physics experiments but also in medical particle tomography [10] and tracking in space experiments [11], which would benefit from the low material budget, a fine pixel pitch, and a low power consumption.

In this article, we present the first prototype of a monolithic sensor with internal gain based on a commercial 110 nm CMOS process. In particular, section 2 discusses the design of MadPix, covering the geometry and operation of the device, and the description of the integrated electronics and readout system. In section 3, the laboratory results of the sensor characterisation are compared with the expectations of the performed simulations. In section 4 we show the first test beam measurements and the relative results obtained at the Proton Synchrotron (PS) at CERN. Section 5 investigates the properties of the sensor through a numerical study based on a 2D TCAD framework explaining the MadPix behavior. Finally, the conclusions and the perspectives for this technology are highlighted in section 6.

2 Design

In this section, the description of the sensor layout and the front-end electronics is reported. Furthermore, an overview of the first prototype of monolithic CMOS sensor with internal gain in 110 nm, MadPix, is presented. Finally, the test-board for the chip readout is illustrated.

2.1 Sensor

The sensor concept is based on the fully-depleted MAPS developed within the ARCADIA project, where the add-on of a gain layer implant has been implemented [12]. In particular, MadPix design, together with a set of sensor test structures, were fabricated in the ARCADIA third engineering run.

The devices are processed through the ion implantation technique on the chip frontside (see figure 1). As in standard pixelated MAPS, a shallow n^+ implant works as collection electrode, while the gain layer is obtained through a p^+-type layer implanted just beneath the electrode. Surrounding this n^+ region, and the underlying gain layer, we find the deep-p-wells hosting the front-end electronics (n-wells, NW, for the PMOS and p-wells, PW, for the NMOS). These p-type implants are crucial to achieve a full isolation between neighboring PMOS structures, as well as to prevent competitive charge collection that would take place among the NW and the n^+ electrode. Concerning the substrate, the upper part consists of a thin n-type epitaxial layer followed by a second, slightly less doped, epitaxial layer of the same type. These two regions represent the active volume of the sensor and have a global thickness of about 48 µm. They are grown on a highly doped p^+ silicon wafer, that completes the pn junction of the device and allows to apply a reverse bias on the back contact. The biases

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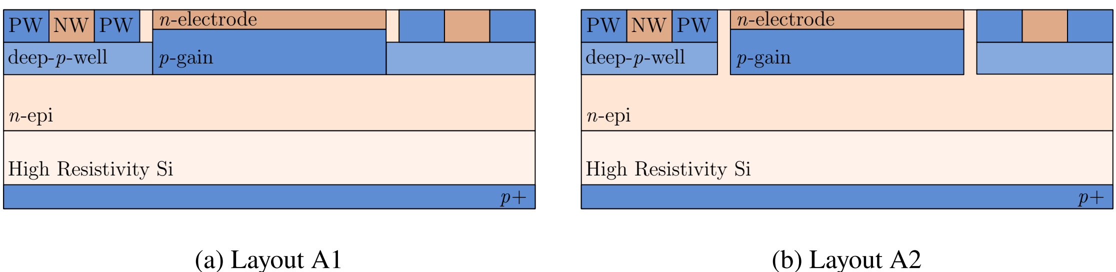
of the front and back contact are referred to the common ground (0 V) applied to the deep-p-wells. Typically, −40 V to −50 V are applied on the backside to have saturation of carriers velocity and operate in full depletion conditions. While, regarding the frontside, applying a certain voltage on the n^+ electrode (in the range between 30 V and 45 V) the electric field in the gain layer becomes high enough to trigger the onset of the charge multiplication through the impact ionization mechanism. The higher the voltage applied to the collection electrode, the higher the gain. For what concerns the guard-rings, they are biased at 8–9 V since this voltage is sufficiently high to contribute, along with the backside bias, to the full-depletion of substrate, but at the same time it is safely low to avoid breakdown phenomena at the edges of the active region.

The ARCADIA project developed also fully depleted sensors with an active thickness of 100 µm and 200 µm starting from high resistivity n-type substrates. However, only the 48 µm thick structures were analysed in this study because simulations and data have shown that thinner sensors lead to better time resolutions [13].



(a) Layout A1 (b) Layout A2

Figure 1. Cross-sectional view of the (a) A1 and (b) A2 termination layouts differing by the distance between the p-gain and the deep-p-well implants.

Two different pixel layouts, differing by the termination at the pixel periphery, have been designed (see figure 1). In the first one, called A1 (figure 1(a)), the deep-p-wells are in contact with the gain layer, determining an increased multiplication volume. With this particular design, also primary charges generated via impact ionization under the p-well are multiplied, after being drifted towards the gain layer and then collected by the frontside electrode. However, these charges reach the n^+ implant with a certain delay with respect to the ones produced within the active area, due to the field curvature experienced at pixel borders. In the second layout, called A2 (figure 1(b)), a small gap is provided between the two implants. This means that some charges produced at border may follow drift lines that go through this gap and reach directly the n^+ electrode without crossing the gain layer. As a result, layout A2 allows the discrimination of signals generated in the region with gain, that are induced by charges whose drift lines are straightly directed to the collection electrode, from the peripheral ones, which are not multiplied.

2.2 Electronics

The electronics of the chip is implemented in a 110 nm node and the amplifier design is based on a cascoded common source architecture, with split bias current and active load (see figure 2). The input transistor (M0) is sized to operate in moderate inversion in order to optimise the figure of merit (FoM) [14]:

$$\mathrm{FoM} = \frac{g_\mathrm{m} * f_\mathrm{t}}{I_\mathrm{d}}. \tag{2.1}$$

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This important parameter describes the behaviour of the transistor and it is defined as: g_m/I_d that is the transconductance efficiency, while f_t is the transit frequency of the transistor. The FoM allows to find the size and the operating region of the transistor that maximize the bandwidth of the system for a fixed power consumption.

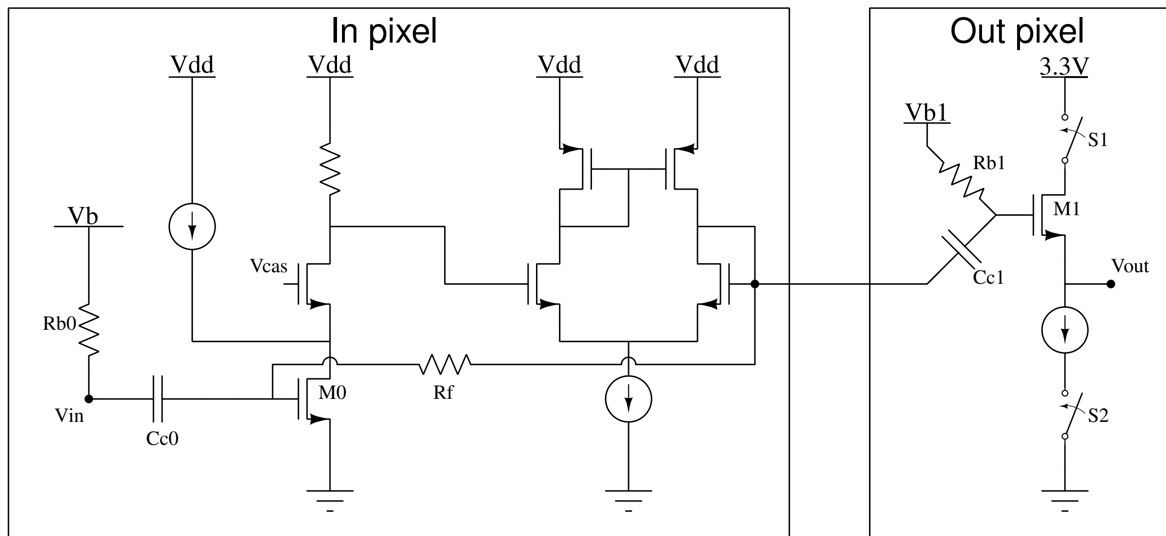

Figure 2. Schematic of the in pixel front-end electronics followed by the output buffer placed outside the matrices.

The first stage is followed by a differential amplifier with unitary gain feedback, needed to separate the amplification from the output load capacitance. During the design phase, a source follower buffer was also considered. However, the voltage drop required to maintain the transistors in saturation mode drastically reduces the dynamic range, which is why the differential configuration was preferred. The output of the buffer is then closed in a resistive feedback loop with the gate of the input transistors to stabilise the gain. The amplifier and the buffer previously described are designed for a power consumption of 200 µW.

The peculiarity of the engineered monolithic device, as described in section 2.1, is the polarisation of the collection electrode to a voltage above 20 V. Therefore, it is crucial to pay special attention to the connection of the sensor to the front-end electronics as the latter operates at a much lower voltage (1.2 V). The proposed solution was to AC couple the pixel and the electronics. The coupling capacitor is an interdigitated multi-finger capacitor implemented above the pixel area. Post-layout simulations were run to set the capacitance value to minimise signal attenuation, dimension, and parasitic to the ground while keeping the inter-finger distances sufficiently large to sustain the required voltage drop.

The front-end is then linked to an output buffer implemented as a source follower enclosed within two transistors working as switches (S1 and S2). An inverter stage is used to turn the buffer on and off with only one signal. Unlike the front-end, which was developed in 1.2 V, the 3.3 V MOSFETs were preferred for this stage since the transistors designed in this power domain have a wider dynamic range and a higher driving capability. Indeed, the transistors of this part are sized to drive a capacitive load higher than 20 pF with a power consumption of 1.6 mW per channel.

As for the collection electrode, having two different power domains implies that a direct connection is not possible. Thus, the output buffer is AC coupled (Cc1) to the front-end electronics and the polarization of the M1 gate is controlled by an external voltage through a 1 MΩ resistor (Rb1).

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2.3 Chip layout

MadPix is $16.4 \times 4.4\,\mathrm{mm}^2$ in size and includes two symmetrical adjacent regions: *top* and *bottom*. Each one has four matrices composed by 64 pixels divided in 8 rows and 8 columns and the layout is shown in figure 3.

Due to size constraint, the chip is designed with only 64 analogue outputs per each region, hence the Vout (figure 2) of four 3.3 V buffers, one for each matrix, shares the same output pad, i.e. the output buffers are multiplexed in groups of four. The pixel size is $100 \times 250\,\mu\mathrm{m}^2$, while the 1.2 V front-end electronics is placed in a $8 \times 250\,\mu\mathrm{m}^2$ deep-*p*-well implemented in the long side dividing two adjacent pixels. Moreover, the 3.3 V source follower buffers are placed outside the matrices and inside the external guard-ring, an important element surrounding each matrix that, polarized to a positive voltage below 10 V, collects the electrons generated in the chip periphery, thus maintaining a low dark current in the pixels. The ratio between the collecting electrode area and the total pixel area is around 67%. For timing measurement this ratio has to be as high as possible in order to minimise the distortion contribution to the time resolution [15]. However, the density rule of the process did not allow the use of larger pixels for this specific run. Still, the technology is compatible with bigger collection electrodes.

The four matrices are labeled A1_*a*, A2_*a*, A1_*b* and A2_*b*. The A1 and A2 labels distinguish the two layout flavour described in section 2. Instead, the letters *a* or *b* represent two different layouts of the coupling capacitor. Indeed, the library element supplied by the foundry is guaranteed to work up to 30 V while the top electrode needs to be polarized up to 50 V to achieve the target value of the gain. Therefore, a full custom capacitor (layout *b*) was designed with a larger gap between the plates to avoid breakdown discharge. Only the A1_*a* and A2_*a* flavors were characterised because no breakdown was observed with the standard capacitor up to 50 V.

As for the readout, two different configurations are possible: a single matrix or a quadruplet pixel readout. The former is active if a matrix *Enable* signal is high, then all the pixels of a matrix are linked to the 64 analogue outputs, and the lines can be read in parallel. The latter enters into operation when all the *Enable* are low; with this configuration only four adjacent pixels of a matrix are selected through a shift-register and read out. The remaining pixels are switched off.

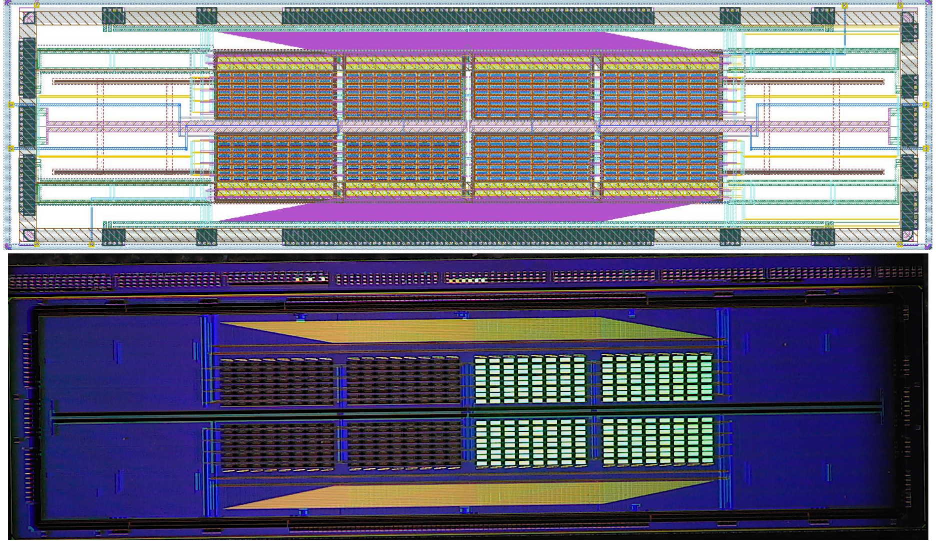

Figure 3. Chip layout on the top and dice micrograph on the bottom.

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2.4 Readout system

A custom PCB TestBoard (TB) has been developed in order to test the MadPix chip (figure 4(b)). Its main purpose is to set all the bias currents and voltages needed by the electronics. In addition, the board provides all the digital signals employed to select the readout mode.

Like the chip, the PCB is divided in two parts: *top* and *bottom*. The top has four analogue buffers each one driving a 50 Ω impedance line, that can be connected to an oscilloscope or to a digitizer via a SMA cable. The bottom part has four LVDS buffers used as discriminators, with the outputs sent to an external FPGA. The same FPGA controls the board via two flat cables (IDC 50 connectors placed on the back of the TB, not visible in the picture).

Depending on the wire bonding configuration, the four analogue buffers and the four discriminators placed on the TB can alternatively read all the pixels or just some of them. Indeed, 16 of the 64 top and bottom outputs pads can be bonded in parallel on the test board in order to read a quadruplet of pixel. The selection of the quadruplet is made by a shift register and all the remaining pixels are switched off thanks to S1 and S2 in figure 2.

The PCB is also responsible for generating the test pulse signal that can be used to easily check the operation properties of the chip. The signal is generated using the circuit displayed in figure 4(a): the BJT is turned on with a signal coming from the FPGA and, as a result, a step in the HV is generated. This perturbation is then propagated through all the chip as the HV line is common to all pixels.

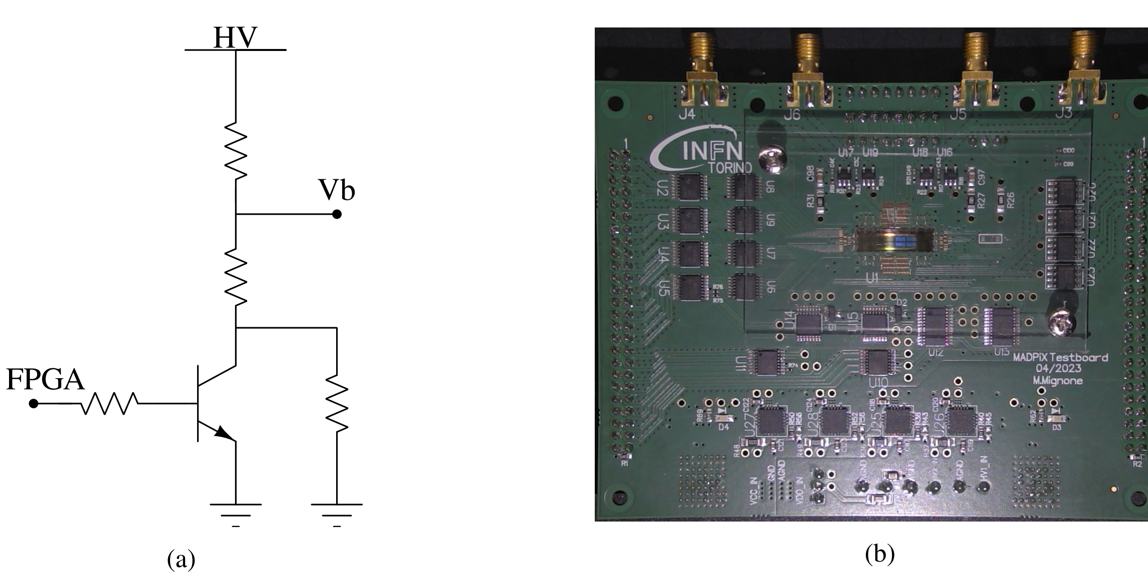

Figure 4. Schematic of the test pulse circuit placed on the test board (a) and picture of the PCB (b). The ASIC is wire bonded to the PCB.

3 Test bench results

This section presents the results obtained from the electrical and optical characterisations.

3.1 Sensor characterisation

Current versus voltage $I(V)$ measurements were performed to characterise the sensor. Specifically, two currents were measured as a function of the scan of the two polarisation voltages with the external

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guard-ring (n-type implant) biased at 9 V (which is high enough to facilitate the full depletion of the sensor, but not too high to avoid an edge breakdown): the backside current I_{back} and the topside current I_{top}. The first one is the current flowing from the p-doped electrode located on the backside of the sensor and it strongly increases due to the punch-through effect which usually arises at backside voltages above 35 V. The I_{top} is the current flowing at the collection electrodes and it significantly grows due to breakdown phenomena when the top electrode is polarised above 45 V. The results are reported in figure 5 where the backside current is normalised per mm^2 while the topside current is given per pixel.

The plot 5(a) illustrates the currents (I_{back} and I_{top}) as a function of the backside voltage V_{back} for the case of 45 V applied on the top collection electrode V_{top}. The I_{top} current shows a decreasing trend with increasing reverse bias, due to the progressive depletion process. Indeed, at low V_{back} the I_{top} is composed mainly by a flow of charge from the collection electrode to the n guard-ring placed around the pixels. Once the substrate is depleted and the conductive path between these two structures is eliminated, we can easily appreciate the thermally generated carriers entering the gain region and causing an increase of the top current. As can be observed, the backside voltage required to fully deplete the substrate is around −28 V, where the I_{top} stops decreasing and reaches a range of stability. Furthermore, the backside current has a significant increase around −12 V due to a floating guard-ring placed outside the padframe, i.e. very close to the silicon border where the chip is diced. This element, if biased, would collect the increase of the border current due to the low resistive path created during the dicing process. This growth has also an impact on the I_{top}, which rises when the backside voltage exceeds −12 V (see figure 5(a)). Indeed, the high I_{back} shifts the start of the full depletion to −28 V. Moreover, it is possible to observe that for reverse bias higher than 33 V, the topside current starts to increase as the multiplication process is increasing too. In figure 5(b) a scan of the V_{top} was made polarizing the V_{top} at −30 V, and the breakdown voltage can be estimated to be around 47 V when the current starts increasing exponentially.

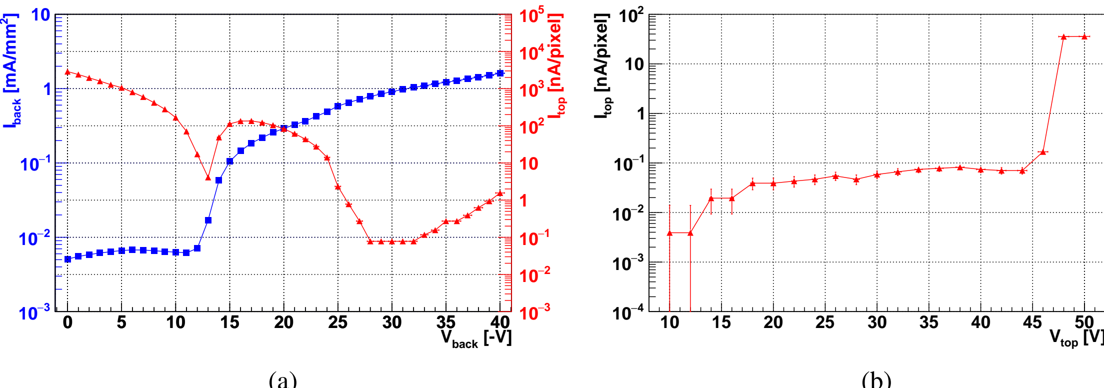

Figure 5. IV plots of the backside (blue squares) and topside (red triangles) currents as a function of the backside (a) and of the topside (b) voltage. The plot (a) is obtained with a given voltage on the collection electrode of 45 V, while plot (b) is reported for −30 V applied to the backside.

3.2 Test pulse characterisation

This section illustrates the characterisation of the pixels of the two top matrices using the test pulse circuitry. The analogue amplitudes in response to an injected test pulse were measured using a Lecroy WaveSurfer 4104HD oscilloscope.

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The results obtained for the two layouts described in section 2.1 (A1_*a* and A2_*a*) are reported in figure 6. A pattern in the pixels response is evident along the matrix due to the layout of the power rails, which are routed from the right side to the left side for both A1 (figure 6(a)) and A2 (figure 6(b)) arrays. Indeed, the signal amplitude decreases with the decrease of the column number due to the voltage drop. A 20% variation on the output amplitude was observed overall in each matrix and no dead pixels were found.

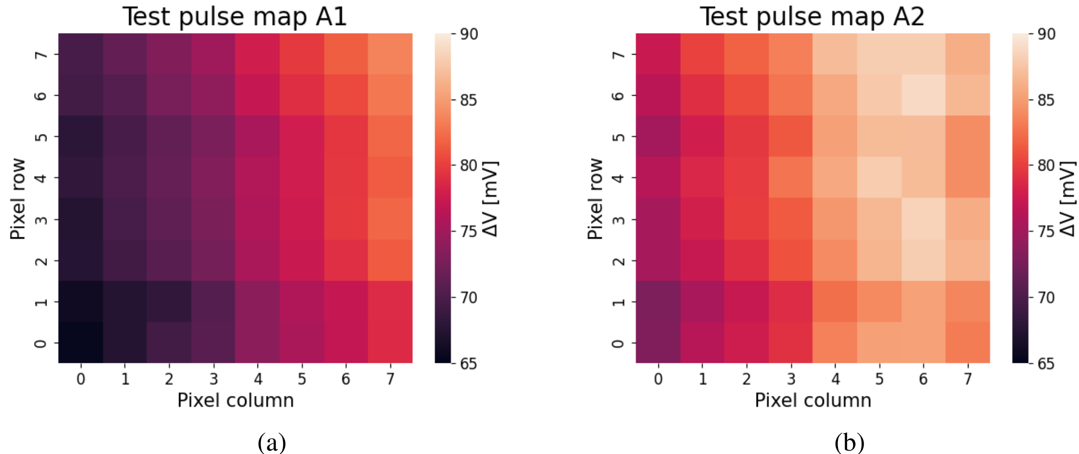

Figure 6. Analogue amplitude measured for each pixel of matrices with flavour A1 (a) and A2 (b).

3.3 Laser measurements

After the electrical characterisation, the behaviour of the chip has been investigated using the Transient Current Technique (TCT), which exploits the signal induced in the sensor by a laser. The TCT setup employed in this study is equipped with micro-metrical *x*-*y* step motors and a fast pulsed (100 ps) IR laser (1060 nm wavelength), that can be focused in a minimum spot with a FWHM ~ 10 µm.

Four analogue outputs of MadPix have been wire-bonded to the 4-channel readout board. The output signals have been acquired with a digital oscilloscope having 1 GHz bandwidth (Tektronix MDO3102).

First, the value of the depletion voltage and the bias dependence of gain have been investigated. The analogue output signal of a pixel in response to a laser pulse of constant intensity has been acquired by varying the top and back voltages. The signal amplitude as a function of both V_{top} and V_{back} is illustrated in figure 7. Specifically, the depletion voltage, i.e. the voltage at which both the substrate and gain layer (since V_{top} is at 45 V) are fully depleted and the drift velocity of the carriers is saturated, corresponds to the point where the amplitude of the signal stops increasing while decreasing the backside voltage, i.e. $V_{\mathrm{back}} < 25$ V (figure 7(a)). On the other hand, from figure 7(b), it can be observed that rising the voltage applied to the frontside collection electrode from 30 V to 45 V, the signal is enhanced by a factor ~ 2.5, proving that the gain gradually grows in this range of V_{top}. The obtained value is in agreement with the one obtained from simulations (section 5).

The same setup has been exploited to provide an estimation of the electronic jitter. The most important contributions to the temporal resolution σ_{t} are shown in equation 3.1:

$$\sigma_{\mathrm{t}}^2 \simeq \sigma_{\mathrm{TimeWalk}}^2 + \sigma_{\mathrm{LandauNoise}}^2 + \sigma_{\mathrm{Distortion}}^2 + \sigma_{\mathrm{Jitter}}^2 + \sigma_{\mathrm{TDC}}^2 \tag{3.1}$$

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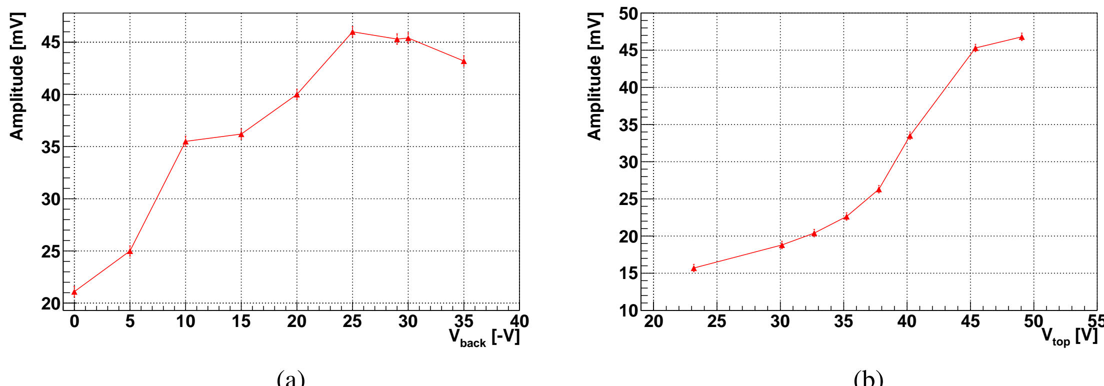

(a) (b)

Figure 7. Analogue output amplitude of one pixel of flavour A1 in response to a laser pulse. The measurements were carried out changing the backside voltage (a) and the collection electrode bias voltage (b). The V_{top} was set at 45 V in (a) while in (b) the V_{back} to -30 V.

Each of these terms takes into account a different physical effect and influences the time resolution. A detailed description can be found in [13].

For the specific case of a laser pulse, the time resolution is not affected by Landau and distortion contributions (eq. 3.1), if the laser spot is smaller than the pixel size. For this measurement, it is important to increase by steps the IR laser intensity performing a laser power scan since the jitter is function of the signal amplitude. In this way, the time walk contribution is negligible as the intensity of the laser is fixed at each step.

Initially, the laser has been set up to release an amount of charge similar to the one induced by one Minimum Ionizing Particle (MIP) and the time resolution was estimated as the standard deviation of the time difference between laser trigger out (TTL) and the analogue output of MadPix at 50% signal amplitude. The measurement results are reported in figure 8 and, in the same plot, the jitter evaluated in post-layout simulations of the electronics is shown. Specifically, the capacitance of the detector used in these simulations was extracted using the CV of the passive structures (figure 14(a)) and the jitter was evaluated using the definition 3.2:

$$\sigma_{\text{jitter}} \propto \frac{N}{\frac{\mathrm{d}V}{\mathrm{d}t}}, \tag{3.2}$$

where the slew rate $\mathrm{d}V/\mathrm{d}t$ is measured at 40–60% of the signal amplitude and the RMS noise is estimated from the integral of the power spectral density obtained through an AC noise analysis.

As expected, by increasing the signal amplitude, raising the output power of the laser, the jitter contribution decreases achieving $\sim$ 50 ps.

4 Test beam measurements

In the following section the test beam setup is described. The charge distributions and the time resolution are then analysed.

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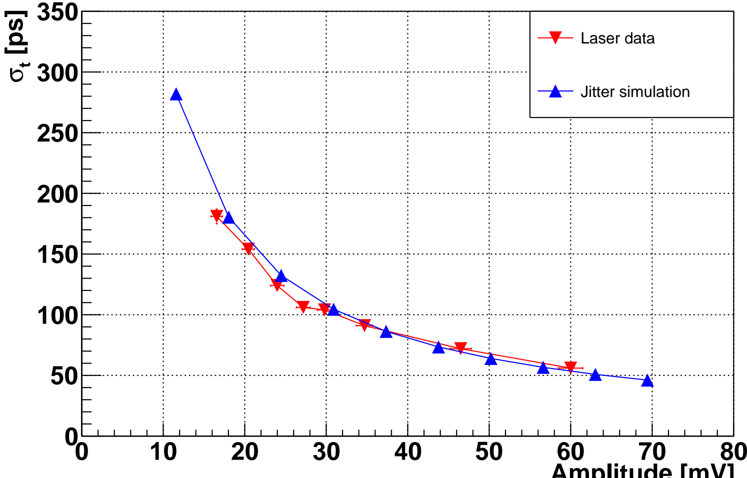

Figure 8. Electronic jitter extracted from circuit simulations (blue) and time resolution from experimental laser measurements (red), acquired with $V_{\text{back}} = -30$ V and $V_{\text{top}} = 40$ V.

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4.1 Setup

The last step to complete the characterisation of MadPix is the measurement of the time resolution. The test beam campaign was carried out at the Proton Synchrotron at CERN (T10 beamline) in October 2023, where a beam composed by a mixture of proton and pions with a momentum of 10 GeV/c was provided. The sensors were arranged on moving stages with micrometric precision and the telescope was placed in a dark box kept at room temperature. The telescope was made of two planes: the Device-Under-Test (DUT) and a 1×1 mm^2 LGAD manufactured by FBK [16] with a thickness of 35 µm, employed as trigger plane. The outputs of three adjacent pixels of MadPix were read out and acquired together with the LGAD output. In particular, a LeCroy WaveRunner 9404M-MS oscilloscope with 20 GS/s sampling rate, 4 GHz of analogue bandwidth and 8-bit vertical resolution was used. Since only four signals could be recorded simultaneously, only the data of three adjacent pixels were acquired and the last channel of the oscilloscope was used for the reference trigger. Specifically, the data acquisition was performed triggering on the coincidence of one pixel of MadPix and the LGAD.

4.2 Collected charge

Owing to the sampling of the full analogue waveform, the collected charge distribution could be extrapolated and the results are reported in figure 9. In these plots, the charge is evaluated as the maximum amplitude of the analogue signal divided by the electronics gain extracted through post-layout simulations and the distributions are fitted with a convolution of a Landau and a Gaussian functions. In figure 9(a) the charge distributions of the A2 structure are plotted for different collection electrode voltages, i.e. 30 V and 45 V. As can be observed, by increasing the voltage, the MPV of the distribution increases by a factor ~ 2.2, which confirms the activation of the gain, in agreement with the laser measurements. Figure 9(b) illustrates the comparison between the structures A1 and A2 at the same bias voltage on the collection electrode, which was set at 45 V. The small difference in the MPVs could be explained by minor fluctuations in the gain of the electronics, while the mismatch in

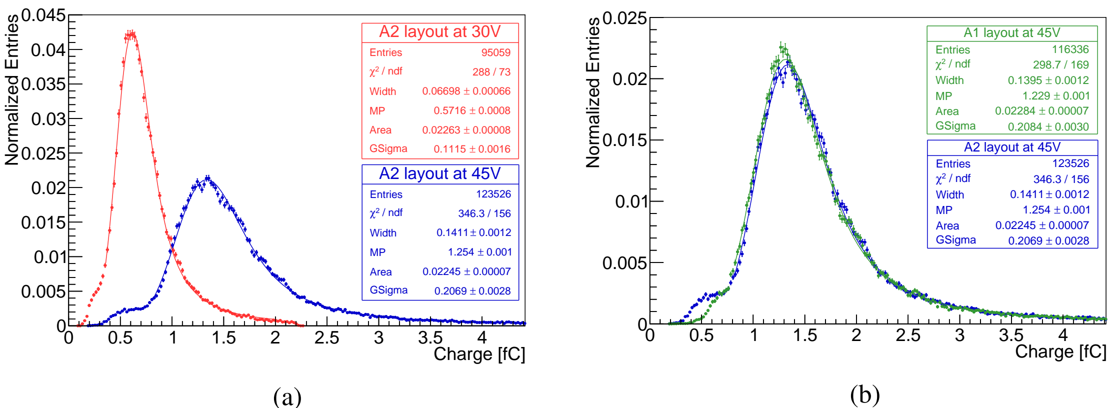

Figure 9. Distribution of the collected charge for two different top bias voltages in the A2 structure: 30 V in red and 45 V in blue (a). Distribution of the charge for the two structures (V_{top} = 45 V): A1 in green and A2 in blue (b). The backside polarization was set at −30 V.

the tails at small charge values can be attributed to the different termination of A1 and A2, since the former provides charge gain through avalanche multiplication also at the edges of the sensor.

4.3 Time resolution

The full waveforms of the LGAD trigger plane and the DUT have been recorded and analysed. The time resolution of Madpix has been evaluated with an offline analysis software and exploiting different analysis methods (fixed threshold and time at a constant fraction). This paper reports the best results obtained using a fixed threshold algorithm with time walk correction.

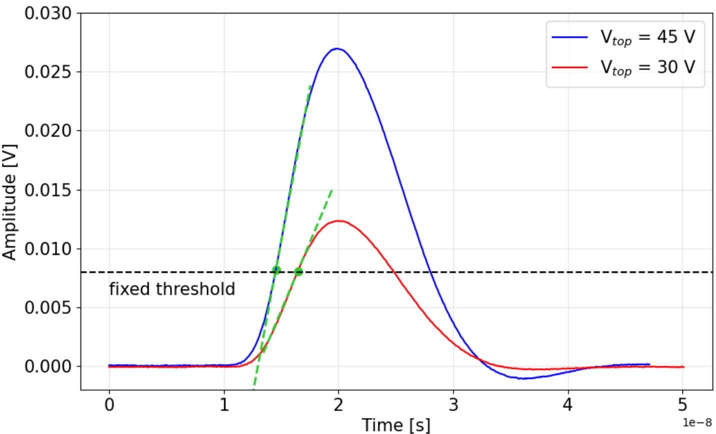

Figure 10. Averaged waveforms of 300 collected events acquired at a top voltage of 45 V and 30 V. A fixed threshold of 8 mV is shown as example, together with the tangent in correspondence of the crossing time. The mean amplitudes of the two waveforms are 27 ± 10 mV and 13 ± 5 mV, where the errors have been evaluated as the standard deviation of the distributions obtained with the aforementioned statistics.

In this method, the Time Of Arrival (TOA) of a particle is set as the time where the signal crosses a given threshold in mV, as depicted in figure 10. The plot shows two averaged waveforms obtained

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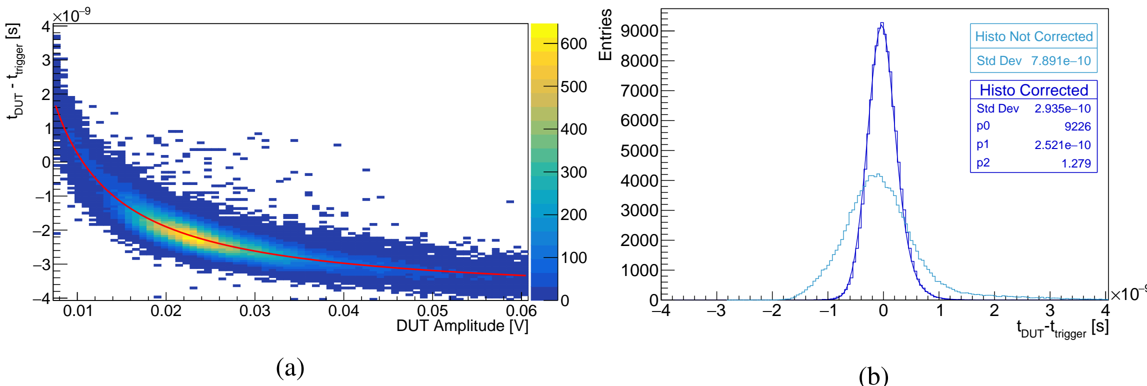
with two different top voltages: 45 V and 30 V. As an example, a constant threshold of 8 mV is applied. The lowest threshold applied has been chosen in order to be at least equal to 5 σ_{noise}.

For what concerns the trigger plane, the TOA has been evaluated using the crossing time at a 30% fraction of the amplitude, obtained with the algorithm described in [17].

However, by employing the fixed threshold method, it has been necessary to correct the time-walk effect. Thus, the time differences between the DUT and the LGAD have been plotted as a function of the signal amplitude of DUT, as shown in figure 11(a). The distribution is then fitted with the following function:

$$t_{\text{DUT}} - t_{\text{trigger}} = a + \frac{b}{(\text{DUT Amplitude})} + \frac{c}{(\text{DUT Amplitude})^2} \tag{4.1}$$

and the correction is applied by subtracting its value from the measured data. Figure 11(b) shows the time difference distribution obtained with a threshold of 5 mV applied on DUT, before and after the time walk correction. Finally, the corrected time difference distributions were used to evaluate the time resolution of the sensor. The distributions are fitted with an asymmetric q-Gaussian function to take into account the tails. Afterwards, the resolution of the reference LGAD is quadratically subtracted from the sigma of the fits.



(a) (b)

Figure 11. Distribution of the time difference between the CMOS sensor and the trigger system as a function of the DUT amplitude. The red line is the fit used to perform the time-walk correction (a). Time difference distributions between the DUT and LGAD before (light blue) and after (dark blue) the time-walk correction (b). The fit used to extract the time resolution is superimposed to the second histogram, where p0 represents the normalization, p1 the sigma, and p2 the right heavy tail of the q-Gaussian.

The time resolution obtained with the fixed threshold method is shown in figure 12 as a function of different applied thresholds. Figure 12(a) clearly illustrates the difference in the response of an A2 test structure when the top voltage is raised from 30 V to 45 V. On average, an improvement around 25% in the timing performance is observed with the $V_{\text{top}} = 45$ V bias voltage. In the $V_{\text{top}} = 30$ V condition, the avalanche gain is strongly reduced and this has an effect on the signal amplitude, that will be lower with respect to the $V_{\text{top}} = 45$ V case. For this reason, the resolution at $V_{\text{top}} = 30$ V starts to increase for thresholds higher than 6 mV, where the slope of the signal starts to decrease, as shown in figure 10 for the case of a 8 mV threshold, translating into a higher jitter contribution. On the other hand, for the $V_{\text{top}} = 45$ V, the slope of the signal is still constant in this region and this translates into a stability in the timing performance.

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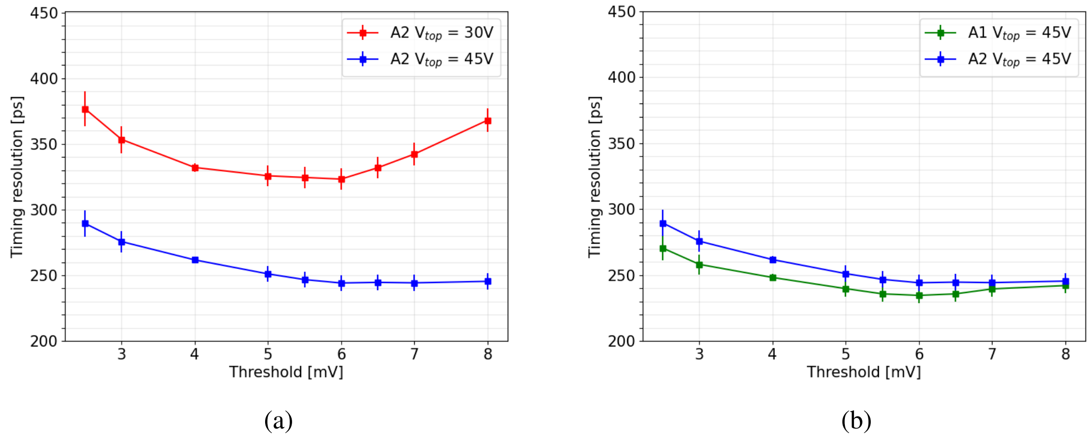
In figure 12(b) the time resolution measured on A1 and A2 structures, both with $V_{\text{top}} = 45$ V, is compared showing a slightly better performance for the A1 version. This effect could be attributed to the different sensor layout and the increased multiplication volume in the A1. The best time resolution extracted with a fixed threshold combined with the time walk correction is 234 ± 6 ps for the A1 and 244 ± 6 ps for the A2, both achieved with a threshold of 6 mV.

The errors at 30 V in figure 12 are evaluated considering the standard deviation of the time resolution of four different pixels of the same structure. Then the relative uncertainty is employed to assign an error to the 45 V results.



(a) (b)

Figure 12. Time resolution as a function of the applied threshold for an A2 structure at two different V_{top} voltages (a). Time resolution at $V_{\text{top}} = 45$ V for the two structures A1 and A2 (b). The V_{back} is set at -30 V.

5 Investigations on gain profiles

To better understand the time resolution performance of MadPix and how it was affected by the gain of the structure, we carried out further experimental and numerical analyses focusing on the gain layer. In figure 13, several measurements of the charge collection dynamics, performed with a near-IR laser setup on test structures with and without (the reference) gain implant, are reported. Dividing the charge obtained in devices with gain by the one acquired by the reference structure, a multiplication factor of about 2.5 was obtained. Moreover, this plot shows that the collected charge is just slightly increasing with the top voltage, thus providing further indication of low gain.

In order to investigate the properties of the gain layer in the ARCADIA third run, we designed a numerical study based on a 2D TCAD (Technology Computer-Aided Design) framework. Since from the capacitance variation as a function of the applied bias voltage it is generally possible to extract useful information about the multiplication implant of an LGAD diode, we proceeded to use the $C(V)$ characteristics as a benchmark tool to validate our gain calculations. The first check that has been performed is the simulation of the lateral capacitance as a function of the top bias in a $250 \times 250\ \mu\text{m}^2$ pitch test-structure with layout A1. Unlike in standard LGADs, we cannot infer any detail about the gain layer through a $C(V)$ obtained with a bias scan performed at the bottom. This occurs because the p^+ region on the chip backside extends throughout the whole device, and the evolution of the space charge region with bias is inadequate for probing the gain layer depletion alone. For such reason, both

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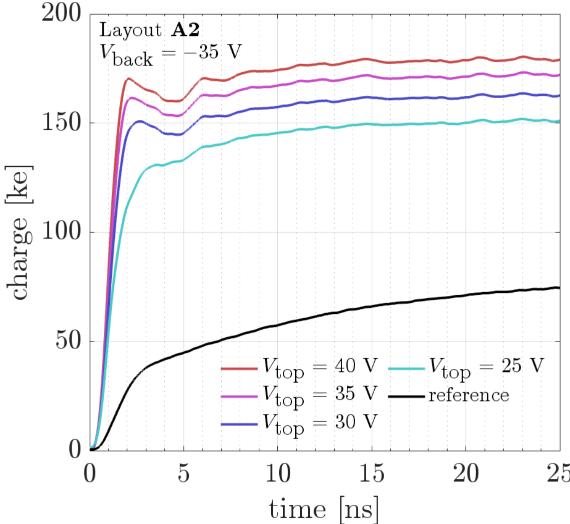

Figure 13. Measured collected charge versus time in a test-structure obtained with a 1060 nm IR pulsed laser. The curves at different top voltage refer to a device with internal gain while the black curve has been acquired with a device without gain (reference sensor).

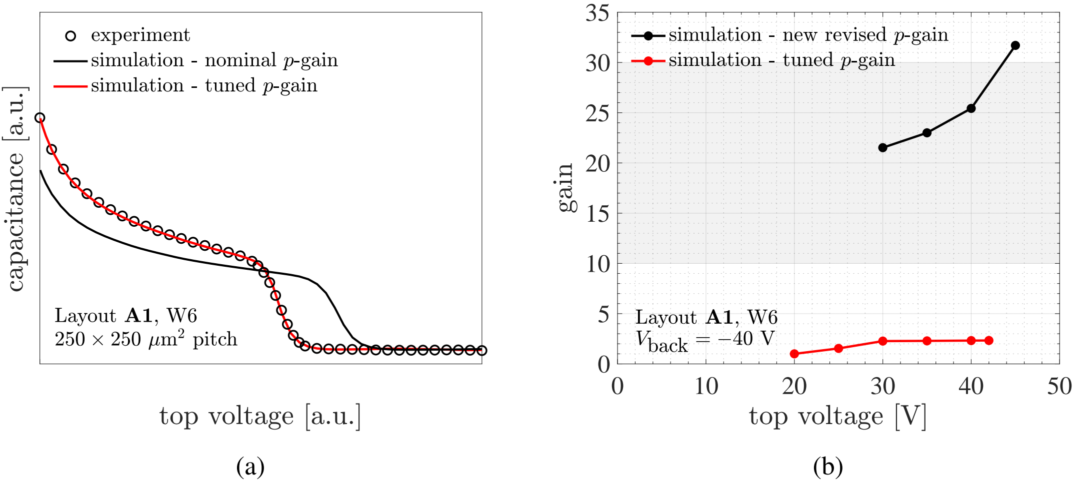

Figure 14. (a) Simulated (lines) and measured (circles) lateral $C(V)$ characteristics of a $250 \times 250\,\mu m^2$ pitch test-structure with gain (units are not explicitly indicated due to non-disclosure reasons). (b) Gain curves simulated using the p-gain implant tuned on the $C(V)$ measurements (red) and with the new profile submitted for the next short-loop run (black).

measured and simulated $C(V)$ are obtained by increasing the potential between the deep-p-well and the n^+ electrode on the top. This is why we refer to our curves as lateral $C(V)$ characteristics. As one may see in figure 14(a), the capacitance simulated with the use of the nominal profile expected for wafer 6 (black-solid line) does not allow to reproduce the experimental $C(V)$. In order to find a good matching between measurements and simulations, the gain implant needs to be considerably shifted towards the chip frontside (red-solid). This fact, since the shallower the gain layer the lower the multiplication factor, could justify the gain 2.5 we measured.

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To prove such hypothesis, we designed a second simulation that calculates the gain G as a function of the top voltage using the tuned implantation profile as input parameter. In the simulations, charge particles incident perpendicularly to the sensor have been considered, and the gain has been calculated as the ratio between the integrated charge with and without the multiplication model activated. In the estimation of avalanche gain we used van Overstraeten - de Man ionization coefficients [18] and the resulting $G(V)$ curve for a device with the same layout of the previous simulations can be observed in figure 14(b). As specified in the plot, the backside bias is set to −40 V, while the top voltage is sweeping in the range 20 V to 45 V. In agreement with the results we have shown in figure 13, the gain simulated using the multiplication layer tuned on the measured $C(V)$ is in the range between 2 and 3, i.e. considerably lower than our expectations ($G \sim 10$–30). This could indicate that an issue has probably occurred during fabrication. As a matter of fact, a cross-check with the process flow revealed that the ion implantation was set at an energy 30% lower than the agreed value. After this check, we submitted a new short-loop run, using the same maskset of the previous production and with a revised version of the p-gain. This new profile should reasonably allow to obtain the initial target $G \sim 10$–30, as the simulation represented by the black curve is showing in figure 14(b).

6 Conclusions

A first monolithic pixel sensor prototype with internal gain in a 110 nm CMOS platform has been produced and characterised in laboratory and in a test beam. The prototype is composed by 8 matrices with 64 pixels each. Every channel has an in pixel front-end followed by an analogue buffer outside the matrix. Two layout of the sensor terminations (A1 and A2) were implemented and tested. In laboratory tests the operation of each pixel was verified and the different bias points of the sensor were analysed. With a voltage of −30 V on the backside, allowing the sensor to be completely depleted, and 45 V applied to the collection electrode we measured a gain of ~ 2.5 with an IR pulsed laser. The optical characterisation also provided an evaluation of the electronic jitter which is ~ 150 ps for a signal amplitude of 20 mV and below 50 ps for signals above 60 mV. The test beam campaign at CERN Proton Synchrotron with protons and pions of 10 GeV/c validated the sensor gain of ~ 2.5 previously estimated with the IR laser and yielded the first estimate of time resolution. The A1 layout showed slightly better performance than the other one and a resolution of 234 ± 6 ps was achieved using an offline analysis with a constant 6 mV threshold and a time-walk correction based on the signal amplitude. Furthermore, TCAD simulations on lateral capacitance of passive structures were employed to explain the measured gain around 2.5. In agreement with the foundry, a short-loop run has been scheduled and the new structures with higher gain are expected to be ready for testing in mid 2024. Further productions will be designed with an improved front-end electronics characterised by a lower jitter to achieve the target of 20 ps total time resolution.

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