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# Digital duty-cycle correction circuit for clock paths in radiation-tolerant high-speed wireline transmitters

**A. Klekotko**,[a,b,*] **M. Baszczyk**,[b] **S. Biereigel**,[b] **S. Kulis**,[b] **F. Martina**,[b] **P. Moreira**,[b] **F. Tavernier**[c] **and J. Prinzie**[a]

[a] *Department Electrical Engineering, KU Leuven, Kleinhoefstraat 4, B-2440 Geel, Belgium*
[b] *European Organization for Nuclear Research (CERN), Espl. des Particules 1, CH-1211 Meyrin, Switzerland*
[c] *ESAT-MICAS, KU Leuven, Kasteelpark Arenberg 10, 3001 Heverlee, Belgium*

*E-mail:* adam.klekotko@cern.ch

Abstract: Ongoing developments in the field of radiation-tolerant high-speed transmitters (HSTs) aim at increasing the data rates above 25 Gb/s while increasing total ionizing dose (TID) tolerance above 1 Grad. The use of half-rate architectures imposes tight constraints on clock signal quality, in particular its duty-cycle. Radiation degradation of transistors in the clock path causes duty cycle distortion (DCD), affecting the output signal quality of the HST. In this paper, a digitally controlled duty-cycle correction circuit suitable for HST is presented. It compensates for process voltage temperature (PVT) variations as well as radiation-induced duty-cycle distortion of the clock.

Keywords: Digital electronic circuits; Radiation-hard electronics; Radiation calculations; Radiation damage to electronic components

*Corresponding author.

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## 1 Introduction

Radiation-tolerant transmitters for high energy physics (HEP) targeting high data rates and ultra-high doses are impaired by signal distortion and various types of jitter. These circuits should be radiation-tolerant and meet all signal requirements within the whole TID range. In half- and quarter-rate serializer topologies, one of the crucial parameters is the even-odd jitter (EOJ), which primarily originates from DCD in the high-speed clock of the serializer. Prior research has shown unequal radiation-induced degradation of PMOS and NMOS devices [1], which may lead to radiation-induced DCD of the critical clock signals.

The demonstrator ASIC for radiation-tolerant transmitter in 28 nm CMOS (DART28) developed in the context of the CERN experimental physics R&D programme [2] operates at 25.6 Gb/s per channel combined with a target radiation tolerance of 1 Grad. Its serializer adopts a half-rate topology requiring a 12.8 GHz clock. The chosen topology implies that any DCD of the high-speed clock will be converted into EOJ at the output. Commercial communications standards such as OIF-CEI-04.0 [3] require an EOJ below 0.035 Unit Interval peak-peak (UIpp) which in this case is 1.36 ps. To meet this specification across all PVT variations and radiation-induced degradation, a digitally controlled duty cycle corrector (DCC) circuit for this clock signal is proposed.

In this paper, the architecture and performance of the designed DCC circuit that provides a tuning range of +/-6% (~4.7 ps) within 0.5% (400 fs) resolution is presented. The methodology used to assess the TID tolerance of the circuit is discussed.

## 2 Duty-cycle correction circuit

The digitally controlled DCC circuit (see figure 1) consists of a duty cycle adjustor (DCA) and a duty cycle measurement (DCM) circuits. The first component changes the duty-cycle of the triplicated pseudo-differential clock received from the phase-locked loop (PLL) and forwards it to the high-speed serializer and DCM. Then the DCM unit provides feedback information to the digital logic. A



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digital control word defines the duty-cycle adjustment applied by the DCA. The DCM results are processed by a digital control circuit having the capability of changing DCA control word as well as DCM measurement settings.

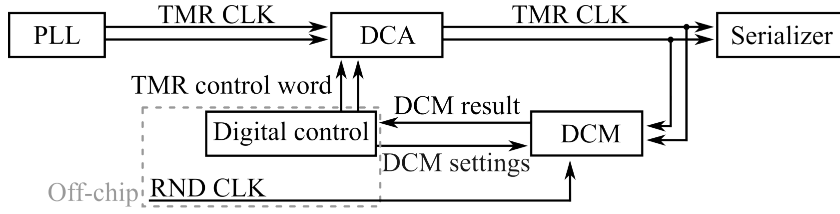


**Figure 1.** Simplified schematic of the DART28 HST duty-cycle correction circuit.

### 2.1 Duty-cycle corrector

The DCA circuit is composed of multiple unit cells, each one is a digitally controlled starved inverter which is shown in figure 2. The minimum driving strength of this cell is fixed by an always-on NMOS ($M_2$) and PMOS ($M_3$) transistors, ensuring that the signal always propagates through the chain. The duty-cycle correction is achieved by controlling the rising and falling edges of the output signal by adjusting the number of enabled PMOS ($M_5$)/NMOS ($M_4$) transistors. The change in signal rise and fall time translates to a difference in the propagation time of the corresponding edge. This influences the duty-cycle of the cell output as follows

$$\Delta \text{DutyCycle} = \frac{\Delta t_{\text{rise}} - \Delta t_{\text{fall}}}{T} * 100\ [\%], \tag{2.1}$$

where T is a period and $\Delta t_{\text{fall}} = t_2 - t_1$ and $\Delta t_{\text{rise}} = t_2' - t_1'$.

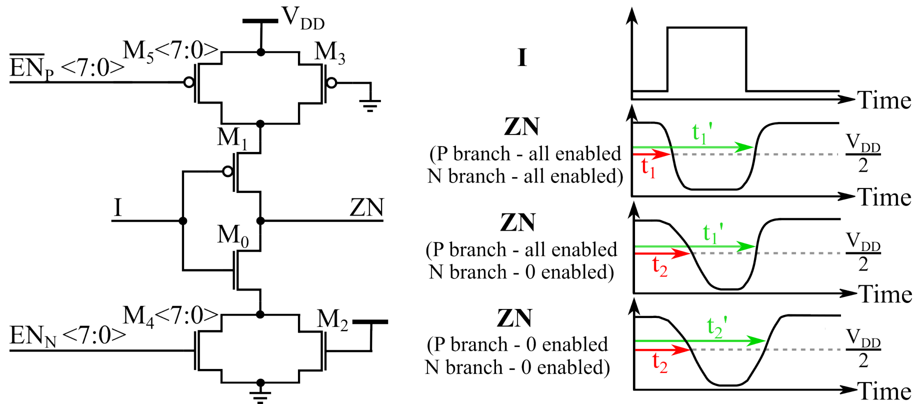


**Figure 2.** The unit cell schematic with example waveforms showing the cell capability of the duty-cycle correction.

The correction capability of single unit cells is relatively small therefore four consecutive variable unit cells (see figure 3) are used to ensure tunability of ± 6% and a resolution below 200 fs. In order to equalize the loading of each unit cell a fifth unit cell with a fixed control setting is used. The total DCA correction capability equals the combined correction of all variable unit cells. In the case of the second and fourth cells, a negative sign is applied because of the odd number of inversions at the cell input.

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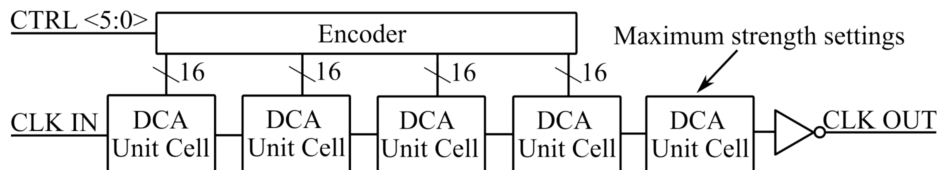


**Figure 3.** Schematic of the DCA.

The encoding scheme accounts for the signal inversion carried out by the unit cell. This means that when multiple transistors need to be set to achieve the desired duty-cycle shift the interleaving of the type of branch being changed is performed (e.g. when the first unit cell NMOS branch is decreased in the following unit cell PMOS branch will be decreased). The enabling procedure is achieved by encoding binary words into thermometric code used by DCA, with the additional benefit of limiting the routing of the control signals over the high-speed clock domain. The resolution requirement was tightened to provide a margin for the error introduced by the measurement of the duty-cycle. Each of the DCA unit cells is fed with a 16-bit control word to control the rising and falling edges. The last unit cell in the chain is used to ensure similar loading for each of the controlled ones therefore its strength is fixed to the maximum. To maintain the phase and match the loading an inverter is placed at the end of the chain.

### 2.2 Duty-cycle measurement

The DCM circuit is shown in figure 4. It measures the duty-cycle of the high-speed clock, providing precise feedback for the digital control circuit to control the DCA.

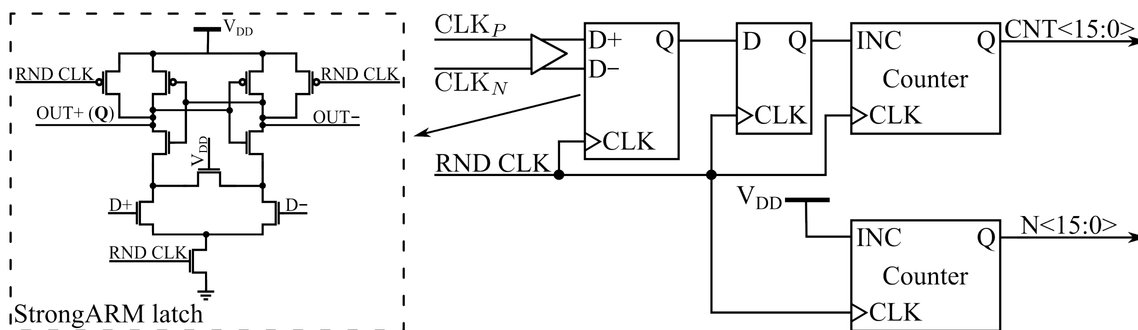


**Figure 4.** Schematic of the DCM circuit utilizing random sampling clock (RND CLK). It consists of sampling flip-flop on the input, re-sampling flip-flop and two counters counting the number of all sampling edges (N), and the number of captured high states (CNT).

The sampling flip-flop captures the high-speed clock signal with a low-speed off-chip sampling clock. The sampling flip-flop is based on a StrongARM latch [4] characterized by very low hysteresis, making the contribution of sampling error negligible. The sampling clock is chosen to minimize its correlation with the measured clock.

Over a given period, the number of acquired ones represents the high-speed clock's duty-cycle and can be formulated as $DC = \frac{CNT}{N}$ if a sufficient number of samples was taken and the high-speed clock signal is sampled with an uncorrelated sampling clock.

To ensure low error levels the circuit adopts the random sampling measurement technique previously presented in [5]. This is a statistical method that does not impose limitations on the



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accuracy of the measurement. This assumption is true when the sampling clock has no correlation with the clock measured in other words its sampling edges are random with respect to the high-speed clock. Then the number of samples to obtain a measurement error at the level of $\alpha$ with confidence level $z_c$ can be described as [5]

$$N = \left(\frac{z_c}{\alpha}\right)^2 P(1 - P), \tag{2.2}$$

where P is the measured duty-cycle. To achieve an error level below 0.5%, with $z_c$ equal to 1.96 for the target range of duty-cycles, the minimum number of samples must be above 38416. This puts a requirement on the counter length which in this case must be at least 16 bits long. If a higher level of confidence or lower error levels are required a higher number of samples can be obtained by repeating measurement several times.

### 2.3 Digital control logic

Digital logic was implemented to change the control words based on the DCM measurement results. The implemented procedure checks if the measured duty-cycle is higher or lower than the target duty-cycle, and depending on this outcome, it decrements the strength of the relevant transistor branches in the DCA by changing the control word. The duty-cycle correction can be performed in five iterations by using the binary search for this process. That algorithm does not go through all possible settings of the DCA, therefore the tunability error is almost 0.5%, still being below the required limit.

## 3 Radiation hardening

The DART28 chip is designed to be radiation tolerant application specific integrated circuit (ASIC) up to 1 Grad TID. This means that the usage of radiation-hardening techniques is necessary for that application.

The high-speed clocks together with the corresponding DCA circuits are triplicated to protect the circuit from errors caused by single event transients (SETs). A triple modular redundancy (TMR)-based mitigation technique [6] is also used in the DCM and DCA encoder logic. Each of these clock signals has its own DCM block, which provides redundant feedback information. To further increase SET robustness, a minimum spacing of 10 µm between TMR copies has been kept, minimizing the likelihood of a SET affecting multiple replica circuits.

Further design constraints were placed to reduce the TID-induced degradation of the circuit. As earlier works showed significant degradation of the drive current of narrow PMOS devices when exposed to large TID [7, 8], the width of all used devices was constrained to be at least 3 times larger than the width of minimum size transistor.

### 3.1 TID simulations

To validate the circuit TID immunity, simulations with transistor radiation models were performed. The used model extends the one described in [9] by TID-induced mobility degradation. The mobility change due to TID was modeled based on measurements of the particular MOS devices used in the design. In simulations, this degradation was incorporated by modifying the corresponding BSIM6 model parameters [10].



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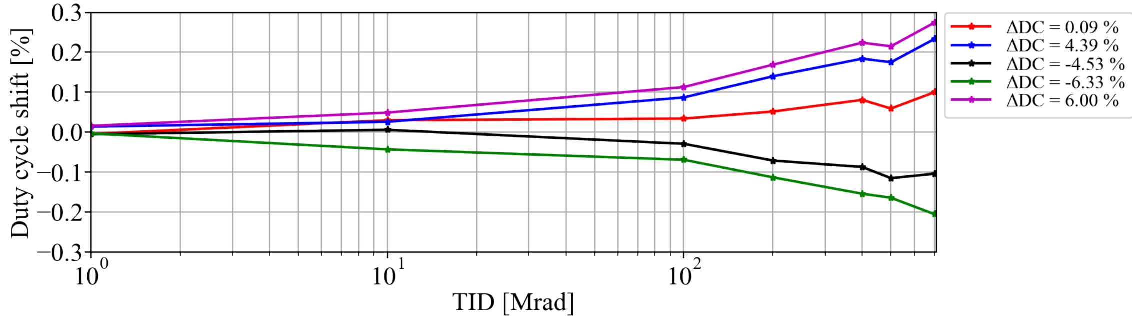


**Figure 5.** TID-induced evolution of the DCA for selected settings including tuning range extremes. The labels show the duty-cycle change performed by DCA for the pre-radiation state.

The DCA was simulated at various settings within the target tuning range. These simulations showed that the radiation-induced degradation is negligible (see figure 5). Even for tuning range extremes at ultra-high doses, the TID-induced duty-cycle shift remains below 0.3%. This indicates that the design itself is radiation-resistant and no compensation of the DCC settings during the lifetime is expected.

## 4 Measurements

The designed DCC circuit was integrated into the DART28 chip. The chip was wire-bonded to the PCB. Communication with ASIC was performed through the $I^2C$ interface. A frequency generator was used to generate an uncorrelated clock with frequency ~100 Mhz for the DCM tests. For each measurement point, the maximum number of samples of DCM have been collected to provide the highest possible accuracy.

The results are shown in the figure 6 together with simulation results. The results show the tuning range achievable for an input duty-cycle of 50% for various PVT corners. Looking into the details of the figure 6(a) a small positive offset (~ 0.5%) is observed, which may be caused by the duty-cycle value offset of the output clock at the output of the PLL. Figure 6(b) shows that the step size in the whole tunability range shows similar results as the simulated for the slow PVT corner.

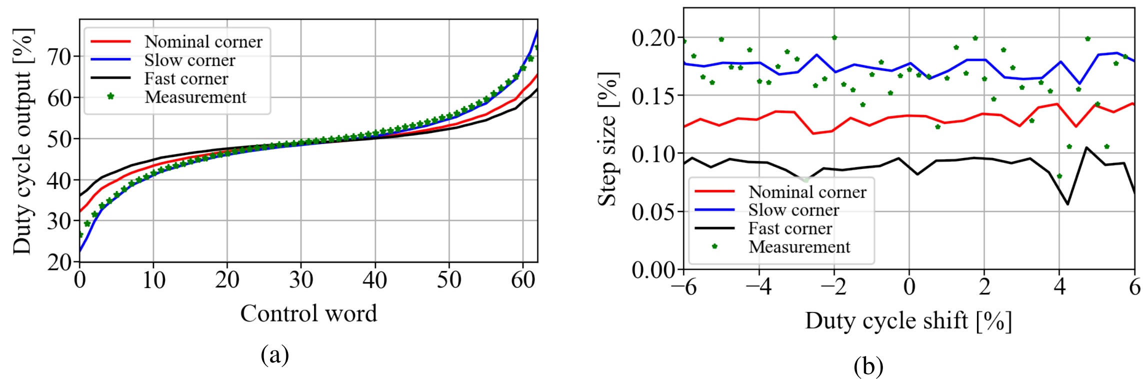


**Figure 6.** The DCA chain characteristics of the (a) duty-cycle tunability as a function of a control word and (b) resolution as a function of applied duty-cycle shift.

TID and single event effect (SEE) campaigns are planned to confirm the targeted level of radiation tolerance of the circuit.



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## 5 Conclusions

A radiation-tolerant DCC circuit was presented in this paper. The simulations and preliminary measurements have demonstrated that the circuit satisfies the requirements, providing a tuning range of ± 6% at 12.8 GHz with a resolution of 400 fs being able to counteract duty-cycle distortion caused by e.g. PVT variations. These results have been validated through measurements. The TID-immunity was accessed in simulations showing that radiation-induced duty-cycle shift within the whole range of tunability does not exceed the value of 0.3% indicating promising radiation immunity, which will be validated in a future X-ray experiment.

The presented DCC circuit is well-suited for use in radiation-tolerant high-speed transmitters. It extends the radiation tolerance of the DART28 transmitter by expanding the allowable margin for radiation-induced degradation of the clock path.

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