Phase-II Upgrade of the ATLAS L1 Central Trigger

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Abstract. The ATLAS trigger system will be upgraded for the Phase-II period of LHC operation, with data-taking expected in 2029. This system will include a Level-0 trigger based on custom electronics and firmware, and a high-level software trigger running on off-the-shelf hardware. The upgraded L0 trigger system uses information from the calorimeters and the muon trigger detectors. The system will be operating at ten times the current rate, reaching 1MHz readout rate. The MUCTPI receives candidates from muon trigger sectors and calculates multiplicities. Muon multiplicity information is sent to the Central-Trigger-Processor and trigger objects are sent to the L0 Global Trigger Processor. In Phase-II, the CTP will be a newly designed and custom-built electronics system, based on the ATCA standard. It will employ a SoC and optical serial inputs to receive trigger information from the Global Trigger and the MUCTPI system. The control and monitoring software will run directly on the System-on-Chip, while the trigger logic runs on an FPGA. The CTP will operate with double the number of inputs, allowing a set of 1024 trigger items based on 1024 usable single-bit inputs, which, in turn, requires updates in the trigger logic implementation, as well as the software for compiling the trigger conditions into FPGA configuration files. New features will also be introduced, such as delayed triggers. We will present the design and status of the Phase-II L0CT system and its new features, including a view of the pilot Phase-I upgrade, which paves the way for the upcoming upgrades.

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1 HL-LHC and the ATLAS upgrades

The High Luminosity upgrade of the LHC (HL-LHC) comes with about an order of magnitude more instantaneous luminosity delivered to the LHC experiments, which comes with an increase of pileup collisions reaching 200. This increase creates the challenge to be able to capture more interesting physics events, as well as to do it more efficiently in an environment of hundreds of tracks per event. The planned trigger rates at the first-level trigger will increase from 100 kHz to 1 MHz, while the final event selection from 1 kHz to 10 kHz. The ATLAS experiment [1] will upgrade multiple components in the coming years to prepare for the increased luminosity provided from the HL-LHC [2]. This includes upgrades of the Trigger and Data Acquisition (TDAQ) system of ATLAS [3]. The key features of the TDAQ upgrade are:

- Increased operating rates: higher trigger rates (factor of 10) than the ones expected in Run 3 are needed to achieve the targets of the ATLAS physics program in Run 4.
- Full detector granularity: taking advantage of increased granularity will improve efficiency for muon-based triggers.
- Extended coverage: similarly, taking advantage of extended coverage of the solid angle around the collision point will help improve the physics efficiency. This is mainly achieved with detector upgrades, which augment the trigger input information.
- Improved muon trigger efficiency, thanks to the upgraded electronics of the Muon Drift Chambers (MDT), allowing better p_T resolution for the L0 trigger.
- Similar overall architecture, following the current system's connectivity scheme.
- Modern hardware technologies: utilization of the modern Advanced Telecommunications Computing Architecture (ATCA) for the new electronics, as well as incorporating System-on-Chip (SoC) modules.

2 ATLAS Level-1 Central Trigger (L1CT)

In this section we describe the L1CT components' functionality and how they come together within the TDAQ context. Details about the upgrades of Phase-I and II are given in following sections.

Central Trigger Processor (CTP): The CTP receives trigger inputs from the detector and issues the first -level "accept" signal when the inputs match any of the pre-defined interesting combinations. The accept signal is forwarded to the front-end electronics to allow the full event data to be sent to the High-Level-Trigger (HLT) and then through the data acquisition (DAQ) path towards permanent storage.

MUon-CTP-Interface (MUCTPI): The MUCTPI receives candidates from muon detectors, sorts them by p_T and arranges them based on defined thresholds. The multiplicity of each threshold is sent to the CTP to be taken into account for the required trigger conditions, as well as to the L1 topological trigger module (L1Topo) to allow complex combinatorics. The MUCTPI also applies overlap removal between the inputs, wherever they correspond to overlapping detectors.

TTC distribution: A distributed component (currently: ALTI) in charge of the fan-out of the Timing, Trigger and Control (TTC) signals to the front-end electronics, as well as the back-propagation of the "busy" signal from the detectors to the CTP. It also provides some trigger logic functionalities for sub-systems tests in standalone. While not shown in Fig.1, it connects the CTP with the detector readout systems (FELIX, for Phase-II).

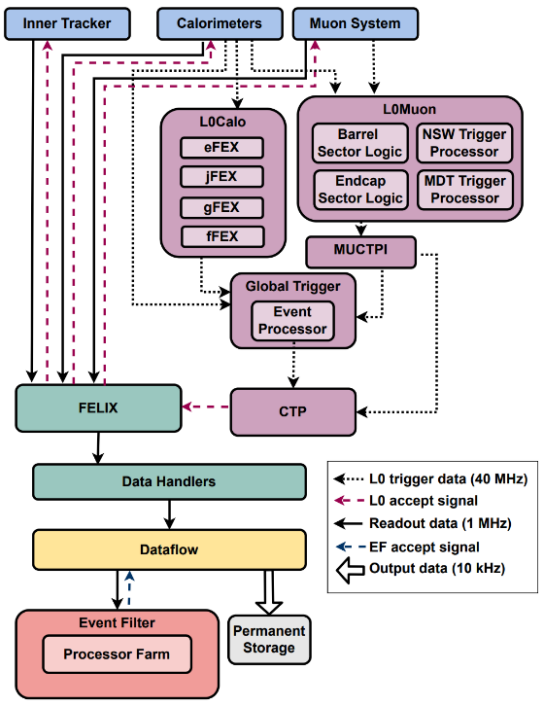

Figure 1: ATLAS TDAQ scheme showing flow of readout and trigger data in the Phase-II upgrade.

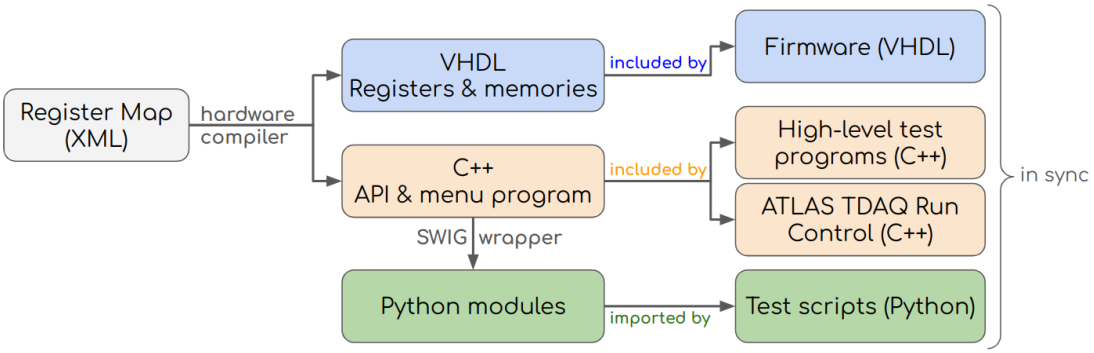

Figure 2: L1CT Phase-I development workflow showing common XML files being the basis for separate & synchronised developments in firmware and software.

3 ATLAS Level-1 Central Trigger - Phase-I upgrade

L1CT Phase-I upgrades include the CTP+ modules (added optical inputs and re-configurable trigger logic) and the MUCTPI (was a set of VME boards before) [5], while a new TTC distribution board was also employed. In this paper, we only mention a few details of the MUCTPI Phase-I upgrade, since it serves as a pilot upgrade for Phase-II, which is the main topic.

The MUCTPI in Phase-I is implemented as a single ATCA blade, employing a SoC which runs Linux. Initially, a 32-bit architecture was used, but the production version uses the 64-bit Zynq Ultrascale+ MPSoC, running AlmaLinux OS. The trigger logic is implemented in three FPGAs (2x Virtex Ultrascale+ and one Kintex Ultrascale). High-speed optical connections are used for most inputs and outputs.

In addition to the hardware, the software development workflow used for the MUCTPI proved efficient and will be kept in Phase-II. The workflow starts with hardware definition files, which include the firmware block parameters and status/control register mapping. These files are then used in the firmware compilation, but also as input to a "hardware compiler" software which generates low-level C++ classes. The generated classes are used as an interface in the development of test scripts and high-level run control applications. The same generated classes are made available for use in python test scripts through SWIG (C++ to python wrapper), which facilitates early operation and testing, when execution speed, type safety and compatibility with TDAQ software are not required. The software workflow is also shown on Fig. 2. The software was initially cross-compiled, but we have moved to a native central method, which can serve as an example for other ATLAS groups. It's notable that the MUCTPI is the only system currently running the run-control software directly on the SoC. Last but not least, Gitlab CI/CD tools are used to increase efficiency in software deployment.

The same concept of a SoC mounted on an ATCA blade will be widely used in Phase-II by L1CT and other groups. With the successful operation so far in LHC Run 3, the Phase-I experience [4] provides a solid base for Phase-II developments, described in the next section.

4 ATLAS Level-0 Central Trigger - Phase-II upgrade

In the ATLAS Phase-II upgrade, the first-level trigger is named Level-0. Thus, the central system is called Level-0 Central Trigger (L0CT).

4.1 Local Trigger Interface (LTI)

As its predecessor (ALTI), the LTI board's purpose is to distribute the Timing Trigger and Control (TTC) signals, which are formed at the CTP and reach the front-end detector electronics. Similar to the Phase-I MUCTPI, it is also a single ATCA blade with a SoC and high-speed optical connections. The board offers a wide range of functionalities:

- Per-bunch & rate monitoring for the TTC signals.
- Playback & snapshot memories, useful for debugging and particular tests.
- *miniCTP*: this is a subset of CTP functionalities, allowing sub-systems to run in standalone f.
- Resource partitioning, allowing flexibility in standalone operations.

Another important new feature is the protocol used in the optical link between LTI and its interfaces (CTP, readout), which is meant to have jitter of less than 15 ps and phase stability better than 30 ps (based on components of [6]). This will allow the ATLAS detector to reach the timing resolution necessary for efficient tracking in the high-background HL-LHC environment.

The board (see Fig. 3) prototype is in production during 2024 and a few boards will be made available to the detector groups soon after initial testing.

4.2 Central Trigger Processor (CTP)

The Phase-II CTP, following the MUCTPI example, will change from a full 9U VME crate into a single ATCA blade, with a SoC for control and monitoring. The new system will primarily use optical inputs, keeping the option for a few electrical trigger inputs. Features include:

- Trigger logic with 1024 bits of input.
- Delayed triggers.
- Configurable prescaling per trigger combination.
- Programmable preventive dead-time.
- LHC bunch pattern matching.
- Per-bunch & rate monitoring at various stages of the trigger logic.
- Resource partitioning.
- Calibration request processing.
- Event readout at 1 MHz.

See also Fig. 4 for a schematic of the CTP interfaces and the order of trigger logic steps.

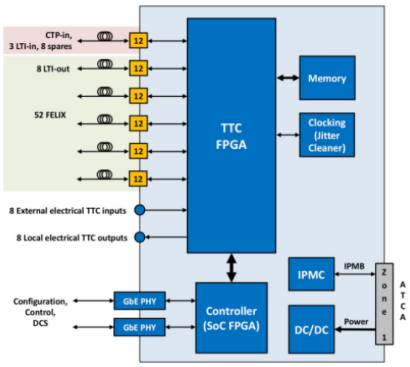

Figure 3: Schematic of the LTI board showing the optical input/output connections, as well as a high-level view of the on-board components.

4.3 From physics requirements to trigger logic

The physics program of ATLAS is translated into a collection of trigger requirements. Each LHC bunch crossing is checked against these requirements with the first-level trigger. These requirements are assembled in a human-readable *Trigger Menu* file. This file is translated into FPGA configuration files using the Trigger Menu Compiler (TMC). Due to the differences in hardware and implementation of trigger inputs, there is the need for a new TMC (TMC2), which will take the L1 Trigger Menu as input and produce the CTP configuration files for Phase-II.

The main steps in the TMC2 software are:

1. Parse the menu, interpreting trigger requirements as logical variables and expressions.
2. Simplify and transform the logical expressions into a form suitable for the firmware implementation logic.
3. Identify connected components ("cliques") among all logical expressions.
4. Assign cliques to the LUTs in the firmware trigger logic.
5. Produce configuration files in the hardware-specific format.

TMC2 is implemented in python, utilizing existing libraries[1]. *Sympy* is used to handle logical expressions. *networkx* is used to identify connected components in groups of trigger inputs. *Google OR-tools* includes a knapsack solver, which is used for optimal assignment of trigger input groups to existing LUTs with restricted number of inputs.

[1] sympy.org, networkx.org, developers.google.com/optimization

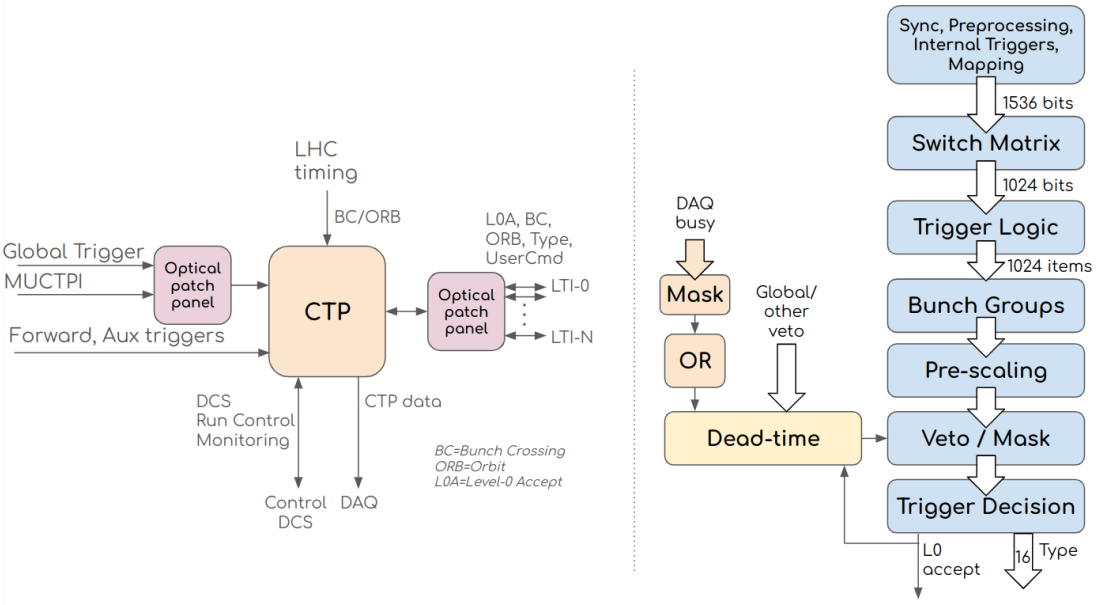

Figure 4: **Left**: CTP interfaces (clockwise: common LHC clock and Orbit signal, TTC output to sub-system LTI boards, event readout, Detector Control System (DCS), detector trigger inputs. **Right**: CTP trigger logic order (input re-arrangement, L1-accept signal formation, bunch group filtering, pseudo-random prescaling, configurable masking and dead-time application, and finally the trigger decision to be sent to the sub-detectors).

5 Conclusions

Demanding conditions of the HL-LHC require major upgrades for the ATLAS experiment in the next long shutdown (2026-2028). ATLAS TDAQ and L1CT groups are preparing for the Phase-II upgrades while ensuring smooth operation of the current system. The L1CT Phase-I work serves as pilot for significant upgrades of key components upcoming in Phase-II, using modern techniques in hardware and software.

References

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