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Updates on Impact Ionisation Triggering of Thyristors

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Abstract: High voltage (HV) generators are used in multiple industrial and scientific facilities. Recent publications have demonstrated that triggering industrial thyristors (relatively slow switching devices) in overvoltage mode, also called impact ionization mode, significantly enhances their dU/dt and dI/dt characteristics. This novel triggering methodology necessitates the application of substantial overvoltage between the thyristor's anode and cathode, delivered with a swift slew rate exceeding 1 kV/ns. The adoption of compact pulse generators constructed from commercially available off-the-shelf components (COTS) opens up avenues for deploying this technology across various domains, including the implementation of high-speed kicker generators in particle accelerators. In our methodology, we employed commercially available high-voltage SiC MOSFETs along with a custom-designed fast gate driver. This driver was conceptualized based on the recent development of gate boosting techniques, featuring a driving voltage exceeding 600 V. The gate driver for these MOSFETs comprises three key components: a level-shifter with NMOS and PMOS transistors, a compact Marx generator with two avalanche transistors, and a GaN HEMT in a high input and low output impedance configuration. The proposed gate-boosting driver achieves a slew rate exceeding 1 kV/ns for the driving pulse. Furthermore, we demonstrate that with this driver, a 1.7 kV rated SiC MOSFET can produce an output pulse of 1.45 kV and a maximum slew rate of ≈2.5 kV/ns. This gate-boosting driver aims to minimize commutation times, achieves a slew rate of over 1 kV/ns, and handle higher loads, making it ideal for impact ionization triggering of industrial thyristors.

Keywords: pulse generator; driver; gate boosting; avalanche; overvoltage triggering; SiC MOSFET; GaN HEMT

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1. Introduction

Particle accelerator facilities often rely on pulse generators capable of delivering high voltage (>20 kV) and current levels (>10 kA) to ensure the efficient transfer of particle beams. At CERN, the sequence of accelerators acts like a relay system, each stage boosting the energy of the particles before handing them off to the next accelerator in the chain. Consequently, pulsed magnets in the transfer lines require fast (in the range of <100 ns for the fastest magnets) and precisely controlled magnetic fields [1]. Achieving such speed and precision necessitates the use of fast pulse generators.

Pulse power systems employed at CERN frequently utilize pulse forming lines (PFLs) and pulse forming networks (PFNs) to energize kicker magnets [2]. These configurations typically feature at least one high-voltage closing switch, which may consist of a spark gap, IGBT modules, thyratrons or thyristors [3]. Thyratrons, in particular, provide precise control over switching characteristics, fast switching times, and high reliability. This makes them suitable for high-current and high-voltage applications. However, their inherent drawbacks such as complex triggering and biasing electronics, high cost, rarity, and limited market presence [4], have prompted the exploration of alternative, more reliable, and cost-effective replacement systems based on different technologies.

An alternative approach to delivering high-voltage nanosecond pulses is detailed in [5]. This method centers on the utilization of Insulated-Gate Bipolar Transistors (IGBTs) within a solid-state microsecond pulse charger design. These IGBTs switch the primary capacitor bank to a pulse transformer, facilitating the generation of high-voltage microsecond pulses. These pulses charge the pulse-forming line (PFL), which subsequently discharges through a spark gap to produce the final nanosecond pulses. Employing IGBTs in a parallel configuration in the pulse charger enhances their capacity to handle the high power required for rapid and repeated pulse generation. However, the implementation of such a solution would result in excessive bulkiness, rendering it impractical for applications requiring tens of kilovolts and tens of kiloamperes. Additionally, the requirement for a microsecond charging phase poses another limitation.

A different approach is the inductive adder as presented in [6]. An inductive adder is a solid-state modulator that generates high-voltage pulses through a series of transformers, each equipped with a 1:1 turn ratio. Key components include semiconductor switches (like IGBTs or MOSFETs) to control pulse timing, capacitors to store energy, diode clamps for voltage spike protection, and gate drive circuits for switch management. Its modular design allows for scalable configurations, facilitating maintenance and adaptation to varying needs. However, like the previous approach, inductive adders tend to be bulky, limiting their use in space-constrained environments. Moreover, the transformers within these adders are prone to magnetic saturation if exceeded in capacity, complicating their design. Additionally, while inductive adders are scalable, each added module increases the overall impedance, complicating impedance matching and requiring further adjustments, especially as system specifications expand.

A Marx generator can also be implemented as presented in [7]. This Marx Generator, based on SiC MOSFETs, is engineered to provide fast switching capabilities, targeting specifications for rapid rise and fall times with high voltage and current outputs. The key advantage of this system lies in its use of off-the-shelf components to achieve lower inductance and faster switching times. The use of such a system introduces significant component stress, which can reduce its reliability and lifespan. Additionally, scaling the Marx Generator to achieve higher voltages by adding more stages can lead to increased complexity, larger physical size, and synchronization challenges between the stages, potentially complicating the system's overall operation.

Solid-state thyristor switches have shown reliable performance in accelerator environments [8]. These devices offer a balance of precise control, moderate switching speed, high reliability, and low conduction losses. They are solid-state devices with long operational lifetimes, available in a wide range of voltage and current ratings. They can handle significantly higher currents compared to other semiconductor devices, making them suitable for applications that require robust power handling capabilities. However, designing a system that effectively uses thyristors involves complex assembly with multiple components like fast thyristors, snubbers, and custom gate drive circuits. Regular industrial devices do not meet the requirements to generate a field rise time of less than 100 ns as mandated by our application.

Recent investigations [9] have demonstrated that thyristors triggered in overvoltage mode, typically called impact ionization (II) mode, offer a new approach to fast triggering (sub-nanosecond scale) for high-power applications. In general, an avalanche is a process that occurs in semiconductors under high electric fields. When carriers gain enough energy from the electric field, they can free electrons in the crystal lattice, creating electron–hole pairs. This process can lead to a rapid increase in the carrier density, resulting in an avalanche effect. When the applied electric field is sufficiently high and rapidly increased, ionization occurs throughout the semiconductor, forming an ionization front [10]. If the ionisation front propagates at a speed higher than the carrier speed, the process is called impact ionization.

This triggering method requires the application of high dU/dt and sufficient overvoltage to the thyristor, resulting in the creation of an ionization wavefront within the

semiconductor structure [11]. This technique enables ultra-fast switching and can even be implemented using commercially available thyristors, rendering them faster and capable of accommodating higher current density compared to similarly sized thyratrons.

To induce impact ionization in four-layered devices, like thyristors, the triggering circuit necessitates a voltage applied across the anode–cathode region exceeding twice the static breakdown voltage, alongside a slew rate surpassing 1 kV/ns ([12,13]). Consequently, the triggering circuit must deliver sufficient current to charge the thyristor's parasitic capacitance with the required dU/dt.

Previous documentation provides in-depth insights into the conditions necessary for inducing impact ionization in thyristors. Researchers in [9] explored the operation of fast, GTO-like thyristors developed by ABB Semiconductors, which were triggered in the impact-ionization wave mode. This innovative triggering method, employing a Semiconductor Opening Switch (SOS) generator, significantly improved the current rise rate and reduced turn-on delays. Subsequently, in a study by [12], researchers investigated the capability of triggering commercial low-frequency thyristors within sub-nanosecond timescales using a fast, sub-nanosecond pulse across the thyristors' main electrodes from a compact solid-state generator. In [13], researchers investigated the parallel switching of high-voltage thyristors triggered in the impact-ionization wave mode, leveraging a Marx generator with a peaking module to achieve the necessary fast voltage rise time. This method effectively handled high current pulses while reducing current imbalance among the devices. Once the feasibility of inducing impact ionization mode in commercial thyristors has been demonstrated, the question arises regarding the selection of the triggering method. In [14], researchers explore the application of a Marx generator using thyristors triggered in shock ionization wave mode. The trigger voltage required for the shock ionization wave mode is generated using an avalanche transistor Marx generator of 60 stages.

Previous studies [15] have explored the usage of components from the fast opening switches family (Drift Step Recovery Diodes—DSRD and Semiconductor Opening Switch—SOS diodes) as triggering generators for impact ionization. However, these components present challenges such as unavailability on the commercial market, bulky designs and relatively long pre-charging phases in the hundreds of nanoseconds range—resulting in a pulse triggering delay of up to more than 500 ns [16]. Both types are categorized as opening switches, operating on the principle of rapidly recovering the blocking capability after the removal of the pre-charged plasma from the component structure (equivalent to reverse recovery in diodes) [17]. This involves the generation and maintenance of plasma prior to its application for triggering functions, a process that demands considerable effort.

The spiral generator, used in the study from [18] to trigger thyristors in impact-ionization wave mode, features a compact design based on the spiral/vector inversion principle. It charges a spiral stripline to a high voltage that is rapidly discharged upon activation, reversing the electric field direction and effectively doubling the output voltage. Although the spiral stripline's design is compact compared to other high-voltage generators, it remains bulkier than solid-state electronics. Scaling this design for different sizes or enhanced performance without losing efficiency or enlarging the footprint poses significant challenges.

Our approach emphasizes utilizing commercial off-the-shelf (COTS) components while maintaining a compact and scalable design. This paper details our efforts to enhance the output voltage, slew rate, and current of the super-boosting driver. These enhancements are pivotal in minimizing the commutation time of SiC MOSFETs and preparing the driver for increased MOS gate loads. Our aim is to empirically showcase the potential benefits of employing COTS components within a compact configuration. This approach is expected to result in reductions in size and weight, enhanced reliability and stability, lowered manufacturing costs, and improved performance.

Building upon our previous development of an ultra-fast gate-boosting driver for HV SiC MOSFETs that achieved a significant reduction in rise times, an output voltage slew rate exceeding 1 kV/ns and an amplitude greater than 1 kV ([19–22]), the current paper

outlines the enhancements made to the previous driver design. These enhancements are aimed at improving the super-boosting driver's output voltage, slew rate, and current.

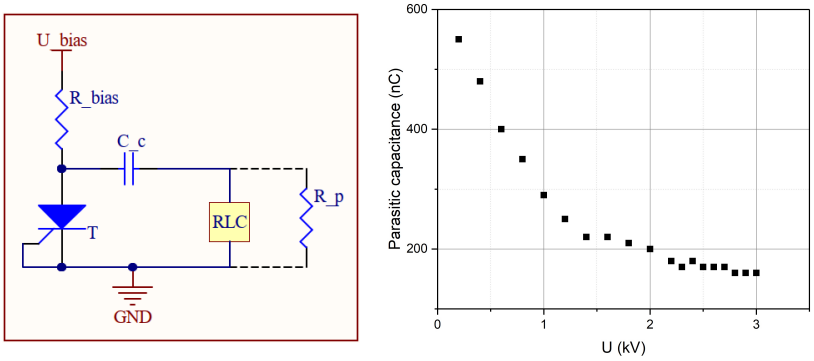
2. Materials and Methods

Previous literature establishes that ultra-fast thyristor triggering requires a significant slew rate and an overvoltage at least twice the static breakdown voltage of the thyristor ([9–12]); all whilst ensuring that enough current is available to guarantee the charging of the thyristor's internal parasitic capacitance at the required dU/dt (Section 1). Therefore, we need to first know the parasitic capacitance of the thyristors in use.

To assess the relationship between the internal parasitic capacitance and voltage for the 2.4 kV rated thyristor MPPCT750D240 [23], a test was conducted as depicted in Figure 1a. The biasing voltage applied via the DC power supply was gradually increased to facilitate the charging of both the thyristor's parasitic capacitance and the series coupling capacitor. Placing a resistor R_p in parallel with the RLC meter is intended to protect it from the charging current of the coupling capacitor during voltage changes. It should be noted that this resistance will only be active during voltage transitions, serving as a protective measure for the RLC meter.

The thyristor's parasitic capacitance was measured by applying a blocking DC voltage on the anode–cathode of the component, on a range from 200 V to 3 kV. The RLC meter measurement was set at 10 kHz. We incorporated a coupling capacitor between the thyristor anode (at positive U_{bias}) and the RLC meter. By ensuring that the value of the coupling capacitor exceeds the parasitic capacitance of the thyristor under measurement, we have addressed its influence by calculating its effect in series arrangement, resulting in $C\_c = 3.3$ nF.

The voltage dependence of the parasitic capacitance of the thyristor is illustrated in Figure 1b. In order to address radiation tolerance, specifically single-event burnout, we intend to implement a voltage derating strategy, limiting the applied voltage to no more than 60% of the nominal rated voltage—equivalent to 1.4 kV for a 2.4 kV rated component. At this biasing voltage, the thyristor exhibits a parasitic capacitance of 220 pF.



(**a**) (**b**)

Figure 1. Assessing the thyristor's parasitic capacitance. (**a**) Setup to measure the parasitic capacitance of a thyristor in relation to bias voltage using an RLC meter. (**b**) Voltage dependance of the MPPCT750D240 thyristor's parasitic capacitance.

Taking as a starting point a small thyristor stack generator, with the previously studied thyristors we know the operating point that the present pulse generator needs to reach:

1. Slew rate at turn-on $\frac{dU}{dt} > 1$ kV/ns.
2. Considering the static breakdown voltage $U_{BD} = 3$ kV, doubling it and substracting the biasing voltage $U_{bias} = 1.4$ kV, the output voltage needs to be $U_{out} > 4.6$ kV.
3. Current $I = C_{parasitic} \cdot \frac{dU}{dt} > 220$ A.

In order to give an overview of how this can be achieved, the methods, materials, and results are hereby presented in a trickle-down way: starting from the output of gate-boosted

SiC MOSFETs that achieve the aforementioned current output requirements (Section 2.1), we will delve into the driving methods that make it possible, all the way back to a standard pulse generator that could be found in any electronics laboratory (Section 2.2).

2.1. Gate-Boosting of SiC MOSFETs

Gate-boosting is a method aimed at speeding the switching transitions of SiC MOSFETs. It is based on the application of an overvoltage on the gate terminal during the commutation time of the device; thus fighting the internal lead inductance and semiconductor structure parasitic capacitances while avoiding permanent damage on said structure. Its effectiveness has been proven in [24], and we succeeded in testing the gate-boosting on a single transistor in previous works ([19–22]). After this test phase, we proceed to the next phase, where we seek to trigger several SiC MOSFET transistors in parallel in order to increase the output current of the pulse generator to more than 220 A, as the requirements explained in Section 2.

We decided to trigger all parallel SiC MOSFETs by a common driver to simplify the system, thus avoiding synchronization issues that could arise from using individual drivers for each transistor. We address the potential problematic coupling of the six parallel transistors between themselves by adding a microstrip to each branch. A microstrip is a transmission line configuration consisting of a conductive trace mounted on a dielectric substrate, with a ground plane on the reverse side [25]. This setup facilitates controlled impedance and effective signal propagation. This physically decouples the SiC MOSFET's respective drains and adds a certain time delay; this said delay is compensated by the geometrical property of the connection. Figure 2 shows the schematic including the six gate-boosted SiC MOSFETs and the corresponding microstrips acting as transmission lines, and Figure 3 shows a 3D rendering of the PCB layout.

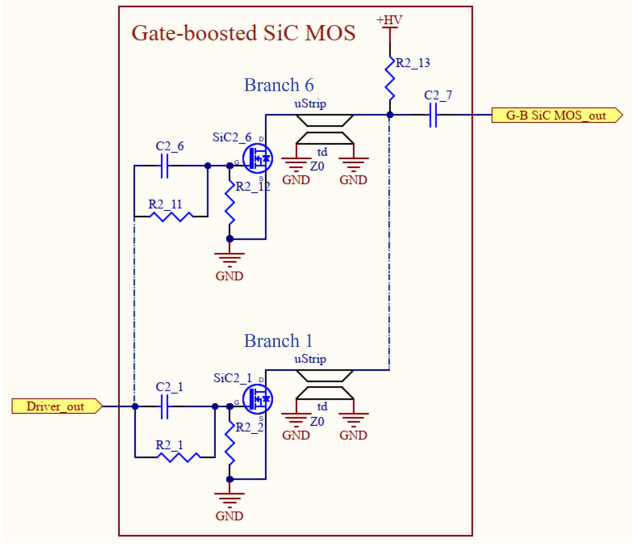


Figure 2. Schematic of the six SiC MOSFETs (*SiC2* _1 to _6), with the corresponding microstrips, in parallel.

To ensure gate boosting of these devices, the values of capacitors *C*2_1 through *C*2_6 are adjusted. These capacitors are used to counteract the impact of both input and reverse transfer (Miller) capacitance inherent in the SiC MOSFET being triggered. In our strategy, we prioritize controlling the total injected MOS gate charge (Q_{tot}) rather than attempting to measure or restrict the gate-source voltage at the wafer level.

To maintain adherence to this criterion, we use a capacitor (*C*2_1 to _6) in series between the driver output and the MOS gate. The choice of their value follows Equation (1):

$$(U_{dr_{max}} - U_{g_{max}}) \cdot C2\_i = Q_{tot}(@U_{g_{max}}) \quad (1)$$

where

- $U_{dr_{max}}$ represents the maximum output voltage of the gate driver circuit.
- $U_{g_{max}}$ is the absolute maximum allowable gate-source voltage.
- $C2\_i$ is the value of the series capacitor between the driver output and corresponding MOS gate.
- $Q_{tot}(@U_{g_{max}})$ denotes the total gate charge extrapolated from the datasheet curve at the maximum gate voltage.

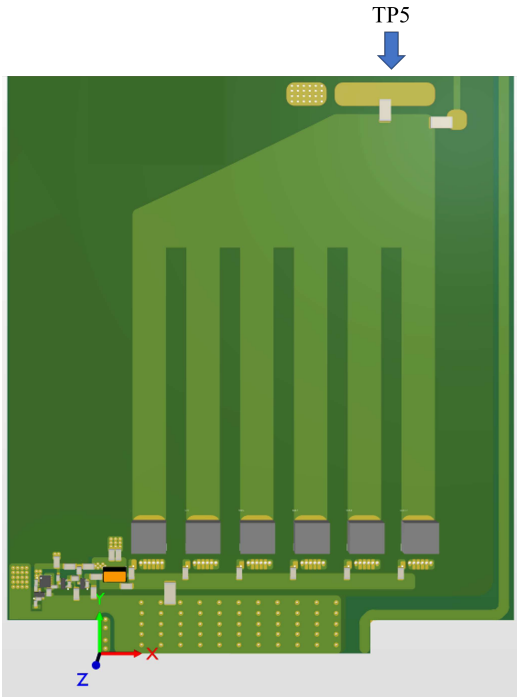


Figure 3. PCB 3D rendering representing the six SiC MOSFETs and microstrip branches of the pulse generator. The propagation delay of the individual SiC gate driving signal is mostly compensated for by the geometry of their drain transmission lines layout and the placement of the output feeding point on the opposite extremity.

This equation is rooted in three assumptions:

1. Q_{tot} follows a linear progression with the gate applied voltage and can as such be extrapolated, as per [26].
2. All relevant voltages are initially zero before triggering.
3. After the SiC reaches complete turn-on, the driver output voltage becomes $U_{dr_{max}}$, the MOS transistor gate-source voltage reaches $U_{g_{max}}$, and the series capacitor accumulates a charge of $(U_{dr_{max}} - U_{g_{max}}) \cdot C2\_i$. As $C2\_i$ is in series with the MOS gate, an equivalent charge is delivered to the MOS gate. While acknowledging a transient period and a brief duration of overvoltage on the gate, these considerations are intentionally deemed acceptable.

Regarding the gate resistors $R2\_1,3,5,7,9,11$ and $R2\_2,4,6,8,10,12$, they form a voltage divider with the goal to fix the DC gate voltage to <20 V, at Udr_{Vmax} as per [26]. It is important to note that any momentary spikes in the gate voltage exceeding this threshold during the commutation time have limited effects given the sub-nanosecond timescales involved. We accept some destructive effect of the transient overvoltage on the SiC gate (>100 V at package level; not measured at a wafer level), under the condition that the required lifetime is respected.

As per [20], we have adopted an aggressive triggering approach. This impacts the component's operational lifespan, albeit within acceptable limits for the system's overall lifetime. A lifetime of $>10^5$ pulses is esteemed sufficient for the kicker systems considered in these investigations [27].

2.2. Boosted Gate Driver

To achieve the SiC MOSFET boosting presented in Section 2.1, we previously designed a specialized driver (Figure 4) capable of delivering 430 V/ns to a 50 Ω load, with a maximum output voltage exceeding 300 V. The resulting output voltage was first presented in [19], as seen in Figure 5. We profit from the rapid switching capability of an avalanche transistor (Av0_1, [28]) to increase the output pulse dU/dt.

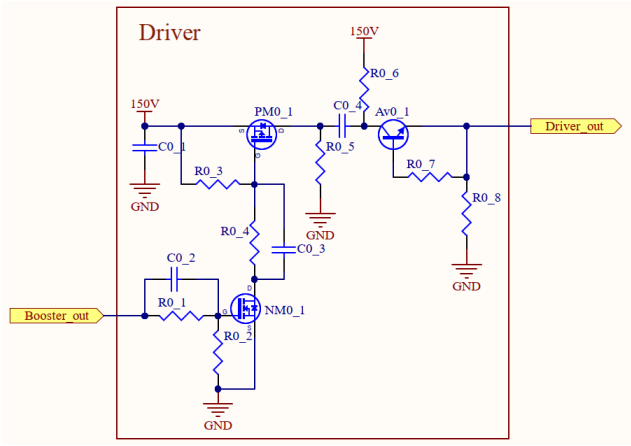


Figure 4. Schematic of the previous version of the SiC MOSFET gate-boosting driver.

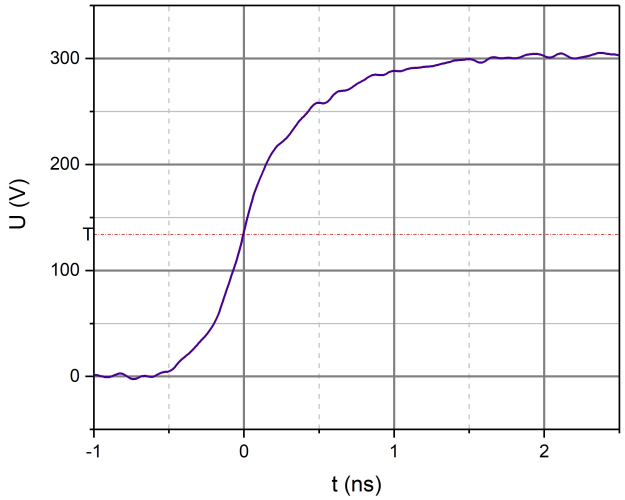


Figure 5. Output voltage of the gate-boosting driver on Figure 4, on a 50 Ω load at a charging voltage of 320 V. Maximum amplitude of 300 V and $t_r = 1$ ns, measured between 10–90%.

The first aspect when choosing the transistors for this driver is their rise time as declared on the datasheet. The faster the transistor, the better for our purposes: potentially, a fast transistor will reach a higher dU/dt and will therefore deliver a pulse that has more chances of resulting in driving the subsequent switching components in gate-boosting mode. Secondly, the total gate charge of the transistors is taken into account. Choosing a transistor with a lower total gate charge Q_g is advantageous because it leads to faster switching speeds and a lesser strain to the driver that switches it on, since it will need to provide less current.

After reviewing our prior research, we pinpointed a potential limitation in the driver's output current, if it was to be used to drive one or more parallel SiC MOSFETs with a significant gate charge. To tackle this challenge, we propose enhancing the driver with a GaN HEMT [29] current-boosting stage configured as a source follower (Figure 6). This upgrade is designed to amplify the output current while simultaneously reducing the stage's output impedance. Its placement on the PCB aims to minimize the loop surface and thereby

decrease stray inductance, as seen in Figure 7. Consequently, one of the criteria in choosing the driver's transistors is based on the shape and size of the package.

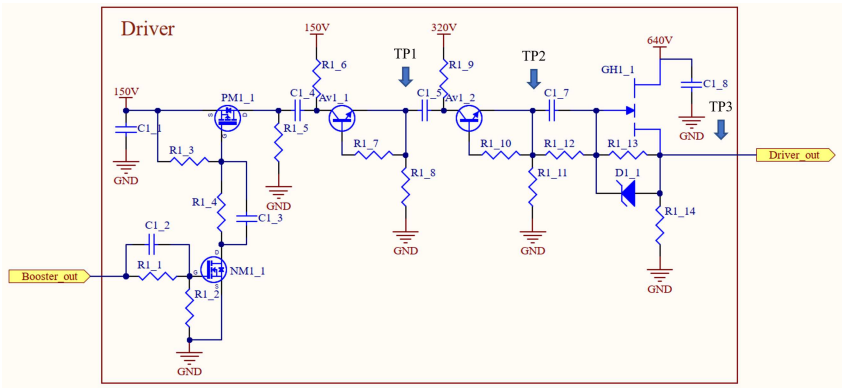


Figure 6. Schematic of the driver with its main stages: $NM1\_1$ and $PM1\_1$ as the fist level-shifting step, then the two-stage Marx generator with $Av1\_1$ and $Av1\_2$, and finally the normally-off $GH1\_1$ in source-follower configuration.

The decision to employ a GaN HEMT in the setup on Figure 6 is driven by the parameters detailed in Table 1. In comparison to alternative options with identical datasheet drain-source voltage and continuous drain current, the GaN HEMT demonstrates a significantly reduced total gate charge. During the switching process, the gate charge is required to be supplied to the switch's gate. A lower total gate charge corresponds to faster switching. Additionally, opting for a switch with a lower gate charge simplifies the design of the driving circuit, resulting in a compact solution, as the one presented in this paper. Regarding the package size criterion, the smaller form factor of the GaN HEMT results in decreased stray inductance. Overall, it is the most suitable component to meet our requirements.

Table 1. Comparison of choice criteria for GaN HEMT, Si MOSFET, and SiC MOSFET devices.

Parameter	**GaN GS66508T [29]**	**Si TK099V65Z [30]**	**SiC NVBG095N065SC1 [31]**
Package	GaNPX®	DFN8×8	D2PAK7L
U_{DS} (V)	650	650	650
I_D (25 °C) (A)	30	30	30
I_{DM} (25 °C) (A)	60	120	79
$Q_{g_{tot}}$ (nC)	6.1	47	50

Presently, on Figure 6, the initial stage involves a driving mechanism intended to elevate the triggering voltage while simultaneously refining the turn-on characteristics of the driving pulse. This driver comprises three essential components, seen in Figure 6: a level-shifting MOS circuit, a two-stage avalanche transistor Marx generator, and a source-follower GaN HEMT. The circuit up to the two-stage avalanche transistor Marx generator has been presented in previous works ([19–22]). The level-shifting circuit comprises two main components: an NMOS transistor (FDN86246 [32]) and a PMOS transistor (FDMC86262P [33]).

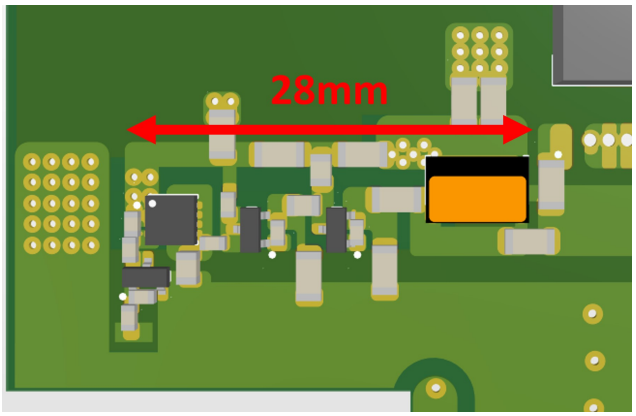


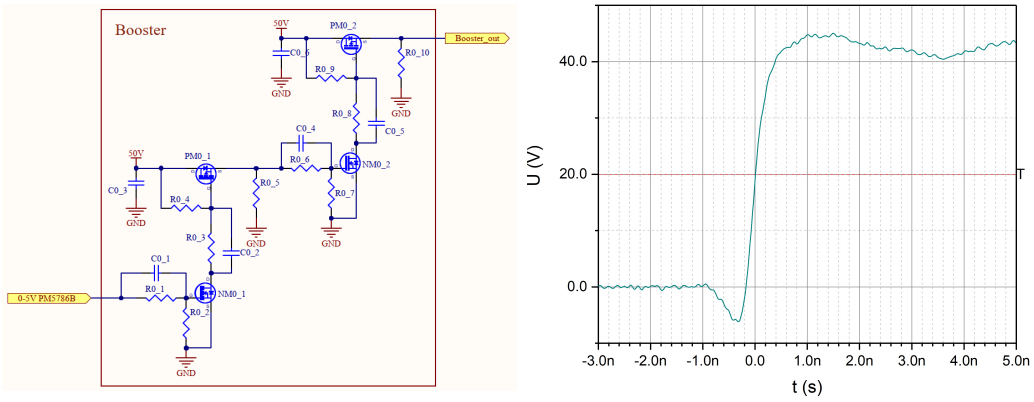
Figure 7. Dimensions of the driver. A more compact layout allows for a reduced stray impedance.

The NMOS transistor $NM1\_1$ in Figure 6 serves as the first level-shifting element, activated by a 45 V pulse at the "Booster" terminal. The capacitor $C1\_2$ is in series with the gate capacitance of the NMOS, which serves as a gate-boosting element to ensure fast switching. The resistors $R1\_1$ and $R1\_2$ form a voltage divider that keeps the voltage in the steady state at <20 V. Following this, we find a similar configuration for the PMOS transistor $PM1\_1$, with capacitor $C1\_3$ acting as a gate-boosting element for the PMOS like $C1\_2$ does for the NMOS, in series with its gate capacitance, and resistors $R1\_3$, $R1\_4$ and $R1\_5$ as the voltage divider that keeps the steady state voltage <25 V in this case. The capacitor $C1\_1$ serves as the bias voltage decoupling capacitor, whereas $C1_4$ is placed to add the output signal of PM_1 to the 150 V feeding voltage of the avalanche transistor $Av1\_1$ that follows.

The avalanche transistors $Av1\_1$ ([28]) and $Av1\_2$ ([34]) work in a two-stage Marx generator configuration. Accordingly, the fast-rising pulse of the PMOS drain (voltage on $C1\_1$ = 150 V) is added to the collector–emitter voltage of the avalanche transistor $Av1\_1$ (biased to 150 V, which is the voltage on its energy storage capacitor $C1\_4$) and triggers it in avalanche. The sum of voltages of $C1\_1$ and $C1\_4$ is then added to the collector–emitter voltage of the avalanche transistor $Av1\_2$ (biased to 320 V, which is the voltage on its energy storage capacitor $C1\_5$) and triggers it also in avalanche. At the end, the sum of the voltages on $C1\_1$, $C1\_4$, and $C1\_5$ appears on the $Av1\_2$ emitter, minus the corresponding voltage drops on PM_1, $Av1\_1$, $Av1\_2$ and on the series resistances of the energy storage capacitors $C1\_1$, $C1\_4$ and $C1\_5$. It should be noted that the actual limitation of $Av1\_1$ is approximately 165 V, as determined through laboratory testing. However, this is not the recommended producer use and therefore the biasing is limited to 150 V.

After this two-stage Marx generator, its output voltage drives the 650 V rated GaN HEMT via its coupling capacitor $C1\_7$. A decoupling capacitor for the GaN HEMT drain biasing $C1\_8$ is grounded as close as possible to the SiC MOSFET source to reduce its gate current loop length and, therefore, inductance. This is carried out to maximize the speed of the SiC MOSFET gate charging.

The driving circuit in Figure 6 employs a pulse trigger of 45 V, with a rise time of 425 ps and a slew rate of approximately 80 V/ns, as depicted in Figure 8b. This result stems from a custom voltage level-shifting process applied to the 10 V, 2 ns output signal from a Philips PM5786B (Fluke Co., Everett, WA, USA) pulse generator [35]. Utilizing gate-boosting, the input signal undergoes sharpening and amplitude amplification through the circuit shown in Figure 8a.



(**a**) (**b**)

Figure 8. The triggering pulse. (**a**) Schematic of the pulse booster for the Philips PM5786B pulse generator. (**b**) Output pulse on a 50 Ω load, labeled "$Booster_{out}$", with a charging voltage of 50 V. Maximum amplitude of 45 V, with a 10–90% rise time of 425 ps.

3. Results

3.1. Gate-Boosting of SiC MOSFETs

The results for a single IMBF170R450M1 SiC MOSFET (as per [22]) are depicted in Figure 9, illustrating three charging voltages in the range representing the later operation from 1.3 kV to 1.5 kV. The measurements were performed using a 50 Ω load and with an identical driver to the one detailed in Section 2.2.

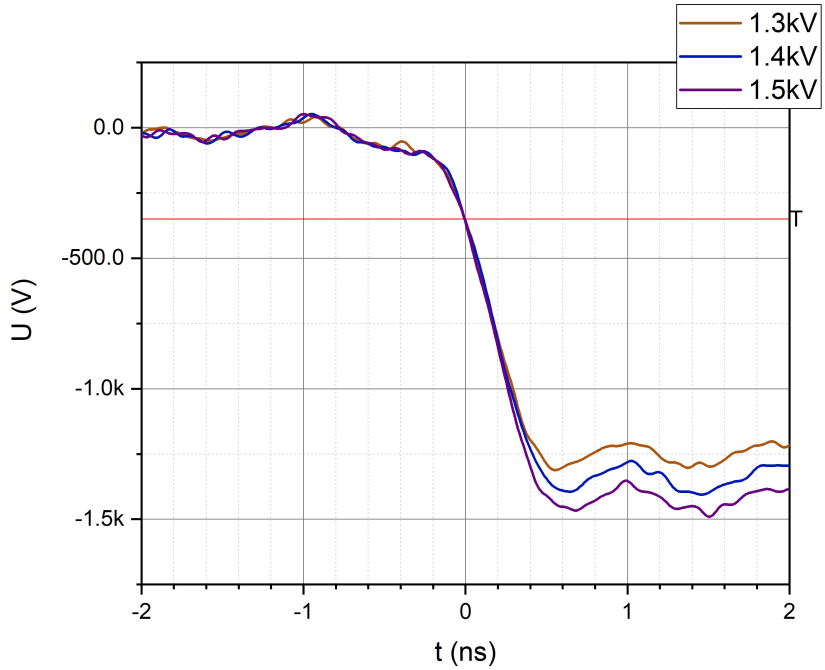


Figure 9. Output voltages obtained on a single IMBF170R450M1 SiC MOSFET on a 50 Ω load, at different charging voltages.

As previously described in Section 2.1, and represented in Figure 3, presently each SiC MOSFET has its own microstrip with ≈15 Ω impedance (FEMM calculation [36]) and ≈0.78 ns length which aims to mutually decouple the individual drains of the SiC MOSFET triggered by a common driver to cope with the spread of the switching times of each individual SiC MOSFET (Figure 3).

$$v_p(outer) = \frac{v_c}{\sqrt{\epsilon_{r_eff}}}$$
$$t_d(outer) = \frac{length}{v_p} \quad (2)$$
$$\epsilon_{r_eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \cdot (1 + 12 \cdot \frac{h}{W})^{-\frac{1}{2}} - \frac{\epsilon_r - 1}{4.6} \cdot \frac{t/h}{\sqrt{W/h}}$$

The delay calculation on an outer stripline on a PCB is described in Equation (2) [37], where

- v_p is the propagation speed, in this case on the outer layer of the PCB.
- v_c is the speed of light in vacuum.
- ϵ_{r_eff} is effective dielectric constant for microstrips.
- ϵ_r is the dielectric constant of the PCB material.
- h is the height of the substrate.
- t and W are respectively the thickness and width of the microstrip.
- t_d is the propagation delay due to the length of the microstrips in the outer layer of the PCB.

The outcome of this step is depicted in Figure 10, capturing the performance characteristics of our pulse generator with six SiC MOSFET transistors operating simultaneously. This test was performed with a charging voltage of 1.7 kV on an attenuator's 50 Ω load. The maximum amplitude of the output voltage is 3.2 kV and a 10–90% slew rate of 2 kV/ns.

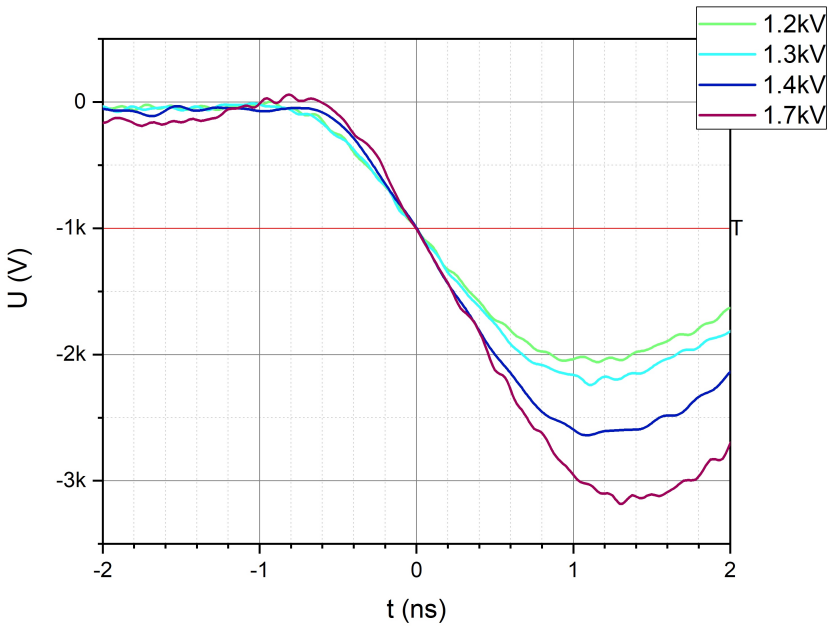


Figure 10. Output voltage of the six parallel IMBF170R450M1 SiC MOSFETs on a 50 Ω load (TP5, Figure 3), different charging voltages. At a 1.7 kV charging voltage, the maximum voltage amplitude is 3.2 kV and a 10–90% slew rate of 2 kV/ns.

The impedance mismatch of the microstrips with respect to the 50 Ω output load causes the reflection of the signal, almost doubling its voltage due to the superposition of the incident and reflected waves (reflection factor $\Gamma = 0.9$). This is the reason why the output voltage is higher than the feeding voltage of the SiC MOSFETs.

Given that the core intention of increasing the quantity of SiC MOSFETs primarily aims to amplify the output current of the pulse generator's driving phase, a focused experiment was undertaken specifically under the condition of a 4 Ω load. This testing procedure was performed to comprehensively evaluate the performance enhancement attributed to

the increased number of SiC MOSFETs. Moreover, we have reduced the feeding voltage according to the recommended derating in irradiated facilities [38].

The obtained results, for a test at 1.7 kV charging voltage on a 4 Ω resistive load with minimized inductive elements, graphically represented in Figure 11, show this. The output voltage on a less mismatched load (4 Ω for six 15 Ω microstripes in parallel) is reduced. However, the output curve exceeds the threshold of 220 A after calculation, delivering 400 A, making it 66 A per SiC MOSFET. According to its datasheet, this implies a 2.6× greater surge output current per SiC MOSFET than the datasheet established 24.8 A [26], lasting in the range of tens of nanoseconds. This upsurge in output current validates the effectiveness of incorporating additional SiC MOSFETs to the setup.

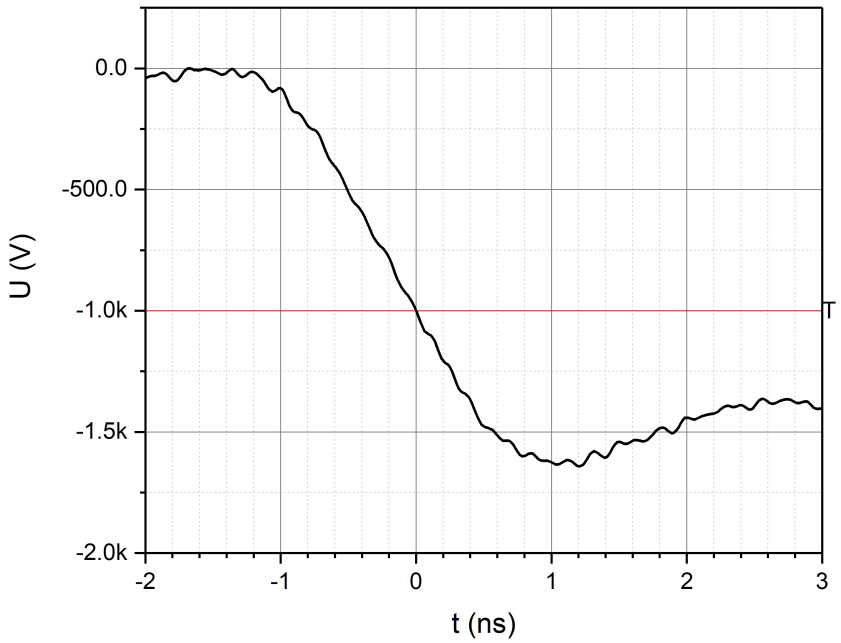


Figure 11. The output voltage of the six parallel IMBF170R450M1 SiC MOSFETs on a 4 Ω load (TP5, Figure 3), charging voltage 1.7 kV. The maximum voltage amplitude is 1.6 kV; hence, there is a calculated output current of 400 A.

3.2. Boosted Gate Driver

The following measurements are taken at the corresponding test points marked "TP" in Figure 6, with a 50 Ω attenuator, with the remaining circuit disconnected at each test point.

The output at the first avalanche transistor level is a pulse of 300 V in amplitude and a rise time of 1.2 ns; at the second avalanche transistor level, there is a pulse of 540 V in amplitude and a rise time of 1.5 ns (Figure 12). At this stage, the pulse does not rise quickly enough as required: after the initial steep ascent, the rate of dU/dt decreases.

After the two avalanche transistors, the addition of a GaN HEMT operated at 640 V makes the driver able to deliver >620 V onto a 50 Ω load (Figure 12) at ≈1 kV/ns in its fastest section (120–240 ps). These are sufficient conditions to trigger a MOS component in the gate-boosted mode.

In an attempt to find the limit of our approach, we operated our setup above the recommended derated voltage in irradiated facilities [38]. We consider operating at 640 V as safe since the GaN HEMT has a significant drain-source voltage margin (≈30%), as stated in its datasheet [29], and GaN technology devices are supposed to be immune against the single-event burnout (SEB) phenomenon. This is an abrupt failure caused by a high-energy hadron (proton or neutron), such as cosmic rays or, in accelerator facilities, stray radiation from the accelerator, striking a power semiconductor device, triggering an instantaneous breakdown of the device and compromising its reliability.

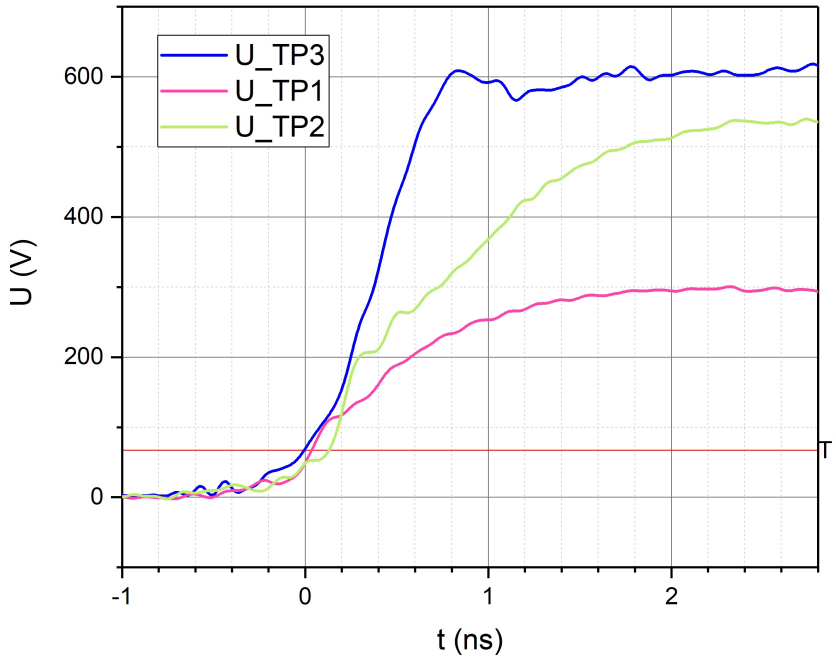
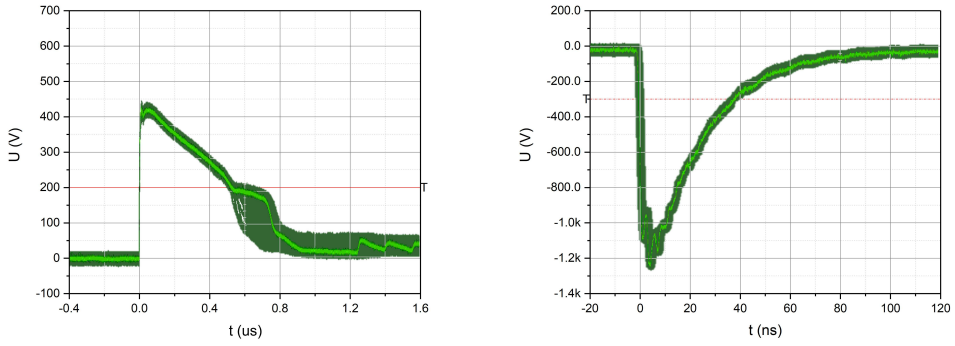


Figure 12. Output voltage of the FMMT413 (pink, TP1, Figure 6) and FMMT417 (green, TP2 Figure 6) avalanche transistors, charging voltages 150 V and 320 V, respectively, and for the GS66508T GaN HEMT (blue, TP3, Figure 6), all measurements are on a 50 Ω load. The final output has a maximum amplitude of 620 V and a maximum slew rate of 1 kV/ns.

In summary, our driver comprising two avalanche transistors and a GaN HEMT in series enables a sharp rising edge, achieving slew rates exceeding 1 kV/ns for the driving pulse. This is crucial for subsequently triggering high-voltage MOS components in the gate-boosted mode.

3.3. Lifetime Test

A total lifetime of 2×10^6 pulses (Figure 13a) is fulfilled for the driver. The test load for the driver consisted of a combination of 180 pF (six 30 pF coupling capacitors in parallel) in series with 3.5 Ω (six 20 Ω internal gate resistances of each SiC MOSFET in parallel). When connecting the driver to the six paralleled SiC MOSFETs, a total lifetime of at least 1×10^6 pulses (Figure 13b) is demonstrated on a 4 Ω load.



(**a**) (**b**)

Figure 13. Lifetime test. (**a**) Driver lifetime test, total 2×10^6 pulses. Loaded with 180 pF and 3.5 Ω to reproduce the six SiC MOSFET loading; charging voltage 640 V. (**b**) 6× SiC MOSFET lifetime test, total 1×10^6 pulses. Loaded with 4 Ω to reproduce the condition of an output current >220 A (calculated output current >300 A); charging voltage 1.3 kV.

Both lifetime tests conducted affirm that our pulse generator aligns with the commissioning criteria for a kicker magnet pulse generator in the beam dump section of the accelerator facility at CERN [27]. However, the results are preliminary, as no statistical lifetime test has been conducted.

Given the negligible steady-state thermal dissipation in our setup and the extremely low duty cycle in our applications (<0.0001%), dynamic thermal dissipation can also be considered negligible. Consequently, we did not conduct any heat management studies on our devices.

4. Summary

Our work focuses on developing a novel methodology to trigger industrial thyristors for high-voltage applications, particularly in particle accelerators. Our methodology relies on boosted gate triggering to significantly improve the switching characteristics (dU/dt and dI/dt) of SiC MOSFET devices, allowing for faster and more efficient operation compared to conventional triggering techniques.

Presently, this paper introduces the latest improvements to the driving of SiC MOSFETs in view of reaching the sufficient output voltage, current and dU/dt to trigger thyristors in the impact ionization mode. In summary, our efforts have resulted in an approach to amplify the current output of our driver circuit, leading to sub-nanosecond performance. By pushing components off the shelf to their limits, we have achieved a pulse generator with an output current exceeding 220 A and a turn-on slew rate exceeding 1 kV/ns. However, the final output voltage falls short of twice the breakdown voltage for the 2.4 kV rated thyristors. To address this limitation, we will incorporate a D2PAK thyristor Marx generator to meet the requirements of a future stack utilizing the 2.4 kV rated thyristors.

Despite the challenges faced, the proposed solution offers significant advantages. The use of compact topologies and commercially available components results in a design that is smaller and reproducible, with potential cost benefits. The design of the gate-boosting driver enhances the MOSFET's output voltage, slew rate, and current, enabling faster commutation times and suitability for higher loads, thus facilitating ultra-fast switching. Furthermore, the developed technology's ability to respond rapidly to beam dump requests presents a potential for replacing traditional systems in particle accelerators, promising and improved performance if implemented. Our approach provides a nanosecond delay from trigger request to the output signal, unlike the opening switch approach, which necessitates a preparation period exceeding 500 nanoseconds—a crucial disadvantage compared to our approach.

Looking forward, our primary objective remains focused on building a stack of thyristors to reach the voltage and current requirements of our target application in the accelerator complex at CERN. The next immediate step involves boosting the output voltage of the described setup using a Marx stage with thyristors triggered in impact ionization (II) mode. Optimization and reliability testing of this stage are currently in progress.

Presently, we have developed a technology capable of responding to an accelerator's beam dump requests within nanoseconds, thereby reducing the reaction time of existing technologies by two orders of magnitude. Upon establishing the reliability of the whole chain of this triggering method for accelerator systems, there exists the potential for this technology to replace traditional thyratron-based systems.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

COTS	Commercial Off-The-Shelf
CP	Capacitive Probe
D2PAK	Double Decawatt Package, TO-263
DSRD	Drift Step Recovery Diodes
FEMM	Finite Element Method Magnetics
HEMT	High Electron Mobility Transistor
HF	High Frequency
HV	High voltage
IGBT	Insulated-Gate Bipolar Transistors
II	Impact Ionization
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PFL	Pulse Forming Line
SEB	Single Event Burnout
SOS	Semiconductor Opening Switch

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