ATLAS Level-0 Muon Barrel Trigger System Status and Integration Tests for Phase-II

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Abstract

In preparation for the High-Luminosity Large Hadron Collider (HL-LHC), essential upgrades are underway for the ATLAS Level-0 Barrel Muon Trigger system in order to cope with the higher data rates and radiation level. These enhancements involve incorporating a new inner layer of Resistive Plate Chambers detectors (RPCs), and replacing the trigger and readout electronics, using a novel Data Collector and Transmitter (DCT) and new Sector Logic (SL) boards. DCT boards collect and process RPC data, while SL boards execute the trigger algorithm and transmit the muon candidates to the Central Trigger Processor.

This paper presents the current status of the Phase-II Muon Barrel Level-0 Trigger system, focusing on the DCT and SL hardware and firmware developments. We detail the design and testing processes. Results from data communication tests and ongoing developments are also discussed.

Keywords: ATLAS, Level-0 trigger, Muon Spectrometer, Phase-II upgrade, RPC, DCT, SL, FPGA, HL-LHC, data transmission

1. Introduction

The ATLAS experiment at CERN is upgrading its Level-0 (L0) Muon Barrel Trigger system for Phase-II to handle the increased data rates and radiation levels of HL-LHC ([1]). Upgrades include a new inner RPC layer and the replacement of both the on-detector and off-detector electronics ([2], [3]). The system (Fig. 1) identifies L0 muon trigger candidates using Resistive Plate Chamber detectors (RPCs) and the Tile Calorimeter. Trigger candidates are validated by the Monitored Drift Tube Trigger Processor (MDTTP) before being forwarded to the Muon Central Trigger Processor Interface (MuCTPI). The system also performs data readout, delivering the RPC data to the FELIX ([4]) upon the L0 Accept signal arrival. The L0 Muon Barrel Trigger system employs 32 Sector Logic (SL) boards to execute the trigger and readout algorithms for one of the ATLAS trigger sectors. Each FPGA-based board is housed in ATCA shelves outside the ATLAS cavern.

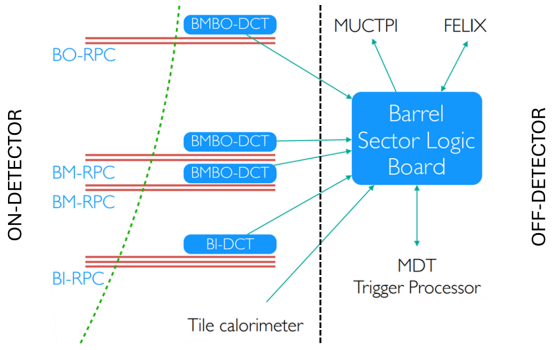

Figure 1: Simplified schema of the L0 Muon Barrel Trigger System.

SLs receive RPC data from the on-detector Data Collector and Transmitter (DCT) boards, which are also FPGA-based and gather signals from the RPC detectors. A total of 1546 DCT boards are planned, with two variations to accommodate dif-

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ferent electronics: BMBO-DCTs for the legacy RPCs, and BI-DCTs for the new BI RPCs.

2. System Architecture

2.1. On-detector Electronics: DCT

The 1208 BMBO-DCTs, used for the legacy system, utilize the Artix-7 XC7A200 Xilinx FPGA. They digitize the RPC signals with 800 ps time binning using FPGA-TDC and employ zero-suppression logic. A key component is the lpGBT ASIC ([5]) which handles the bi-directional optical communication with the SL. It provides an uplink with a bandwidth of 10.24 Gb/s (8.96 Gb/s user data when FEC5 coded) for transmitting data and monitoring information from the DCT to the SL. Configuration FEC5 encoded commands arrive from the SL at 2.56 Gb/s (1.28 Gb/s user data).

The BI-DCT FPGA firmware, used for the new RPCs, is a specialized version of the BMBO. In contrast to BMBO-DCT, which primarily measures the rising edge time of the RPC signals, BI-DCT receives them already digitized and Manchester encoded by the new RPC on-detector ASIC. The BI-DCT firmware includes custom designed blocks designed to deserialize and decode Manchester signals received at 600 Mb/s. For the 338 BI-DCT boards a Xilinx Kintex-7 XC7K325 FPGA is needed: the algorithm occupies 55% of the available LUTs.

The firmwares currently include all the decoding logic, configuration, and basic monitoring functionality.

2.2. Off-detector Electronics: SL

Each SL board, based on the Virtex Ultrascale+ XCVU13P FPGA, process RPC data received from up to 50 DCTs (BI and BMBO) via optical fibers. An lpGBT-FPGA core decodes and encodes data from and to the DCTs. The trigger logic applies a trigger algorithm to identify muon candidates by requiring hit coincidences in three out of four RPC layers within defined windows. Per every event, up to four trigger candidates per RPC sector, are generated and forwarded to MDTTP for further verification and then to the Muon Central Trigger Processor Interface for final processing.

The SL also implements the readout logic, which temporarily stores data in dual-port RAM memories, awaiting L0-Accept signals. Upon acceptance, data is sent to the readout system via FELIX modules.

3. Testing and Results

The test setup for the L0 Muon Barrel trigger and readout electronics involves ensuring successful communication between the DCT and SL boards using the lpGBT protocol. To achieve this, two separate firmwares were developed and used for the first BMBO-DCT and SL prototypes.

On the SL side, an lpGBT-FPGA core plus a GTY transceiver operating at 10.24 Gb/s for RX and 2.56 Gb/s for TX have been used for the optical serial link. Control and monitoring software (based on [6]) has been connected to the lpGBT-FPGA core and used for managing the DCT lpGBT ASIC configurations, as well as FPGA and flash programming.

To qualify the configured uplink and downlink, eye diagrams have been stored for each one. The results in Fig. 2 and Fig. 3 shown a large open area (over 60%) for both the connections, expected for an error-free communication.

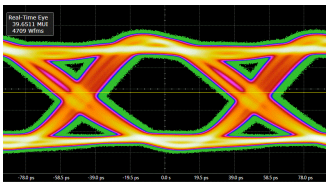

Figure 2: Uplink Eye diagram.

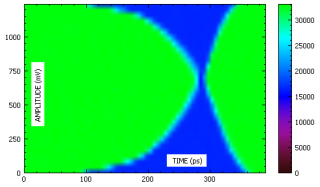

Figure 3: Downlink Eye Diagram.

To run a BERT test, the DCT and the SL board have been programmed with special test firmware in order to transmit a fixed pseudo-random pattern from the lpGBT-FPGA to the lpGBT ASIC, and vice versa. The receiving firmware decodes the data and verifies it. Integrated Logic Analyzer IP cores confirm zero errors over a continuous 24-hour test period.

4. Future Work and Conclusion

The development of the new L0 Muon Barrel Trigger system has reached a significant milestone with the successful operation of the first BMBO-DCT and SL prototype and the ongoing testing of the second BMBO-DCT prototype.
The firmware of the BI-DCT has been completed and simulated with MC data, prototype schematic design is finished with layout in progress. The first prototype is set for delivery by the end of the 2024, and it will benefit from the successful results of the BMBO-DCT upon which it is based. To further enhance the system's muon detection capabilities, various trigger algorithms are being explored. These include spatial coincidences, pattern matching and neural networks.
Scheduled for completion in 2024, radiation-hardness testing is a critical step to ensure the system's reliability within the high-radiation environment of the ATLAS detector.

Preliminary tests of the Phase-II Muon Barrel L0 Trigger system have demonstrated promising performance. With continuous development and thorough testing, the DCTs and SL hardware and firmware are going to meet the stringent requirements of the ATLAS experiment upgrade.

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