



ALICE ITS3: A truly cylindrical vertex detector based on bent, wafer-scale stitched CMOS sensors

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ARTICLE INFO

Keywords:

Particle tracking detectors
Monolithic Active Pixel Sensors (MAPS)
Bent sensors

ABSTRACT

The new inner tracking system (ITS2) of the ALICE experiment at the LHC, upgraded during the LHC Long Shutdown 2 (2019–2021) with CMOS monolithic active pixel sensors (ALPIDE), is currently taking data and demonstrating excellent performance in the LHC Run 3. A replacement of the three innermost layers of the ITS2, called ITS3, is foreseen during the LHC Long Shutdown 3 (2026–2028) to further improve its tracking precision and efficiency, particularly at very low transverse momentum down to $p_T = 0.1$ GeV/c. The ITS3 is a cylindrically bent silicon vertex detector based on stitched wafer-scale monolithic active pixel sensors with 65 nm CMOS technology. The large stitched sensors are 26.6 cm in length and can be thinned down to below 50 μm , where the sensors are flexible to be bent to form truly cylindrical detector half-barrels. An extremely low material budget of 0.05% X_0/X_0 per layer can be achieved in combination with air-cooling and lightweight carbon foam spacers as support structures.

In this article, an overview of the ALICE ITS3 and the R&D achievements including detector concept, sensor design and technology qualification, sensor bending, detector mechanics and cooling, and system integration will be given.

1. Introduction

ALICE [1] (A Large Ion Collider Experiment) is a general-purpose detector designed for heavy-ion physics studies at the Large Hadron Collider (LHC). The ALICE detector is specifically designed for probing the characteristics of quark–gluon plasma and matter that interacts strongly under extremely high energy densities. This is achieved through the analysis of various types of collisions, including nucleus–nucleus, proton–proton, and proton–nucleus.

The ALICE detector primarily focuses on reconstructing tracks from events with a high multiplicity in central Pb–Pb collisions and providing particle identification over a wide transverse momentum range. Fruitful scientific outcomes have been obtained using the data collected in the LHC Run 1 and 2 [2]. During the LHC Long Shutdown 2 (LS2) from 2019 to 2021, ALICE underwent major upgrades [3,4] to extend its physics capabilities with a significant improvement in tracking precision and efficiency, especially at low transverse momentum. A key component of these upgrades is the newly developed Inner Tracking System (ITS2), which is an entirely silicon-pixel vertexing and tracking detector built with CMOS monolithic active pixel sensors (MAPS), known as ALPIDE [5]. It has been operational and taking physics data since the beginning of LHC Run 3 on July 5th, 2022. The detector has demonstrated excellent performance with a very satisfactory low noise

level and a stable pixel threshold in the first two years of Run 3 during both proton–proton and Pb–Pb collision data taking periods.

To further improve the detector's pointing resolution and tracking efficiency, particularly for particles with very low transverse momentum down to $p_T = 100$ MeV/c, an upgrade to the three innermost layers of the ITS2, called ITS3 [6,7], is scheduled for the LHC LS3 between 2026 and 2028.

2. Detector concept

The ITS3 is a cylindrical silicon vertex detector leveraging advanced 65 nm CMOS technology for its stitched wafer-scale MAPS [8]. These sensors are both large, measuring 266 mm in length, and remarkably thin, with the capability of being reduced to under 50 μm . This thinness grants the sensors enough flexibility to be shaped into true cylindrical half-barrels, as depicted in Fig. 1. The ITS3 detector is structured into three layers, designated as L0, L1, and L2, with respective target radii of 19.0 mm, 25.2 mm, and 31.5 mm. Each of these layers is further segmented into two sub-layers, forming two sets of half-layers, denoted as H-L0, H-L1, and H-L2. The simplified schematic of the half-layer 0 (H-L0) is shown in Fig. 2. Each half-layer consists of a

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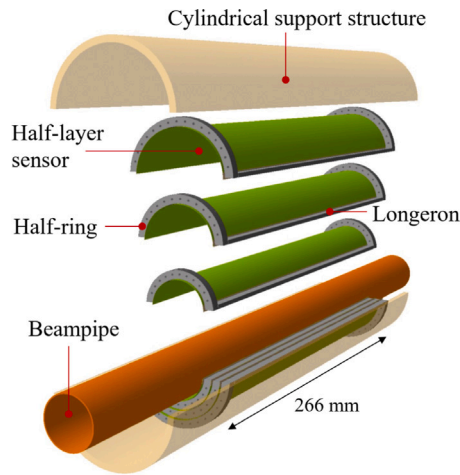


Fig. 1. Sketch of the ITS3 detector layout.

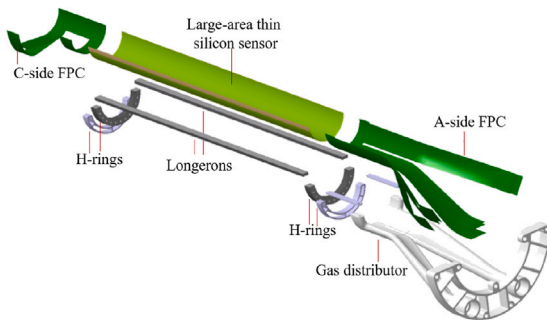


Fig. 2. Exploded view of the conceptual layout of H-L0.

wafer-scale stitched sensor, flexible printed circuits (FPCs), lightweight support structures, a radiator half-ring, and a gas distributor. A very homogeneous material distribution can be achieved by eliminating water cooling, readout circuits, and most of the support structures in sensitive areas, which results in a significant material budget reduction, from 0.36% X/X_0 to 0.05% X/X_0 , compared to the ITS2 inner barrel layers. The innermost layer's position has been adjusted to 19 mm from the interaction point, closer than ITS2's first layer at 23 mm. These enhancements will significantly improve the precision, particularly of heavy-flavor hadron measurements [9].

3. Sensor design and characterization

The design of the sensor ASIC (application-specific integrated circuit) for the ITS3 detector is guided by the knowledge and experience gained during the development and operation of the ALPIDE sensor for the ITS2 detector [10,11]. The new ASICs utilize the Tower Partners Semiconductor Co. (TPSCo) 65 nm process for its smaller feature size and the capability to use larger 300 mm wafers, enabling the production of 26 cm long stitched sensors. This stitching technique connects multiple reticles to form a larger sensor segment. In the manufacturing process, specific parts of the reticle known as repeated sensor units (RSUs) are systematically arranged adjacent to one another on the silicon wafer. Additionally, end-cap structures are positioned at both the left and right extremes of these RSUs. To accommodate the different dimensions required for the three layers of the ITS3, segments are cut from the wafer in groups of three, four, or five to create the respective half-barrels. The development process of the ITS3 sensor ASIC is systematically divided into three critical stages: verifying the chosen technology, ensuring the yield and efficacy of stitching, and designing the full-scale sensor ASIC.

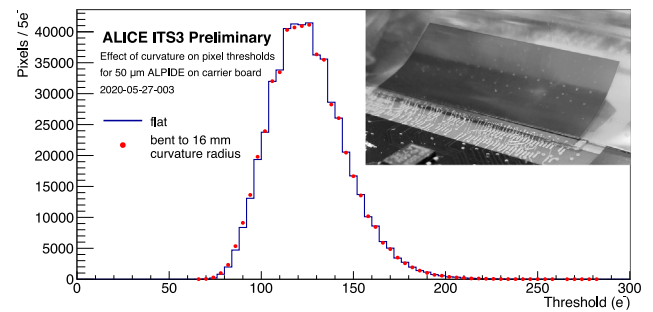


Fig. 3. Comparison of pixel threshold distribution before and after bending the sensor along the short edge.

Several pixel test structures have been designed and submitted with the first multi-reticle-layer (MLR1) run in 2021 to optimize the fabrication process and qualify the technology in terms of detection efficiency, spatial resolution, charge collection time, power consumption, and radiation hardness. The MLR1 prototypes underwent thorough testing both in the laboratory and through beam tests. The prototypes demonstrated excellent performance in terms of detection efficiency (> 99%) and spatial resolution (3–4.5 μm), and the performance can be sustained at the required ITS3 radiation loads [12].

Following the successful verification of the TPSCo 65 nm technology, two large stitched sensors, the monolithic stitched sensor [13] (MOSS) and the monolithic stitched sensor timing (MOST) have been designed and submitted with the first engineering run (ER1) in 2022 to assess the yield, stitching and power distribution. Extensive characterizations for the MOSS and MOST have been started in June 2023. Meanwhile, the fully functional prototype sensor is being designed based on the experience learned from the MLR1 and ER1 prototypes. This final prototype is expected to be submitted with the ER2 in the second half of 2024.

4. Sensor bending

Silicon wafers are initially thinned down to varying thicknesses through a back-grinding process. Subsequently, chips and test structures diced out from the wafers are bent to different radii using specialized tools. The procedure has been optimized through a series of tests to meet the ITS3-specific requirements.

The characterization of bent sensors made using 180 nm and 65 nm CMOS technology processes has been conducted with a focus on both mechanical and electrical properties. This study is essential to understand how the bending, or curvature, of these sensors might impact their overall performance.

As an initial stage, the ALPIDE chips are thinned down to 50 μm and bent along their short edge and long edge, respectively. The chips remain fully functional after bending. The observed changes in current consumption were approximately $\pm 10\%$ and $\pm 5\%$ for bending along the short and long edges, respectively. These deviations, attributable to piezo-resistive effects, are significantly influenced by the orientation of current mirror transistors within the ALPIDE chip's architecture [14]. These changes are within the operational tolerances for ALPIDE chips. The deviations of pixel charge threshold are negligible between the bent and flat sensors, as shown in Fig. 3.

To validate the functionality of bent sensors, a dedicated test setup, called μITS3 , is built, as shown in Fig. 4. This assembly includes six ALPIDE sensors, each 50 μm thick, curved along the long edge to the intended radii for ITS3. The performance of those bent sensors on μITS3 was characterized by using a 5.4 GeV electron beam at the DESY test beam facility. The detection inefficiency as a function of the pixel threshold for three ALPIDE sensors is shown in Fig. 5. The analysis indicates that the inefficiency is independent of the bending radius and

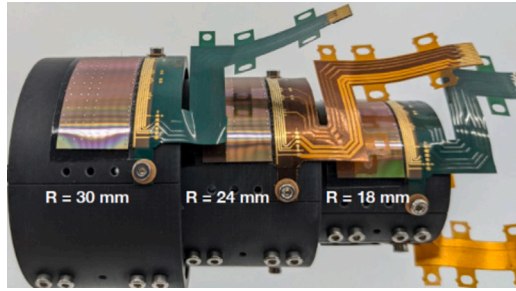


Fig. 4. μ ITS3 assembly. The bent ALPIDE chips are fixed onto cylindrical jigs.

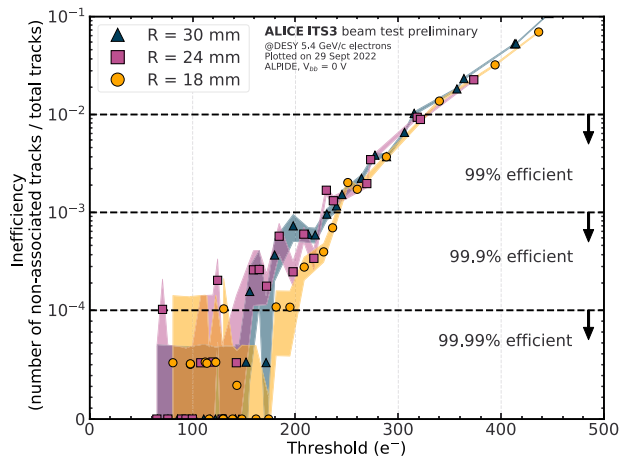
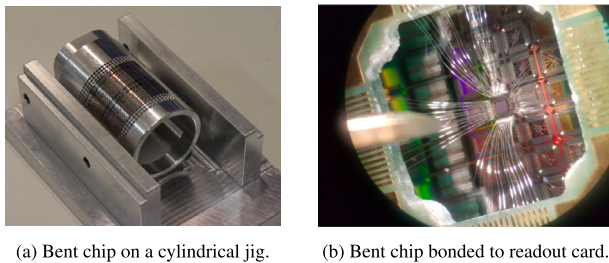


Fig. 5. Detection inefficiency as a function of threshold. Three ALPIDEs were bent along the long edge to radii of 18 mm, 24 mm and 30 mm, respectively.

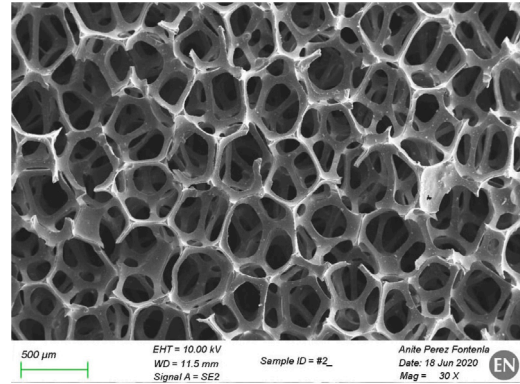


(a) Bent chip on a cylindrical jig. (b) Bent chip bonded to readout card.

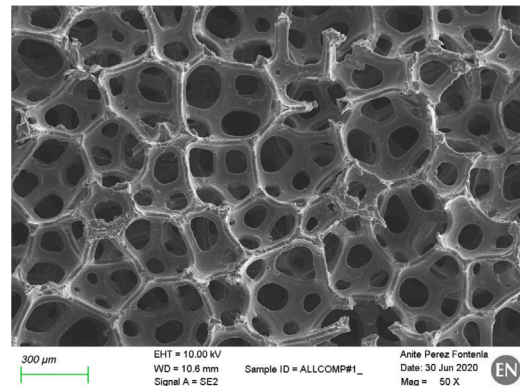
Fig. 6. Bent MLR1 chip. (a) A bent MLR1 reticle chip glued onto a cylindrical jig. (b) The bent digital test structure was bonded to the custom-made adapter card.

the sensors can be operated with an inefficiency of 10^{-2} in a wide pixel threshold range. The detection efficiency is also consistent with the performance of the flat ALPIDE sensor. Notably, at the typical threshold value of approximately 100 electrons, inefficiency remains below 10^{-4} , demonstrating robust performance for normal operation.

To accommodate the small dimensions of the MLR1 test structures, chips containing four MLR1 reticles each, totaling an area of 2.4×3.2 cm² and a thickness of approximately 40 μ m, are bent by using a cylindrical support jig with a known curvature radius, as depicted in Fig. 6(a). The bent prototypes are then electrically connected to a readout card via wire bonding, as shown in Fig. 6(b). Preliminary measurements using ⁵⁵Fe sources indicate that the spectral response of the MLR1 prototypes is uniform across both bent and flat configurations, with no significant variation in the seed pixel signal distributions observed.



(a) Carbon (RVC) Duocel



(b) Allcomp K9 standard density

Fig. 7. Microscopic views of the carbon foams for ITS3. The scale varies between images (a) and (b).

5. Mechanics and cooling

The short-term stability of the sensor is required to vary by no more than 2 μ m to ensure it is smaller than the sensor's spatial resolution. The operational temperature of the sensor must remain below 30 $^{\circ}$ C, a condition essential for mitigating thermal noise and ensuring reliable performance. Furthermore, the maximum temperature gradient within the pixel matrix region should be confined to less than 5 $^{\circ}$ C to maintain consistent operation and uniformity across the sensor. To minimize the material budget impact on the sensor-sensitive region and ensure the required detector performance, any mechanical contributions must be minimized. Air-cooling is selected to efficiently dissipate sensor-generated heat while keeping the material budget at a minimum [15].

Carbon foam has been identified as the optimal material to satisfy various requirements for ITS3. Two varieties of open-cell reticulated vitreous carbon (RVC) foams have been chosen based on the functionality of the mechanical components. A low-density foam (45 kg/m³) with a high stiffness, Carbon Duocel, is selected as the support longerons. Meanwhile, for the cooling radiator, the Allcomp K9 standard density RVC foam, distinguished by its high thermal conductivity (25 W/(m K)), has been chosen. The microscopic structures for both mentioned carbon foams are shown in Fig. 7.

Several mechanical prototypes have been designed and produced to thoroughly investigate and optimize the ITS3 cooling and mechanics performance. A breadboard model (BBM), referred to as BBM3 and depicted in Fig. 8(a), was constructed to emulate the thermal performance of a half-detector. It consists of three half-layers, each composed

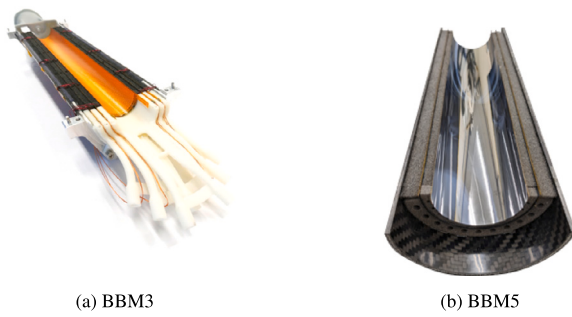
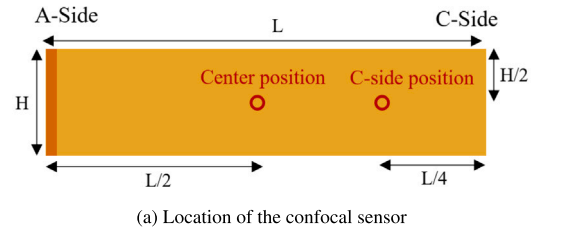
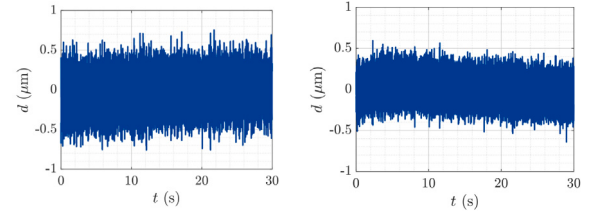


Fig. 8. Breadboard models assembled for ITS3. (a) BBM3 for thermal and aeroelastic tests. (b) BBM5 for thermo-elastic test.



(a) Location of the confocal sensor

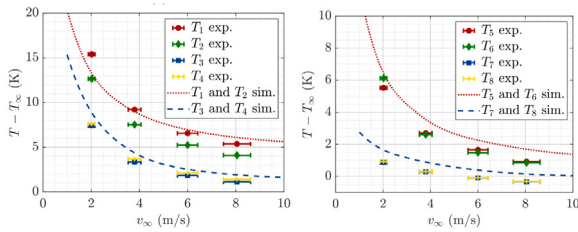


(b) Displacement at center position (c) Displacement at C-side position

Fig. 10. Displacement results of the aeroelastic tests measured on the H-L2 of BBM3.



(a) Location of the temperature sensors



(b) Endcap of H-L0

(c) Matrix of H-L0

Fig. 9. Temperature difference in the dummy silicon H-L0.

of dummy silicon incorporated with polyimide heaters. These layers include 40 μm of silicon, a 5 μm copper serpentine, and intervening polyimide layers. Two different copper serpentine designs are integrated into the dummy silicon heater to simulate heat dissipation in the endcap and matrix regions. The temperature at the polyimide surface interfacing with the silicon is measured by using eight PT1000 resistance temperature detectors (RTDs). The position of the RTDs is described in Fig. 9(a). The measured and computational fluid dynamics (CFD) simulated temperature difference as a function of average airflow freestream velocity for the endcap and matrix regions are shown in Figs. 9(b) and 9(c), respectively. For the matrix and end-cap regions, the surface power densities are 25 mW/cm^2 and 1000 mW/cm^2 , respectively. One can see that with an average freestream airflow velocity (v_∞) of approximately 8 m/s between the layers, the detector is capable of operating at a temperature that is 5 $^\circ\text{C}$ higher than the inlet air temperature (T_∞), and there is an overall good agreement between the CFD simulations and the measurements. Additionally, temperature uniformity along the sensor can be maintained within a 5 $^\circ\text{C}$ range.

The vibrational response and positional stability of the large curved sensor area are studied through finite element modal and dynamic response analyses, which are further validated by experimental tests using the BBM3. The vibration measurements are conducted using non-contact displacement sensors, known as confocal chromatic displacement sensors, which prevent perturbation of the airflow approaching the half-layers and are mounted on two different positions along the beampipe axis to measure H-L0 and H-L2 as depicted in Fig. 10(a). The displacements measured at the center and C-side positions with an average freestream airflow velocity (v_∞) of 8 m/s as a function of time for H-L2 are shown in Figs. 10(b) and 10(c), respectively. The maximum peak-to-peak displacement is about 1.1 μm and the RMS is below 0.4 μm , which well meets the ITS3 requirements.

Another breadboard model, called BBM5 as depicted in Fig. 8(b), was built based on blank silicon half-layers and carbon foam supporting structures to assess potential failures of the half-layers caused by thermo-elastic deformation. The BBM5 is tested in a climate chamber where the temperature is increased to 40 $^\circ\text{C}$ and then decreased to 10 $^\circ\text{C}$. This temperature change is executed in increments of 2 $^\circ\text{C}$, each maintained for a 15-minute interval, with a ramp rate of 0.5 $^\circ\text{C}$ per minute. Additionally, to ensure consistency in conditions, the relative humidity within the climate chamber is kept constant at 50% throughout the thermal cycling process. During the 50-hour testing phase, which encompasses several thermal cycles, the prototype demonstrates resilience, showing no detrimental effects from the temperature fluctuations.

6. Detector integration

The detector half-layers are initially assembled, followed by the process of gluing these half-layers together to form the complete half-detector.

The procedure for half-layer assembly is described in Fig. 11. The flat sensor is first bent to the target radius by using a specifically designed mandrel. Then, the FPC is mounted onto the mandrel and aligned to the half-layer sensor. The electrical interconnection between the sensor and the FPC is realized by wire-bonding. Finally, the half-layer is glued onto the cylindrical structural shell and connected to the corresponding air distributor. The first assembled demonstrator H-L0 with MLR1 wafer is shown in Fig. 12.

7. Summary

The ITS3 project involves the replacement of the inner barrel of ITS2 with stitched wafer-scale 65 nm MAPS, aimed at enhancing pointing resolution and tracking efficiency. The 65 nm CMOS technology has been validated based on the characterizations of the MLR1 prototypes. Initial laboratory and test beam evaluations of the first stitched sensors are in progress. Furthermore, ongoing efforts are directed towards designing the fully functional ITS3 sensor prototype. Notably, experiments with bent ALPIDE chips have confirmed the viability of operating bent silicon sensors without compromising performance efficiency. Procedures for sensor bending, interconnection, and detector integration have been verified, and further optimizations are underway. The production of ITS3 final sensors is scheduled for 2025, with detector installation expected during LHC LS3 between 2026 and 2028.

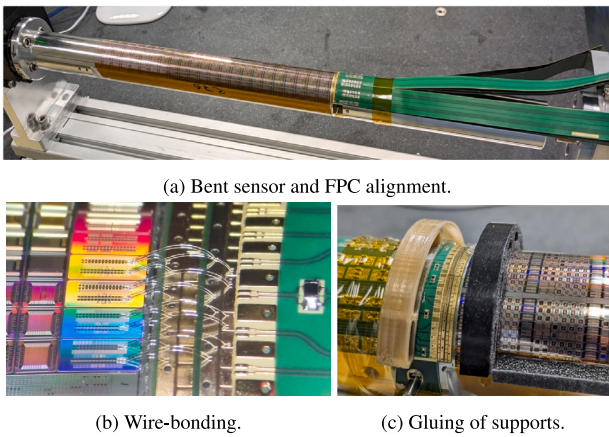


Fig. 11. Half-layer assembly procedure. (a) Alignment of the bent sensor and FPC. (b) Electrically connecting the sensor to the FPC via wire-bonding. (c) Gluing the mechanical supports.

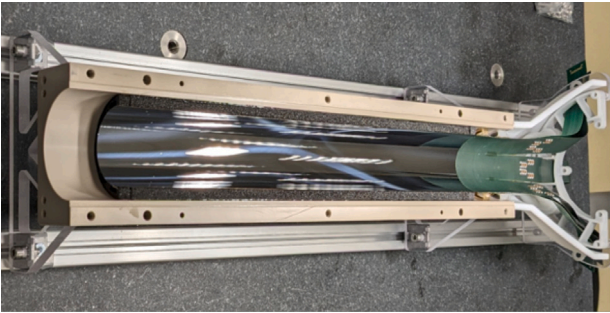


Fig. 12. Assembled first demonstrator H-L0.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

The measurements leading to the results of the bent ALPIDE chips have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF). We express our sincere gratitude to the coordinators and staff at DESY for their invaluable support of this test beam measurement and for providing an excellent test beam environment.

References

- [1] The ALICE Collaboration, The ALICE experiment at the CERN LHC, *J. Instrum.* 3 (08) (2008) S08002.
- [2] The ALICE Collaboration, The ALICE Experiment - A Journey Through QCD, Tech. Rep., CERN, Geneva, 2022, [arXiv:2211.04384](https://arxiv.org/abs/2211.04384).
- [3] The ALICE Collaboration, Upgrade of the ALICE experiment: Letter of intent, *J. Phys. G: Nucl. Part. Phys.* 41 (8) (2014) 087001.
- [4] The ALICE Collaboration, ALICE upgrades during the LHC Long Shutdown 2, 2023, [arXiv:2302.01238](https://arxiv.org/abs/2302.01238).
- [5] G. Aglieri Rinella, The ALPIDE pixel sensor chip for the upgrade of the ALICE inner tracking system, *Nucl. Instrum. Methods Phys. Res. A* 845 (2017) 583–587.
- [6] L. Musa, Letter of Intent for an ALICE ITS Upgrade in LS3, Tech. Rep., CERN, Geneva, 2019.
- [7] The ALICE collaboration, Technical Design Report for the ALICE Inner Tracking System 3 - ITS3 ; A Bent Wafer-Scale Monolithic Pixel Detector, Tech. Rep., CERN, Geneva, 2024.
- [8] M. Mager, for the ALICE collaboration, The future of bent MAPS, full-wafer (stitched) design: Status and challenges, *Nucl. Instrum. Methods Phys. Res. A* HSTD13 (2024).
- [9] The ALICE Collaboration, Upgrade of the ALICE Inner Tracking System during LS3: study of physics performance, 2023, ALICE-PUBLIC-2023-002.
- [10] W. Snoeys, et al., Optimization of a 65 nm CMOS imaging process for monolithic CMOS sensors for high energy physics, *PoS Pixel2022* (2023) 083.
- [11] F. Piro, et al., A compact front-end circuit for a monolithic sensor in a 65-nm CMOS imaging technology, *IEEE Trans. Nucl. Sci.* 70 (9) (2023) 2191–2200.
- [12] G. Aglieri Rinella, et al., Digital pixel test structures implemented in a 65 nm CMOS process, *Nucl. Instrum. Methods Phys. Res. A* 1056 (2023) 168589.
- [13] P.V. Leitaó, et al., Development of a stitched monolithic pixel sensor prototype (MOSS chip) towards the ITS3 upgrade of the ALICE inner tracking system, *J. Instrum.* 18 (01) (2023) C01044.
- [14] M.J. Rossewij, et al., Electrical/piezoresistive effects in bent Alpidе MAPS, 2024, [arXiv:2403.12298](https://arxiv.org/abs/2403.12298).
- [15] A. Amatriain, et al., Development of an air cooling system with low material budget for high-energy physics applications, *Appl. Therm. Eng.* 236 (2024) 121699.