Conceptual design of a high reactive-power ferroelectric fast reactive tuner

Ilan Ben-Zvi,[1,*] Graeme Burt,[2] Alejandro Castilla,[3] Alick Macpherson,[4,†] and Nicholas Shipman[4]

[1]*Physics and Astronomy Department, Stony Brook University, New York, USA*
[2]*Engineering Department, Lancaster University, LA1 4YW, United Kingdom*
[3]*SRF S&T, Accelerator Operations Division, TJNAF, Newport News, Virginia, USA*
[4]*CERN, CH-1211 Geneva, Switzerland*

(Received 8 December 2023; accepted 12 April 2024; published 10 May 2024)

We present a novel design of a ferroelectric fast reactive tuner (FE-FRT) capable of modulating mega-VAR reactive power on a submicrosecond timescale. The high reactive power capability of our design extends the range of applications of reactive tuners to numerous applications. We present a detailed analytical model of the performance of a megawatt-class reactive power device and benchmark it against finite-element method eigenmode and frequency domain electromagnetic simulations. We introduce new features, including an annulus design for the ferroelectric capacitors and capacitive window coupling to the cavity. We consider thermal design issues and nonlinear effects in the ferroelectric. The model covers several configurations, allowing control of the frequency of superconducting and normal-conducting cavities in a variety of applications and frequencies. We calculate that the FE-FRT designed should be capable of handling around 0.45 MVAR of reactive power with around 3 kW of resistive losses, providing a frequency tuning range of 8 kHz in an example of 400 MHz cavity geometry.

DOI: 10.1103/PhysRevAccelBeams.27.052001

I. INTRODUCTION

Fast tuning of rf cavities at high power is an enabling technology in particle accelerators. Uses are abundant and include avoidance of beam resonances during acceleration in storage ring cavities; compensation of transient beam loading; and correction of microphonics in superconducting cavities.

Reactive tuning is the controlled change of the resonant frequency of a cavity by coupling the cavity to a variable reactance, and the performance is characterized by the amount of reactive power that the tuner can manage, the speed of tuning, and the resultant power dissipation in the tuner. In the most elementary example, the variable reactance may be a variable capacitor coupled to the cavity. Under practical conditions, the frequency of the cavity depends linearly on the variable capacitance. There is a long history of the development of reactive tuning with the voltage-controlled reactance [1] developed at Argonne National Laboratory for the control of acoustic frequency noise of superconducting resonators in a linac being the highest reactive power tuner example to date. That device, using PIN diodes, operated as a two-state device and achieved a peak reactive power of 20 kVAR with a 70-W power dissipation in the diodes. However, the introduction of ferroelectric materials has provided a fast, low loss [2] continuously variable reactance alternative for such tuning applications. This led to the development of microwave active pulse compressor, using the ferroelectric element as a fast switch [3], then a fast phase-shifter and attenuator to the rf input of a 1.3 GHz cavity [4], leading to a coaxial phase shifter with high peak power, but low average power capability at L band [5]. To the best of our knowledge, there is no previous record of a tuner design based on the ferroelectric material providing the details presented in this manuscript, such as the exact tuning range and power loss, detailed analytic expressions and comparison to finite-element simulations. The first demonstration of frequency control of a cavity using a ferroelectric tuner fast reactive tuner (FE-FRT) was made using a coaxial tuner geometry coupled to a superconducting 400 MHz cavity in 2019 at CERN [6], and more recent tests have measured the speed of the cavity frequency shift to be <600 ns [7], much faster than the cavity time constant. In fact, the tuner response time, as reported, is believed to be limited only by the speed of the external powering circuit and could be further reduced, as the response time of bulk ferroelectric like the material used in the prototype FE-FRT has been measured at less than 30 ns [8].

The objective of this paper is to present a new conceptual design and evaluate the performance of an FE-FRT,

*Ilan.Ben-Zvi@StonyBrook.edu
†alick.macpherson@cern.ch

representing a new class of fast tuners, capable of about 450 kVAR.

The FE-FRT design described here is a coaxial structure containing multiple parallel-plate capacitors whose dielectric material is a ferroelectric ceramic. The FE-FRT is coupled to the cavity via a short, coaxial transmission line and to affect the tuning, the permittivity of the ferroelectric is modulated by a voltage signal (bias) applied to the electrodes on either side of the ferroelectric ceramics. Notable features of this design include: (i) The use of thin wafers of ferroelectric material, thus providing high electric field (and thus large permittivity modulation) for a given bias voltage. Thin wafers also result in good thermal conductivity through the wafer. (ii) Employing a stack geometry where multiple capacitors made of wafers and spacers are connected in series. The spacers provide the thermal and electrical contact to the wafers and allow for the impedance of the stack to be optimized. (iii) A particular matching geometry for the tuner circuit to achieve the best coupling to the cavity.

The salient feature of the design presented here is the ability to handle very high average reactive power. Besides increasing the cooling power having multiple wafers reduces thickness and therefore bias voltage. But once you have multiple wafers, you anyway need to bias them. Therefore, there is a metallic connection made from each electrode and putting a channel for the cooling fluid inside the metallic connection shields the coolant from the rf field.

The layout of this paper is as follows: In Sec. II, we establish an analytic model where we derive the impedance of the tuner for various tuner configurations and investigate both the effect of coupling this impedance to the cavity, and the permittivity dependent nonlinear generation of harmonic power; in Sec. III, we address the physical realization of the new ferroelectric tuner concept; and in Sec. IV, we provide a comparison of the analytic model to numerical simulations, and we summarize in Sec. V.

The central thesis of this manuscript is a detailed theory, backed up by numerical simulations of a high average power fast ferroelectric tuner, showing the feasibility of such a device. The detailed implementation of such a tuner clearly draws upon various engineering disciplines. For example, a tuner for a superconducting cavity assumes engineering details of the power handling and cooling practices of high-power couplers, as an example [9]; the detailed engineering of these aspects is considered beyond the scope of this manuscript and is deferred for future contributions.

II. ANALYTIC MODEL

It is useful to develop an analytic circuit model of the tuner to get an intuitive understanding of its behavior and performance and to evaluate the frequency tuning range, the power loss in the tuner and its components, as well as several other properties. While such a model may be less accurate than a detailed numerical finite-element electromagnetic simulation, it offers several advantages, primarily its simplicity and speed which allows a large number of design choices and parameter combinations to be evaluated and provides intuitive insights into how different aspects of tuner behavior are impacted by different parameters. Thus, the analytic model developed has been fully utilized to guide the design of the tuner and provide both a starting point and cross checks for more detailed numerical simulation of the tuner response.

A. Equivalent circuit

Given that the tuner design is dependent on the application use case, the equivalent circuit for three typical terminated tuner stub designs are considered and shown in Fig. 1. They all have in common a coupler port to the cavity, a section containing thin ferroelectric capacitors connected in series, and a transmission line of a given length connecting the cavity port to the ferroelectric section.

Design A is the simplest with a string of ferroelectric capacitors connected in series (four capacitors shown as an arbitrary example), the permittivity of the capacitors is modulated by a bias voltage, with bias connections introduced between the series capacitors (these connections are not modeled in the analytic model). The capacitors' connection in series, which we introduced in [10], offers several advantages over a single capacitor configuration, in that it has a larger power handling capacity (due to the larger surface area) and a higher reactance (due to the series

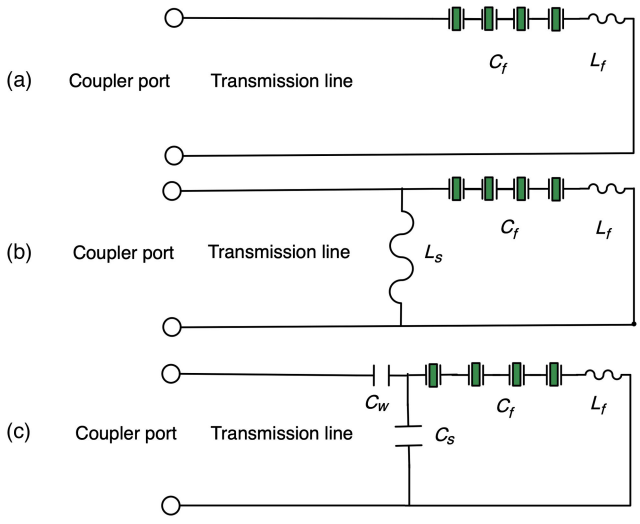

FIG. 1. Circuit diagrams for three potential configurations of a tuner using ferroelectric loaded capacitors. The number of ferroelectric capacitors connected in series is N_w, set at four in this figure. Configuration (A) is a proportional, resonant, or nonresonant circuit. Configuration (B) employs a resonant circuit for increased reactance. Configuration (C) shows a resonant circuit for high-frequency applications and in addition a capacitive coupling to the transmission line through a window.

connection) to match the impedance of the coupler port. It also allows for a lower voltage bias power supply, since biaswise the wafers are in parallel.

Also included in this terminated ferroelectric capacitor stack is a self-inductance L_f depicted as a single element, but in the precise construction of the stack, the inductance is distributed over the conducting spacers and the ferroelectric wafers. This inductance is intrinsic to the ferroelectric stack and may dominate the reactance at high frequencies. Furthermore, the spacers, which are also used to cool the ferroelectric wafers introduce losses, and the attributed impedance of the ferroelectric capacitors must take into account the rf currents flowing across the interface surfaces between the spacers and the ferroelectric wafer (see Sec. II C).

Design A of Fig. 1 is intended to operate in a nonresonant state. This configuration allows the reactance and therefore the frequency to be continually varied and a typical application could be as a microphonics suppression system for superconducting linac cavities. However, due to its nonresonant design, the performance is inferior compared to the following two schemes.

For a more performant tuning design suitable for either proportional control or two states switching, a resonant tuner design can be considered, shown as design B in Fig. 1. Here, the ferroelectric capacitor stack forms a resonator with the inductance L_s, with the two states of the ferroelectric capacitor (no bias or full bias) set such that the resulting reactances that are equal in magnitude but opposite in sign at the coupler port. In this configuration, the resonant frequency of the tuner in the full bias is above the frequency of the tuned cavity, which we will denote as state 1, and the zero-bias mode of the tuner circuit lies below the frequency of the cavity (denoted as state 2). Such a twin mode tuner is useful for applications that require a fast jump in the frequency of the cavity but can also be used as a proportional tuner in superconducting cavities, and this design has previously been introduced in [10].

Our preferred tuner design is one that operates in a continuous proportional tuning mode, and for this, the combined tuner and transmission line circuit are designed such that the reactance at the cavity port, as a function of permittivity, traces a line between the end states which passes through the Smith chart short. To achieve this condition, the impedance of the tuner can be transformed by controlling the length of the connecting transmission line.

To further enhance the expected performance of the tuner, in a third design (design C of Fig. 1), we introduce two additional capacitors (nonferroelectric). Specifically, the capacitor C_s is useful at high frequencies, when the reactance of the inductor L_f exceeds the reactance of the capacitor C_f at the operating frequency of the cavity and is used to ensure that the tuner end-state resonances are symmetric around the nominal cavity frequency. C_w is introduced in series with the transmission line and serves two functions: to control the reactance of the tuner to approximately match it to the characteristic impedance of the transmission line and to serve as a window coupler, isolating the cavity vacuum from the tuner volume. The latter is seen as valuable for protecting the vacuum of the accelerator's cavities.

Given the properties of a particular ferroelectric material, the equivalent circuits of Fig. 1 provide from four to six free parameters depending on design: C_f, L_f, N_W, C_S (or alternately L_S), C_W, and the length of the transmission line l. Assuming that C_f and N_W are set and L_f controlled by adjusting the length of the spacer electrodes inserted between the ferroelectric wafers, this reduces the model to three key parameters (C_S, C_W, and l) allowing the tuner design requirements to be matched. Considerations for the design include the central frequency, tuning range, power dissipated in the tuner over the tuning range, and the matching of the tuner to its coupling port and can be assessed within the framework of the equivalent circuit model.

As an example, for the CERN-PS 80 MHz cavity tuner configuration described in [10], a resonant circuit design of type design B was considered, comprising the capacitor stack, a "stub," inductive short of inductance L_s, and a tuner configuration capable of high-power reactive tuning was identified.

B. Impedance of the tuner

Significant insight into the performance of the tuner can be gained by calculating the tuner impedance as seen at the point the transmission line section connects to the cavity's coupling port. Further, analytic modeling of all these configurations is easily implemented in standard equivalent circuit modeling packages, and in this paper, both Python and Maple [11] have been used and have shown very good agreement with detailed numerical finite-element simulation using dedicated electromagnetic simulation software. In this subsection, we derive the analytic expression of the impedance of the tuner as measured at the cavity port. Coupling this impedance to the cavity will be carried out in Sec. II D.

To evaluate the tuner impedance Z presented to the cavity coupler port, the complex impedance can be represented as a transmission line of characteristic impedance Z_0, of length l and terminated by a load impedance Z_L. Such an impedance is given by

$$Z \equiv R + jX = Z_0 \frac{Z_L + Z_0 \tanh(\gamma l)}{Z_0 + Z_L \tanh(\gamma l)}, \tag{1}$$

where $\gamma = \alpha + j\beta$ is the complex propagation coefficient, α the transmission line attenuation constant, and $\beta = \omega/c$ the phase advance constant. For a coaxial transmission line of

inner radius a, outer radius b, and surface resistivity R_s, the attenuation constant is

$$\alpha = \frac{R_s}{2\eta \log(\frac{b}{a})}\left(\frac{1}{a}+\frac{1}{b}\right). \tag{2}$$

With $\eta = \sqrt{\mu_0/\epsilon_0} = 376.7\ \Omega$, the impedance of vacuum. Also, the characteristic impedance Z_0 of a lossy line is a complex number and is given as

$$Z_0 = \frac{\eta}{2\pi}\log\left(\frac{b}{a}\right)\left(1 - j\frac{\alpha}{\beta}\right). \tag{3}$$

In this description, the load impedance Z_L is the impedance at the point the main body of the tuner connects to the transmission line. To evaluate these designs of Fig. 1, the impedance of the inductors in the tuner schematics is treated as short transmission line sections, so to include resistive losses, while losses in the ferroelectric material are incorporated via the loss tangent $\tan(\delta) \sim \delta$, for the ferroelectric material that typically has $\tan(\delta) \approx 1 \times 10^{-3}$. We neglect losses in the fixed capacitors (such as C_S and C_W).

Table I gives expressions for Z and Z_L for the three different designs shown in Fig. 1. We use Z_f for the impedance of the ferroelectric capacitor. While one would normally expect to have $Z_f = 1/(j\omega C_f(1-j\delta))$, this expression does not account correctly for the current transition between the spacer and ferroelectric wafer, and the precise form of Z_f will be addressed in the next subsection. Z_L is transformed to the tuner impedance at the coupling port using Eq. (1).

Given the tuner plus transmission line impedances of Table I, it is straightforward to generate equivalent circuit models and evaluate the analytic response for both the real and imaginary parts of Z. Further, for the two permittivity end states of the tuner, where C_f takes values of C_{f1} or C_{f2}, the impedance at the cavity coupler port is denoted as Z_1 and Z_2, respectively. The inductance L_f arises from the electrodes on either side of each wafer, which are actually short sections of transmission lines and are modeled as such. The inductance L_f should not be confused with the inductance that arises from the current flowing along the surface of the ferroelectric wafer-electrode boundary, which we fold into the definition of C_f and treat in Sec. II C. For design B, there is also the inductance L_s which appears in the definition of Z_L, and for simplicity L_s is also modeled as a short section of lossy transmission line. However, depending on the physical realization of a particular tuner design, L_s may or may not manifest a physical transmission line.

TABLE I. Impedances for the three equivalent circuit designs: Z_L is the "tuner load impedance" measured at the point the transmission line joins the main body of the FE-FRT, and Z is the "impedance at the coupling port," which is the impedance of the complete tuner, as seen at the cavity port.

Tuner design	Tuner load impedance Z_L	Impedance at the coupling port Z
Design A	$Z_f + j\omega L_f$	$Z_0\frac{Z_f+j\omega L_f+Z_0\tanh(\gamma l)}{Z_0+(Z_f+j\omega L_f)\tanh(\gamma l)}$
Design B	$\frac{j\omega L_s(Z_f+j\omega L_f)}{j\omega L_s+Z_f+j\omega L_f}$	$\frac{\frac{j\omega L_s(Z_f+j\omega L_f)}{j\omega L_s+Z_f+j\omega L_f}+Z_0\tanh(\gamma l)}{Z_0+\frac{j\omega L_c(Z_f+j\omega L_f)}{j\omega L_c+Z_f+j\omega L_f}\tanh(\gamma l)}$
Design C	$\frac{\frac{1}{j\omega C_s}(Z_f+j\omega L_f)}{\frac{1}{j\omega C_s}+Z_f+j\omega L_f}+\frac{1}{j\omega C_w}$	$Z_0\frac{\frac{\frac{1}{j\omega C_s}(Z_f+j\omega L_f)}{\frac{1}{j\omega C_s}+Z_f+j\omega L_f}+\frac{1}{j\omega C_w}+Z_0\tanh(\gamma l)}{Z_0+\left(\frac{\frac{1}{j\omega C_s}(Z_f+j\omega L_f)}{\frac{1}{j\omega C_s}+Z_f+j\omega L_f}+\frac{1}{j\omega C_w}\right)\tanh(\gamma l)}$

C. Ferroelectric capacitor: Impedance details

To correctly model the impedance of the ferroelectric capacitors, we found it was necessary to consider the inductive contribution of the currents that flow along the interface between the ferroelectric wafers and the electrode surfaces. This in turn leads us to the realization that a performance increase is achieved by using a ferroelectic wafer geometry in the form of an annulus rather than a simple disk. This precise modeling of the spacer-ferroelectric transition is important in view of the large dielectric constant of the ferroelectric.

In the coaxial section of the FE-FRT, rf current flows on the outside surface of the inner conductor. When it reaches the ferroelectric, the rf current flows radially along the interface of the spacer, inducing a displacement current across the ferroelectric wafer. This current pattern clearly introduces resistive loss and, particularly at high frequencies, we must also consider the associated inductive reactance.

We consider the interfaces between the electrodes and ferroelectric as a collection of nested touching annuli of a variable radius r and infinitesimal radial thickness dr, where r can take any value between the inner and outer radii r_1 and r_2. This is shown schematically in Fig. 2.

For a pair of annuli at a given radius r facing each other on either side of the ferroelectric ring, separated by the ferroelectric of width g_0, the resistance, inductance, and capacitance per unit of radius are given by

$$R' = \frac{R_s}{\pi}\frac{1}{r} \qquad L' = \frac{g_0\mu_0}{2\pi}\frac{1}{r} \qquad C' = \frac{2\pi\epsilon_0\epsilon(1-j\delta)r}{g_0}, \tag{4}$$

where R_s is the surface resistance of the metal walls, and the resistance counts surfaces on both sides of the annulus capacitor. The series of connected annuli is then characterized as a lumped element radial transmission line with the lumped elements parameters given above. The complex propagation constant and characteristic impedance can be calculated as

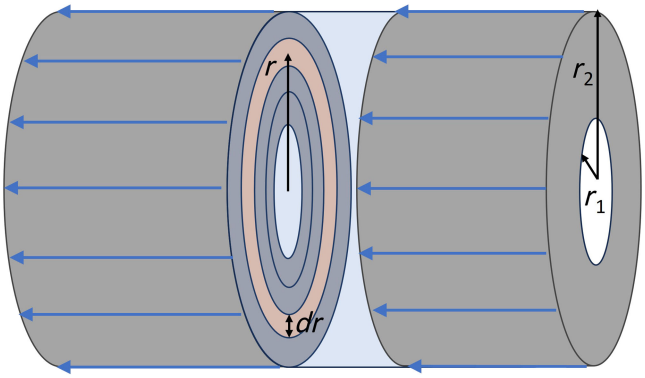

FIG. 2. Detail of the model used to solve the impedance of the ferroelectric capacitor. Blue arrows represent the surface current flowing longitudinally on the surface of the spacers, encountering the capacitive gap, treated as a short section of a radial transmission line extending from r_2 to r_1. This transmission line comprises the two radial surfaces of the spacers and it is loaded by the ferroelectric wafer. The colored annulus of radius r and width dr is used in the integration.

$$\gamma = \sqrt{(R' + j\omega L')j\omega C'},$$
$$Z_0(r) = \sqrt{(R' + j\omega L')/(j\omega C')} = \frac{\zeta}{r},$$
$$\zeta \equiv \sqrt{\frac{\frac{R_s}{\pi} + j\omega\frac{g_0\mu_0}{2\pi}}{j\omega\frac{2\pi\epsilon_0\epsilon(1-j\delta)}{g_0}}}. \tag{5}$$

Note that the propagation constant is independent of the radius r while the characteristic impedance of the line is inversely proportional to the radius.

To calculate the impedance Z_f (r_2) seen between the two spacers, at radius r_2, the geometry is represented by a radial transmission line of length $r_2 - r_1$, with the line terminated at r_1 by a capacitive load approximated by a ferroelectric-free circular capacitor of radius r_1 of impedance

$$Z_f(r_1) = \frac{g_0}{j\omega\epsilon_0\pi r_1^2}. \tag{6}$$

The result of the integration is insensitive of the value of the "terminating impedance" $Z_f(r_1)$ as long as it is a large reactance in comparison with $Z_0(r_1)$. This impedance $Z_f(r_1)$ is then propagated from the initial point at radius r_1 through increasing radius annuli all the way to the final radius of the capacitor r_2. To do this, we consider an infinitesimal annulus of width dr and write the impedance at $r + dr$ using again the transmission line equation:

$$Z_f(r+dr) = Z_0(r+dr)\frac{Z_f(r) + Z_0(r+dr)\tanh(\gamma dr)}{Z_0(r+dr) + Z_f(r)\tanh(\gamma dr)}. \tag{7}$$

Then if $Z_f'(r)$ is the derivative of $Z_f(r)$, the differential equation for $Z_f(r)$ is

$$Z_f'(r) = -b^2 r(Z_f(r))^2 + \frac{c^2}{r}, \tag{8}$$

with $b = \sqrt{\gamma/\zeta}$ and $c = \sqrt{\gamma\zeta}$.

Equation (8) is known as Riccati's equation and has a closed form solution, but this equation can also be easily integrated numerically and fitted for fast evaluation of the impedance of the capacitors including the transition effects. This allows for numerical evaluation of Z_f used to assess the expressions of Table I.

D. Coupling the tuner to the cavity

With the detailed expression of the tuner impedance Z established, the frequency tuning obtained from coupling this tuner impedance to a resonant cavity can be evaluated. Here the cavity is assumed to have a dedicated tuner port with a given external Q_e. In addition, once the coupling is defined, additional tuner performance parameters such as the reactive and dissipative power in the transmission line and ferroelectric ceramics can be assessed.

The cavity tuner is represented by the equivalent circuit diagram shown in Fig. 3. The cavity, which comprises the inductance L_c, capacitance C_c, and resistance R_c is coupled to FE-FRT tuner Z through a port, represented here by the coupling capacitor C_k: The fundamental power coupling port is not shown. The natural (no tuner) resonant frequency of the cavity is ω_0, and the frequency of the tuned cavity (when the tuner reactance Z is included) is ω. For this equivalent circuit model of the cavity, the external quality factor of the cavity's port is given by the cavity's shunt impedance (accelerator convention) $R_{sh}/Q = 1/\omega C_c$, as given in Eq. (9). In addition, Z_0 is the characteristic impedance of the transmission line connected to the port, and the coupling port strength is set by a transformer turn ratio n:

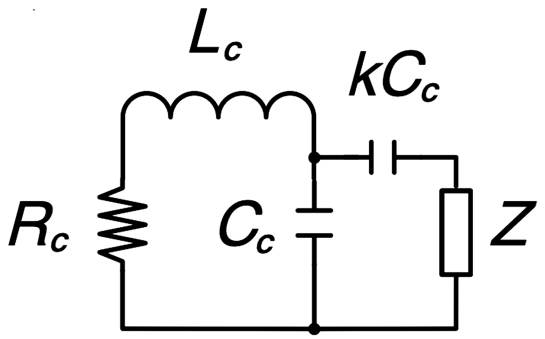

FIG. 3. Equivalent circuit diagram of a cavity with external capacitive coupling. The tuner's impedance Z is coupled to the cavity circuit, represented by $R_c - L_c - C_c$ through the coupling capacitor kC_c.

$$Q_e = \frac{R_{sh}/Q}{Z_0 n^2} \qquad Q \equiv \frac{\omega L_c}{R_c},$$
$$\omega_0 \equiv \frac{1}{\sqrt{L_c C_c}} \qquad \Delta\omega \equiv \omega - \omega_0 \qquad k \equiv \frac{C_k}{C_c}. \quad (9)$$

As seen from Fig. 3, the impedance Z_c measured across the cavity's capacitor C_c is that of a capacitor C_c in parallel with the series combination of the coupling capacitor C_k and the load impedance of the FE-FRT tuner $Z = R + jX$:

$$Z_c = \frac{\frac{1}{j\omega C_c}\left(\frac{1}{j\omega k C_c} + R + jX\right)}{\frac{1}{j\omega C_c} + \frac{1}{j\omega k C_c} + R + jX}. \quad (10)$$

As a cross check of this equation, we can see that as the coupling strength k tends to 0, Z_c reduces to the impedance expected for an uncoupled cavity's capacitor ($k \to 0 \Rightarrow Z_c \to 1/(j\omega C_c)$.

Requiring the tuner load impedance to be purely real (i.e., $X = 0$), the impedance of the effective cavity capacitance reduces to

$$Z_c = \frac{1}{j\omega C_c}\frac{1 + j\omega C_c R k}{1 + k + j\omega C_c R k}. \quad (11)$$

By assuming k is small ($k \ll 1$), that $Q_e \gg 1$, and $Z_0 \simeq R$ then Z_c is simplified such that the resistive component is represented by the load resistance R transformed into the cavity's circuit with the square of the coupling strength, namely:

$$\Re(Z_c) = \frac{Rk^2}{\omega^2 C_c^2 R^2 k^2 + (1+k)^2}$$
$$\approx Rk^2 \quad \text{for } k \ll 1, \qquad Q_e \gg 1. \quad (12)$$

Further, for this real load impedance ($R = Z_0$) matched to the characteristic impedance of the port, the definition of Q_e identifies k as the transformer turn ratio n:

$$Q_e \equiv \frac{\omega L_c}{\Re(Z_c)} = \frac{R_{sh}/Q}{Z_0 k^2}. \quad (13)$$

To assess the reactive tuning of the cavity by the tuner circuit, we can again use Eq. (10), and neglecting dissipation by the real part of Z, consider the purely imaginary part of the load impedance, i.e., $Z = jX$. This gives

$$\Im(Z_c) = \frac{X - \frac{1}{\omega k C_c}}{1 + \frac{1}{k} - X\omega C_c} = -\frac{1}{\omega C_c}\frac{X\omega k C_c - 1}{X\omega k C_c - k - 1}, \quad (14)$$

where we have explicitly factored out the reactance of the bare cavity's capacitor, $-1/(\omega C_c)$. The tuning induced by the coupled load reactance X modifies the impedance of the cavity's capacitor and changes the frequency. If we take the ratio of the reactance of the system with and without the coupled load reactance, in the limit where the coupling capacitance is small compared to the cavity capacitance, we obtain the ratio of the frequency with and without the coupled load reactance:

$$\left(\frac{\omega}{\omega_0}\right)^2 \approx 1 - 2\frac{\Delta\omega}{\omega} = \frac{X\omega k C_c - 1}{X\omega k C_c - k - 1}. \quad (15)$$

Leading to

$$\frac{\Delta\omega}{\omega} = \frac{-1}{2(X\omega C_c - 1 - \frac{1}{k})}. \quad (16)$$

Here it is noted that the coupling port changes the frequency of the cavity by a small amount even if the external reactive load X is zero, as expected, due to the presence of the coupling capacitor. For the two-state tuning due to the different bias states of the ferroelectric, the state-to-state frequency change can be obtained from Eq. (16):

$$\Delta\omega_{12} \equiv \Delta\omega_2 - \Delta\omega_1$$
$$= \frac{-\omega}{2}\left[\frac{1}{X_2\omega C_c - 1 - \frac{1}{k}} - \frac{1}{X_1\omega C_c - 1 - \frac{1}{k}}\right]$$
$$= \frac{\omega}{2}\frac{X_2 - X_1}{(R_{sh}/Q)}k^2 \quad \text{for } k \ll 1, \qquad Q_e \gg 1$$
$$= \frac{\omega}{2Q_e}\frac{X_2 - X_1}{Z_0}. \quad (17)$$

Here it is also noted that when the tuner's reactance approaches $(R_{sh/Q})/k$, the tuning becomes inversely proportional to the reactance, but such a situation is considered highly unlikely.

Equation (17) conveniently expresses the maximum tuning $\Delta\omega_{12}$ as a function of the maximum reactance change and coupling port parameters.

E. Power flow in the tuner

With the tuner now connected to the cavity, it is now reasonable to assess the power flow from the cavity to the tuner. Given that the peak voltage across the cavity capacitor C_c is V, the peak current into the coupling capacitor and load impedance Z combination is then

$$I = \frac{V}{Z + \frac{1}{j\omega C_c k}}. \quad (18)$$

Since $Z \ll \frac{1}{j\omega C_c k}$, the coupling port acts as a current source, and the voltage across the load Z is given by $V_Z = IZ$, with the power P_Z into the load impedance Z, assuming peak voltages and currents, is

$$P_Z = \frac{1}{2} V_Z I^* = \frac{1}{2}|V|^2 \frac{Z}{|Z + \frac{1}{j\omega C_c k}|^2} = \frac{U}{C_c} \frac{Z}{|Z + \frac{1}{j\omega C_c k}|^2}$$
$$\approx \frac{U}{C_c} \frac{Z}{|1/(\omega C_c k)|^2} = U\omega^2 C_c k^2 Z, \tag{19}$$

where we have substituted the stored energy in the cavity $U = 1/2C_c|V|^2$. Using the equivalent circuit definitions of Eq. (9), P_Z can alternatively be written as

$$P_Z = \frac{U\omega}{Q_e}\frac{Z}{Z_0} = \frac{U\omega}{Q_e Z_0}(R + jX). \tag{20}$$

For the case of cavity tuner applications $X \gg R$ by design, and the power in the tuner is mostly reactive. Indeed, for high-power two-state tuners, it is highly desirable to set the end-state powers equal in magnitude, to reduce the demands on the coupler, and this implies a tuner design constraint of having approximately $X_1 = -X_2$.

To make the connection between the frequency tuning range of the tuner, the cavity stored energy, and reactive power in the tuner, Eqs. (17) and (20) give the known relationship:

$$\Im(\Delta P_{12}) = 2U\Delta\omega_{12}. \tag{21}$$

A characteristic figure of merit (FoM) for the tuner can be defined in terms of the complex power vales of the two end states or equivalently in terms of the tuner impedance values at the two end states:

$$\mathrm{FoM} \equiv \frac{\Im(P_2) - \Im(P_1)}{2\sqrt{\Re(P_1)\Re(P_2)}} = \frac{X_2 - X_1}{2\sqrt{R_1 R_2}}. \tag{22}$$

The FoM is an important characteristic of the tuner, since it describes the ability of the tuner to produce reactive power for tuning a cavity given limits on the either power dissipation in the tuner circuit or power drawn from the cavity. The power dissipated in the tuner is given by the real part $\Re(P_Z)$ from Eq. (20) and is also the power extracted from the cavity, which must be provided by the power amplifier driving the cavity.

To evaluate the power dissipated in the ferroelectric material, within the context of this equivalent circuit model, the surface resistivity of all conductors in the tuner can be set to zero and $\Re(P_Z)$ computed. Similarly, the power dissipation in any component of the tuner can be isolated and computed.

F. Nonlinear effects

We now explore the leading cause of nonlinearity in the FE-FRT device. To change the frequency of a cavity with an FE-FRT, we control the permittivity of the ferroelectric stack by applying a bias electric field E_B. However, as the permittivity is a function of the total electric field $E(t) = E_{\mathrm{rf}}(t) + E_B$, where $E_{\mathrm{rf}}(t)$ is the rf electric field generated by the rf current driving the tuner $I = I_0 \sin \omega t$, the permittivity gains an unwanted time dependence. This mechanism leads to the generation of harmonic power, at a level that depends on both the circuit configuration and the magnitude of the fundamental (mostly reactive) power flowing in the circuit. This effect drains power from the cavity and deposits it at the tuner components, thus it requires consideration.

We will examine only bias state 1 (the maximum bias field and lowest permittivity) as the proportional change in permittivity, and therefore, the harmonic power generated will be greatest here. Also in the case of zero bias (state 2) the permittivity, depending only on the absolute value of the rf field, takes the form of a "full wave rectifier" which reduces the peak variation in permittivity further decreasing the harmonic power generated.

For a given temperature of the ferroelectric, we assume that the relative permittivity $\epsilon[E(t)]$ is only dependent on the magnitude of the total applied electric field and has a linear relationship to it. In reality, the permittivity as a function of the applied electric field is not a perfectly straight line, and the deviation of it from a linear relationship can introduce higher harmonics, which we presently neglect. Thus, in state 1, assuming the peak rf field is smaller than the bias field, it can be expressed as

$$\epsilon(E(t)) = \epsilon_1 - \frac{E_{\mathrm{rf}}(t)}{E_p}, \tag{23}$$

where E_p is an intrinsic property of the ferroelectric material at a given temperature, and ϵ_1 is the permittivity in state 2 in the absence of any rf field.

Note also that ϵ_2, the relative permittivity in state 2 in the absence of rf field, can be related to the maximum bias field, E_B, ϵ_1, and E_p as follows:

$$\epsilon_2 = \epsilon_1 + \frac{E_B}{E_p}. \tag{24}$$

The capacitance C_f of the ferroelectric capacitor stack is proportional to the relative permittivity and thus obtains a time dependence from $E_{\mathrm{rf}}(t)$:

$$C_f(t) = C_{f1} - \frac{\epsilon_0 A}{g E_p} E_{\mathrm{rf}}(t), \tag{25}$$

where ϵ_0 is the permittivity of free space, A is the contact surface area between the ferroelectric and a single electrode, g is the total combined thickness of the serially connected ferroelectric wafers, and C_{f1} is the capacitance in state 1 with no rf field:

$$C_{f1} = \epsilon_0 \epsilon_1 \frac{A}{g}. \tag{26}$$

The displacement current through the capacitor determines the voltage across it:

$$\begin{aligned} I(t) &= I_0 \sin \omega t \\ &= \frac{d}{dt}(C_f V) \\ &= C_{f1}\frac{dV}{dt}(1-4\phi V), \\ \text{where } \phi &\equiv \frac{1}{2gE_p\epsilon_1}, \end{aligned} \tag{27}$$

and we have defined $V(t) = g \times E_{\mathrm{rf}}(t)$ and also dropped the explicit time dependence in $V(t)$ and $C_f(t)$ for clarity.

We rewrite this as an equation for the voltage $V(t)$:

$$\frac{dV}{dt} - 4\phi V\frac{dV}{dt} = \frac{I_0}{C_{f1}}\sin \omega t. \tag{28}$$

This nonhomogeneous differential equation for $V(t)$ has a solution:

$$\phi V(t) = \frac{1}{4}\left(1 - \sqrt{1 + 8\phi\frac{I_0}{\omega C_{f1}}\cos \omega t}\right). \tag{29}$$

We may approximate Eq. (29) by expanding the square root provided that $8\phi\frac{I_0}{\omega C_{f1}} \ll 1$. Substituting in for ϕ, we find this condition implies

$$\frac{4E_{\mathrm{rf}}}{E_p\epsilon_1} \ll 1. \tag{30}$$

Alternatively, using Eq. (24), this can be rewritten in terms of E_b as

$$\frac{4\Delta\epsilon}{\epsilon_1}\frac{E_{\mathrm{rf}}}{E_B} \ll 1, \tag{31}$$

where $\Delta\epsilon = \epsilon_2 - \epsilon_1$.

We now continue assuming that Eq. (31) is well satisfied and Eq. (29) can be well approximated from the first three terms of the expansion (if E_{rf} is high enough that this is not true the nonlinearity becomes worse, and various higher harmonics will be generated) giving

$$V(t) \approx \phi\left(\frac{I_0}{\omega C_{f1}}\right)^2 - \frac{I_0\cos \omega t}{\omega C_{f1}} + \phi\left(\frac{I_0}{\omega C_{f1}}\right)^2\cos 2\omega t. \tag{32}$$

From the second term of Eq. (32), the magnitude of the fundamental voltage V_0 is found to be

$$V_0 = \frac{I_0}{\omega C_{f1}}. \tag{33}$$

Comparing to the third term, we see that the harmonic voltage magnitude V_h can be written as

$$V_h = \phi V_0^2. \tag{34}$$

The harmonic voltage is therefore proportional to the square of the fundamental voltage and inversely proportional to g, E_p, and ϵ_1 (from the definition of ϕ).

Our next objective is to find a method to calculate the power dissipated in the circuit by the harmonic component. The circuit diagram for the harmonic component is identical in layout to that of the tuner's fundamental circuit in Fig. 1. However, there are some significant differences in the value of the variables.

(i) The voltage source of the harmonic is the ferroelectric capacitor stack, not the cavity. (ii) We assume that the harmonic power at the coupler port is unlikely to fall on an HOM mode, and we therefore assume that the harmonic is fully reflected by the cavity. Even if the harmonic frequency were to overlap a (damped) HOM mode, the matching would be very poor and would still result in a very high reflection. (iii) The ferroelectric stack and the stub are not resonant for the harmonic, and the values of the various impedances are changed in accordance with the doubled frequency.

The value of V_0 can be obtained from the analytic model and by evaluating the power in the tuner using Eq. (20). Given V_0, we can then obtain V_h from Eq. (34).

V_h drives current through an impedance Z_h presented by the circuits shown in Fig. 1. The exact expressions for Z_h for each of the circuits shown in Fig. 1 are listed below:

$$\begin{aligned} \text{[A] } Z_h &= \frac{1}{2j\omega C(1-j\delta_2)} \\ &\quad + Z_0[\tanh(\gamma_2 l_f) + \tanh(\gamma_2 l)], \\ \text{[B] } Z_h &= \frac{1}{2j\omega C(1-j\delta_2)} + Z_0\tanh(\gamma_2 l_f) \\ &\quad + Z_0\frac{\tanh(\gamma_2 l_s)}{1+\tanh(\gamma_2 l_s)+\tanh(\gamma_2 l)}, \\ \text{[C] } Z_h &= \frac{1}{2j\omega C(1-j\delta_2)} + Z_0\tanh(\gamma_2 l_f) \\ &\quad + Z_0\frac{(Z_0\tanh(\gamma_2 l) + \frac{1}{2j\omega C_w})\frac{1}{2j\omega C_s}}{Z_0\tanh(\gamma_2 l) + \frac{1}{2J\omega C_w} + \frac{1}{2j\omega C_s}}, \end{aligned} \tag{35}$$

where δ_2 and γ_2 are, respectively, the loss tangent and propagation constant at the harmonic frequency.

The power dissipated by the harmonic generated voltage P_h is derived from harmonic voltage and the real part of this impedance:

$$P_h = \frac{V_h^2}{2\Re(Z_h)}. \tag{36}$$

Fortunately, we find that this effect is negligible in the point design presented in Sec. IV.

III. PHYSICAL REALIZATION

To effect a physical realization of the tuner concept, a number of engineering aspects related to FE-FRTs have to be taken into consideration, in order to match the material properties of the ferroelectric with the use case requirements. In particular, factors such as the number of wafers in the stack of the ferroelectric capacitor, the choice of the tuner circuit and realization of circuit parameters, and the impact of of services such as bias voltage distribution and cooling of the wafers has to be considered. The setting of these considerations is governed by the material properties of the ferroelectric ceramic, and for this paper, the properties of the ferroelectric material used are based on $BaTiO_3/SrTiO_3$-Mg ceramic, as described in [2,12] and [13], which are listed for convenience below: (i) Relative permittivity ϵ (unbiased) of the order of 160 at room temperature. (ii) ϵ tuneability ≈40% by application of an 8 MV/m electric field. (iii) Breakdown electric field 20 MV/m. (iv) ϵ response with increasing temperature: $\epsilon \sim 130$ at 50 °C, with tunability reducing to about ∼36%. (v) Loss tangent: $\tan\delta \approx \delta = 3.4 \times 10^{-4}$ at 80 MHz, room temperature [12]. This δ increases slowly with frequency, reaching $\delta \approx 1.3 \times 10^{-3}$ at 400 MHz and room temperature. However, at 400 MHz and 50 °C, this is reduced to $\delta \approx 9.5 \times 10^{-4}$. (vi) Thermal conductivity: $K = 7.02$ W/m degree Kelvin.

The temperature dependence of the permittivity is noted here as it allows for the option of fine adjustment of the tuner's resonant frequency during operation by exercising control of the device operating temperature.

For any cavity tuner application, it is assumed that the minimum tuning requirements are defined by (i) the cavity's frequency ω, (ii) the stored energy U, and (iii) the required frequency tuning $\Delta\omega$, while additional considerations that impact the design may include the following: (i) switching speed and voltage handling characteristics of the bias supply; (ii) power dissipation limits in the cavity generated by the resistance of the tuner; and (iii) power handling limits at the coupling port between cavity and tuner.

From these constraints, the reactive power required by a tuner to apply a tuning shift of $\Delta\omega$ is $2U\Delta\omega$ as given by Eq. (32), and the tuner's reactance change relates to the tuner's port Q_e through $\Delta\omega_{12} = \frac{\omega}{2Q_e}\frac{X_2 - X_1}{Z_0}$ from Eq. (17). Further, to avoid an undesirably large impedance mismatch in the transmission line, ideally, $X_i \sim Z_0$, but this is not a strict requirement. Still, we conclude that the coupling port should have $Q_e \sim \omega/\Delta\omega$. However, from the point of view of looking toward the cavity, this value of Q_e may be difficult to obtain if it is very small, in which, it may be necessary to increase the reactance of the tuner. Assuming $Q_e \approx \omega/\Delta\omega$ is acceptable, the reactance range of the tuner at the port, $X_2 - X_1 \approx 2Z_0$ is set.

For realistic tuner operation, the design must also take into consideration the total load capacitance and required rise time, as seen by the bias supply. However, while such an analysis is out of the scope of this communication, it is noted that the voltage of the bias supply does determine the individual wafer thickness g_0. As fast switching between different bias states is characterized by both the energy delivered per pulse and the pulse repetition rate, the energy delivered per pulse is proportional to the total capacitance seen by the pulser and the square of the required bias voltage. Assuming the ferroelectric to be driven to the maximum allowed electric field, which, adopting a conservative approach, is set at 8 MV/m for the ferroelectric ceramic under consideration, then a bias voltage of 8 kV implies a the wafer thickness of $g_0 = 1$ mm. Mechanical integrity of the ferroelectric material limits how thin the wafer can be, and for this work, we assume nominal ferroelectric wafer thickness of 1 mm such that the pulsed bias supply is constrained to 8 kV or less. Clearly, the capacitance seen by the pulser dependent on the wafer thickness, but also on the number of wafers in the capacitor stack, and the biasing scheme adopted.

Further, a limit on the power dissipation at the cavity may come from restrictions on power from the rf amplifier driving the cavity, and this would manifest as a lower limit for the figure of merit.

Thermal management is important for stable operation of the tuner. To assess the thermal load, we assume that cooling is provided to both surfaces of each of the ferroelectric wafers through the interwafer spacers of the capacitor stack. The electrical and thermal transition between the wafers and spacers can be provided by metallization of the wafers and brazing the wafers to the spacers. The drawback of this approach is the high surface resistance of the metallization layer and brazing compound that will reduce the figure of merit. Alternately, nanometer-scale polishing of the wafers and spacers, which has been demonstrated in our laboratory, provides good thermal and electrical transitions. At this point, we keep both options. Therefore, the average temperature rise in the ferroelectric material will be given by

$$\Delta T = \frac{gP}{6AKN_w^2} = \frac{g_0 P}{6AKN_w}, \tag{37}$$

where P is the total power dissipated in the ferroelectric volume of stack, and $K = 7.02$ W/m degree K is the thermal conductivity coefficient of the ferroelectric material. By applying cooling to copper interwafer spacers, very efficient heat removal from the ferroelectric wafers can be achieved. This cooling efficiency can be assessed by considering each spacer as a cooling circuit and calculating the temperature increase assuming the following processes:

(i) Increase of the water temperature in the cooling channel due to heat exchange with the spacer. (a) This is a minor effect, which is also related to the coolant flow rate. The coolant flow rate may be limited by the allowed pressure drop across the cooling channel. (ii) A step temperature increase due to turbulent flow heat transfer from the water to the spacer surface. (b) This is one of the two significant processes governing the temperature of the ferroelectric wafer. The coefficient of heat transfer is proportional to the Nusselt number and inverse to the characteristic dimension of the cooling channel. The Nusselt number in turn depends on the Reynolds number, and a high Nusselt number implies a highly turbulent flow which improves the coefficient of heat transfer. (iii) Thermal resistance of the copper in the spacer. (c) With a careful design of the spacer, this is a minor effect. (iv) Thermal resistance of the interface between the copper spacer and the ferroelectric wafer. (d) This effect is minimal for brazed wafer-spacer transitions. If brazing was to be avoided, this thermal resistance must be mitigated by careful polishing of the surfaces in contact, adequate contact pressure, and application of heat transfer enhancing grease. (v) The increase in the average temperature of the wafer due to rf heating, as discussed above.

Further, the cooling lines must include inductive elements or notch filters to avoid shorting the rf voltage across connected electrodes in the capacitor stack. In this way, by subdividing the capacitor to N_w units, the wafers are in parallel for the bias circuit, and the required bias voltage reduced by a factor of N_w, while the cooling capacity is increased by a factor of N_w. Cooling issues can be critical for some applications, yet increasing the number of wafers may be only a limited solution, as large N_w increases the complexity of the device. Certainly the choice in number of wafers should be carefully considered, as the ferroelectric material can have a permittivity with non-negligible temperature dependence, and as such, feedback control of the spacers' temperature may be required.

As an example of the construction of a high-power FE-FRT, Fig. 4 shows a four-wafer design that represent an in-series capacitance stack to the tuner rf and a in-parallel stack to the bias circuit. This realization is one of the configurations to be discussed in following subsections. A high-power reactive tuner can be in service of a room-temperature cavity or a superconducting cavity. In either case, the area above the dielectric window E is under vacuum. In the cryogenic case, the complete tuner is in the cryostat vacuum system, and a temperature gradient is maintained along the outer conductor of the transmission line leading to the cavity. In this case, as is the practice in high-power couplers, the outer conductor of the transmission line would be a thin-wall stainless steel tube with a thin layer of copper on the inside surface.

Cooling lines from the spacers exit the unit through holes at the top, clearing the holes without shorting to the copper top plate. The lines are made of a conducting material but include a tubular ceramic feedthrough, such that the coolant flows through the feedthrough, but the rf voltage and bias voltage remain isolated. A normal conducting (low Q) notch filter connects the lines either to the bias voltage supply line or to ground. The purpose of the notch filters is to isolate the rf but pass the bias waveform, which is at a much lower speed then the rf period. The notch filters are tuned during initial assembly to the cavity's rf frequency, but due to the low Q, the frequency of the notch does not have to be retuned.

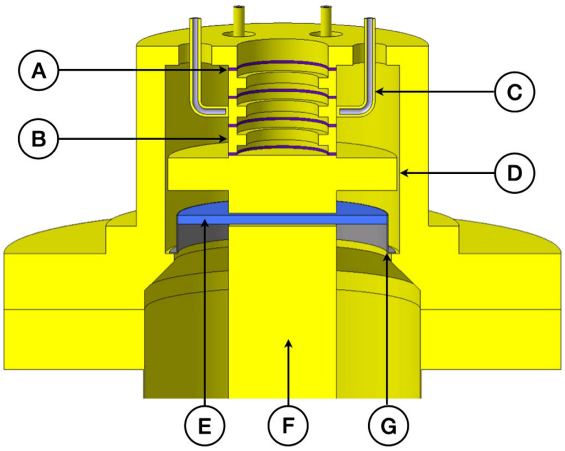

FIG. 4. Model of a four-wafers ferroelectric tuner in configuration C. (A) Ferroelectric wafer. (B) Spacer. (C) Cooling line. (D) Series capacitor gap. (E) Dielectric window. (F) Inner conductor of transmission line. (G) Window support, part of the vacuum enclosure. The copper spacers between the wafers have channels for refrigerant flow. The refrigerant lines also connect the bias voltage but include rf isolation against shorting the rf voltage (not shown). The dielectric of the window capacitor is shown in blue. Yellow color represents copper parts.

A. Configuration (A)

In configuration (A), we have a simple capacitor stack. We also assume that the transmission line is much shorter than the wavelength of operation, and thus may be neglected. With $Q_e \sim \omega/\Delta\omega$, we use Eq. (19) to get $X_2 - X_1 = 2Z_0$. With $X_i = 1/(\omega C_{fi})$, $C_{fi} = \epsilon_0\epsilon_i A/g$, the thickness and surface area of an individual ferroelectric wafer are given as $g_0 = g/N_w$ and A, respectively, and with N_w as the number of wafers in the stack, we obtain the relation

$$\frac{A}{N_w} = \frac{g_0}{2Z_0\omega\epsilon_0}\frac{\epsilon_2 - \epsilon_1}{\epsilon_1\epsilon_2}. \tag{38}$$

The bias electric field required to change the relative permittivity from the room-temperature values $\epsilon_2 = 160$ to $\epsilon_1 = 114$ is 8 MV/m. This bias range gives $(\epsilon_2 - \epsilon_1)/(\epsilon_1\epsilon_2) \approx 0.0025$ and for a wafer thickness of $g_0 \sim 1$ mm $\mathrm{A/N_w}$ is determined. Here it is noted that the ferroelectric

wafer's thickness g_0 is limited from below by machining issues, but a small thickness reduces the bias voltage, and a 1 mm thickness is physically feasible. Now, applying this to Eq. (37), we see that for a given choice of the wafer area A, we get $\Delta T \propto PN_w^{-3}$. For a high-power device, we may want to limit the temperature rise, leading to a larger value of the number of wafers.

Another design consideration is the capacitive load of the bias supply, which becomes important at a very high modulation frequency, as the capacitance seen by the bias supply is $C_B \propto N_w^2$. The main limitation of scheme (A) of Fig. 1 is the small number of free parameters, leading to limitations in the figure of merit. However, in this configuration, equating $|X_2| = |X_1|$ can be done by choosing a particular length of the transmission line.

B. Configuration (B)

In order to extend the tuner performance range, a coupled resonance design can be considered, with the circuit schematic as per Fig. 1(b), with the tuner employing a parallel resonant circuit comprising C_f, L_f, and L_s. The tuner's circuit is arranged to resonate at the cavity's frequency for a midrange permittivity ϵ_r, where $\epsilon_r = \sqrt{\epsilon_1 \epsilon_2}$. In this configuration, the length of the transmission line l and the inductance L_s are free parameters that conveniently allow for the adjustment of the absolute value of $|X_1| = |X_2|$ and choice of Q_e of the cavity's port.

C. Configuration (C)

As a further extension on the resonant tuner design, configuration (C) [Fig. 1(c)] adds two extra features beyond configuration (B). The first is the replacement of the stub inductor L_s by a capacitor C_s in series with the ferroelectric capacitor and is necessary at high frequencies where the stack's inductance dominates, $\omega L_f \geq 1/(\omega C_f)$. The second is the introduction of a "capacitive window coupling," C_w between the tuner and the coupling port. The addition of this window allows both a physical barrier between cavity and tuner volumes that protects the cavity's vacuum from possible contamination, as well as simplifying installation and removal of the tuner from the cavity. Additionally, this provides another free parameter for the optimization of the tuner's circuit.

In terms of physical realization of a tuner unit, configuration C offers a number of advantages of over both configurations A and B [10]. As an indicative summary, the following benefits are noted: (i) For a given value of the ferroelectric capacitor, the modulation high voltage is inversely proportional to the number of wafers. (ii) A high FoM and excellent heat removal can be achieved by stacking multiple wafers. (iii) There is no bias high voltage on the transmission line or coupler. (iv) The ferroelectric material consists of flat wafer plates, easily manufactured with precision to achieve good electric and thermal contacts. (v) Cooling the ferroelectric is simple and independent of the heat dissipated in the transmission line, allowing a very high-power level to be achieved.

IV. NUMERICAL SIMULATIONS

To confirm the design choices detailed above, a example realization of an FE-FRT design is considered and a comparison of the analytic model with a full electromagnetic simulation of rf performance using finite-element numerical methods. For this comparison, a nominal design for a particularly challenging application of an FE-FRT is considered; namely, a high reactive power of about half a mega-VAR at 400 MHz, currently under construction at CERN, and its expected performance calculated both by an analytic model and finite-element numerical methods.

The example we provide is based on configuration C as shown in Fig. 4 and has four wafers in series. Each ferroelectric wafer is a hollow annulus, 0.9 mm thick, with an inner radius of 1.65 cm and outer radius of 1.96 cm. The interwafer spacers are 0.95 cm long. We use a bias voltage of 7.2 kV for state 1 and no bias at state 2 of the ferroelectric wafers.

We can estimate material parameters for the ferroelectric using data from Euclid Techlab Inc., the supplier of the ferroelectric material [2,12] and [13]. For $E_B \approx 8$ MV/m, $\epsilon_2 \approx 160$ (state 2, no bias) $\epsilon_1 \approx 114$, thus $\frac{4\Delta\epsilon}{\epsilon_1} \approx 1$ and the condition holds true provided:

$$E_{\mathrm{rf}} \ll E_B = 8 \text{ MV/m}. \tag{39}$$

From these material parameters, we also obtain a value of the coefficient E_p of

$$E_p = 0.174 \times 10^6 \text{ (V/m)}. \tag{40}$$

We assume that the FE wafer is operated at a temperature of 50 °C, to allow cooling with room temperature water. At this temperature, the permittivity is taken as 96.4 at state 1 and 129.6 at state 2. The loss tangent at this operating temperature is 0.95×10^{-3}.

The tuner, its transmission line, and coupling to a cavity is shown in Fig. 5. For the transmission line from the wafer to the cavity, we use an inner radius of 1.96 cm and outer radius of 5 cm, corresponding to a characteristic impedance of 56.19 Ω.

The cavity's coupler of Fig. 5 has an external Q of $Q_e = 50000$. We assume a cavity with 4.5 J stored energy and we aim for a tuning range of 8 kHz.

A comparison of the analytic prediction and the CST [14] numerical simulations is provided in Table II. The calculation of the series capacitance C_s from the geometry used in the CST model included 3D fringe fields [15]. A detailed description of the Maple code that provides the analytic results is provided separately [16].

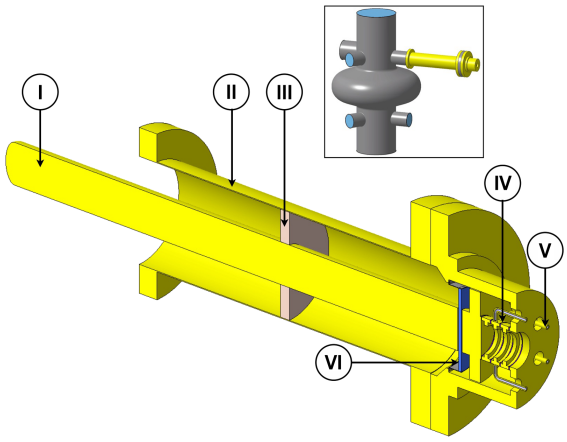

FIG. 5. Cutout view of the tuner of Fig. 4 with the full length of the transmission line. (I) Inner conductor of the transmission line. (II) Outer conductor of the transmission line. (III) Schematic of a possible dielectric support of the inner conductor. (IV) Ferroelectric stack. (V) Refrigerant line. (VI) Window. The inset figure shows the tuner connected to a cavity. The assembly shown is inside the vacuum vessel in the case of a superconducting cavity, or in air for a normal-conducting cavity. The internal volume of the transmission line and ferroelectric stack assembly is under vacuum in either case. Various engineering details are not shown due to the limited scope of this paper, such as heat sinks on the cavity's coupler and rf and bias connections to the refrigerant lines.

Where two numbers are provided in Table II, they correspond to state 1/state 2 of the ferroelectric.

The harmonic power generated is under 1 W, which is negligible for this particular set of parameters.

As seen from Table II, the analytic model provides a surprisingly good estimate of the required parameters of the tuner and its performance. Given the frequency of this example, 400 MHz, one expects an even better agreement at lower frequencies. The analytic estimates provide close to target initial values for the numeric simulations.

TABLE II. Comparison of the tuner's performance as given by the analytic model and finite-element electromagnetic solver. Where two numbers are shown that they correspond to the two states of the bias (full bias or zero voltage). Three dots represent no evaluation done.

Parameter	Units	Analytic	Numeric
Power change state 1 to state 2	VAR	452 000	⋯
Tuner reactance at cavity port	Ω	−56.2/56.2	−56/56.7
Tuner resistance at cavity port	Ω	0.74/0.67	0.70/0.81
Dissipation in FE material	W	1763/1411	⋯
Total dissipation in tuner	W	2985/2699	3534/2827
Average wafer temperature rise	°C	13/11	⋯
Power loss at inner conductor	W	110/120	⋯
Figure of merit	⋯	80	74
Q_{FRT}	10^6	3.8/4.2	3.2/4.0
Series capacitor C_s	pF	39.2	39.2
Window capacitor C_w	pF	5.47	5.64
Length of transmission line	cm	67.7	65.4
Frequency tuning of cavity	kHz	8.0	8.6

A technical challenge in the design of a very high reactive power tuner at high frequency is the cooling of the ferroelectric wafers. The power density in the ferroelectric material is high, requires good thermal conductivity to the copper spacers, and determines to some extent the operating temperature of the wafers. The analytic model uses the thermal conductivity of the ferroelectric material [2] to calculate the peak temperature rise of Table I. Another source of temperature increase is the thermal contact resistance between the wafer and the spacer. Using a thermal contact conductance with a thermal interface material of approximately 10^5 W per degree square meters [17], the temperature rise across this resistance is 3 °C.

V. SUMMARY

A novel design of a ferroelectric fast reactive tuner comprising a short coaxial transmission line terminated by a circuit comprising a stack of parallel wafer capacitors and a few other rf components has been presented. This stacked ferroelectric design offers a simple geometry of the wafers that is straight forward to fabricate and assemble and can be efficiently cooled in order to maintain stable electromagnetic operation. Further, the ability to connect multiple wafers in a series electrical circuit design makes the management of biasing the ferroelectric structure feasible and offers significant reduction of the required tuning bias while enhancing the tuning figure of merit of the unit.

A novel feature of the FE-FRT tuner concept presented is option of use of a reactive element in series with the ferroelectric capacitor stack to create a tuner resonant mode whose frequency can swept over the cavity resonant frequency by changing the bias voltage applied to the ferroelectric components. This coupled resonant mode configuration acts to significantly increase the tuning range for a given Q_e. Alternatively for a required tuning range, such a coupled resonance approach may be employed to raise the Q_e of the cavity tuner port.

For these FE-FRT concepts, the analytical model has been developed and detailed for the generic tuner case, and the model predictions confirmed with finite-element electromagnetic simulation of a resonant tuning design coupled to a typical SRF cavity (based on a 400 MHz elliptical SRF cavity typical of the CERN LHC rf design). Excellent agreement between the analytic model and the numerical solution has been established, even at the high frequency of 400 MHz, giving confidence in corrections to the ferroelectric capacitance that were included in the analytic model. In addition, evaluation of the parametric dependence of the tuner has shown the conceptual design has the capability to provide very high reactive power tuning at high figure of merit values. The aforementioned nonlinear effects due to the voltage-dependent permittivity were crucial to the success of the modeling, and the study

resulted in the introduction of an annular shape for the ferroelectric capacitor, which played a key role in the reduction of losses in the tuner circuit.

Several tuner circuit configurations have been addressed, to highlight the versatility of the FE-FRT concept, with both nonresonant and resonant configurations possible. These configurations are well suited for proportional control over a given tuning range, with the choice if configuration primarily dictated by the required tuning range of the application. Also discussed is a detailed design for ferroelectric tuning applicable to accelerator physics operation and provided the an outline design of such a tuner in a practical scenario for a 400 MHz SRF cavity, currently under construction at CERN.

Finally, we highlight as a part of the realization of the resonant tuner design, the capacitive coupling of the tuner to the cavity through a window. This window coupling is part of the tuner rf design but also has the dual advantage of isolating the tuner vacuum from the cavity vacuum, and allowing for simplified installation of the tuner to an ultraclean SRF cavity.

In conclusion, the ferroelectric fast reactive tuner concept has been addressed and developed, based on a stacked ferroelectric capacitor structure embedded in several novel configurations that lend themselves to implementation. We present an accompanying analytic model facilitating the design of such tuners, which includes refinements such as the detailed reactance modeling of the conductor/ferroelectric/conductor transition. In addition, the analytic model led to the adoption of the annulus geometry of the ferroelectric stack reducing the tuner losses. This model has been successfully compared against detailed numeric finite-element calculations of three-dimensional tuner realizations. Finally, a conceptual realization of a 400 MHz fast reactive tuner with an exceptional tuning range, capable of an average power up to nearly half a MVAR has been detailed. Our results open the possibility for fast tuning of cavities, both normal and superconducting, with multiple applications in rf accelerators.

ACKNOWLEDGMENTS

We gratefully acknowledge the support of our colleagues on related aspects of our research on ferroelectric tuners, A. Kanareykin and C. Jing (Euclid Techlabs LLC). In addition, A. C. would like to acknowledge that this work is supported by Jefferson Science Associates, LLC under U.S. DOE Contract No. DE-AC05-06OR23177.

[1] K. Shepard, P. Markovich, G. Zinkann, B. Clifft, and R. Benaroya, Superconducting low-velocity linac for the argonne positive-ion injector, in *Proceedings of the 1989 IEEE Particle Accelerator Conference Chicago, IL*, (IEEE, New York, 1989), pp. 974–976.

[2] A. Kanareykin, E. Nenasheva, S. Karmanenko, A. Dedyk, and V. Yakovlev, Low-loss ferroelectric for accelerator applications, in *Proceedings of the 21st Particle Accelerator Conference, Knoxville, TN, 2005* (IEEE, Piscataway, NJ, 2005), pp. 4305–4307.

[3] V. Yakovlev, O. Nezhevenko, and J. Hirshfield, Active rf pulse compressor with a ferroelectric switch, in *Proceedings of the 20th Particle Accelerator Conference, PAC-2003, Portland, OR* (IEEE, New York, 2003), pp. 1150–1152.

[4] V. P. Yakovlev, S. Y. Kazakov, and J. Hirshfield, 1.3 GHz electrically-controlled fast ferroelectric tuner, in *Proceedings of the 10th European Particle Accelerator Conference, Edinburgh, Scotland, 2006* (EPS-AG, Edinburgh, Scotland, 2006), p. 487.

[5] A. Kanareykin, S. Kazakov, A. Kozyrev, E. Nenasheva, and V. Yakovlev, Ferroelectric based high power tuner for l-band accelerator applications, in *Proceedings of the 4th International Particle Accelerator Conference, IPAC-2013, Shanghai, China* (JACoW, Geneva, Switzerland, 2013), p. 2486.

[6] N. Shipman, J. L. Bastard, I. Ben-Zvi, G. Burt, A. Castilla, M. Coly, F. Gerigk, A. Macpherson, and N. Stapley, A ferroelectric fast reactive tuner for superconducting cavities, in *Proceedings of the 19th International Conference on RF Superconductivity, SRF-2019, Dresden, Germany* (JACoW, Geneva, Switzerland, 2019), pp. 781–788.

[7] N. C. Shipman, I. Ben-Zvi, G. Burt, A. Castilla, M. R. Coly, F. Gerigk, C.-J. Jing, A. Kanareykin, A. Macpherson, N. Stapley, and H. Timko, Ferro-electric fast reactive tuner applications for SRF cavities, in *Proceedings of the 12th International Particle Accelerator Conference, IPAC-2021, Campinas, Brazil* (JACoW, Geneva, Switzerland, 2021), pp. 1305–1310.

[8] S. Y. Kazakov, S. Shchelkunov, V. Yakovlev, A. Kanareykin, E. Nenasheva, J. Hirshfield, T. Khabiboulline, H. Hahn, and E. Choi, Fast high-power microwave ferroelectric phase shifters for accelerator application, AIP Conf. Proc. **1086**, 477 (2009).

[9] W. Xu, Z. Altinbas, S. Belomestnykh, I. Ben-Zvi, M. Cole, S. Deonarine, M. Falletta, J. Jamilkowski, D. Gassner, P. Kankiya *et al.*, Design, simulations, and conditioning of 500 kW fundamental power couplers for a superconducting rf gun, Phys. Rev. ST Accel. Beams **15**, 072001 (2012).

[10] I. Ben-Zvi, A. Castilla, A. Macpherson, and N. Shipman, High-power ferro-electric fast reactive tuner, arXiv: 2109.06806.

[11] Maplesoft: Maple is a trademark of Waterloo Maple Inc., Maple (2019), https://www.maplesoft.com.

[12] B. Freemire, Measurements of the dielectric properties of a ferroelectric ceramic for use in a fast reactive tuner, Technical Note No. CERN-ACC-NOTE-2020-0070, 2020, http://cds.cern.ch/record/2881905.

[13] C. Jing, Ferroelectric Ceramic measurements at 400 MHz, CERN Internal Technical Note No. EDMS 2995632, 2023, http://cernbox.cern.ch/s/39PS9JGTu2wA7lV.

[14] CST Studio Suite, CST Microwave Studio, 2008.

[15] T. Sakurai and K. Tamaru, Simple formulas for two- and three-dimensional capacitances, IEEE Trans. Electron Devices **30**, 183 (1983).

[16] I. Ben-Zvi, A. Castilla, A. Macpherson, and N. Shipman, Analytic computation of a ferro-electric fast reactive tuner, CERN, Geneva, Switzerland, Technical Note No. CERN-ACC-NOTE-2023-0021, 2023.

[17] D. D. L. Chung, Materials for thermal conduction, Appl. Therm. Eng. **21**, 1593 (2001).