SLAC-PUB-95-6950
July 1995

VXD3: the SLD Vertex Detector Upgrade Based on a 307 MPixel CCD system*

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ABSTRACT

The SLD Collaboration is building a new CCD vertex detector (VXD3) comprising 96 3.2 Mpixel CCDs of 13 cm^2 each for a total of 307 million pixels. This system is an upgrade of the pioneering CCD vertex detector VXD2 which has operated in SLD since 1992. The CCDs of VXD3 are mounted on beryllium ladders in three cylinders, providing three space point measurements along each track of about 5 microns resolution in all three co-ordinates. The design and construction of VXD3 builds on three years of successful performance of VXD2. Significant improvements are achieved with VXD3 in impact parameter resolution (about a factor of two) and acceptance (~20%) through optimized geometry and reduced material. New readout electronics have been developed for this system This new vertex detector will be installed in late 1995 for the future runs of SLD.

Contributed to the 1995 International Europhysics Conference on High Energy Physics (HEP95), Brussels, Belgium, July 27-August 2, 1995.

*This work was supported by Department of Energy contracts: DE-FG02-91ER40676 (BU) DE-FG03-93ER40788 (CSU), DE-FG02-92ER40715 (Massachusetts), DE-AC02-76ER03069 (MIT), DE-FG06-85ER40224 (Oregon), DE-AC03-76SF00515 (SLAC), DE-AC02-76ER00881 (Wisconsin), DE-FG02-92ER40704 (Yale); National Science Foundation grant PHY-92-03212 (Washington); the UK Science and Engineering Research Council (Brunel and RAL); the Istituto Nazionale di Fisica Nucleare of Italy (Bologna, Ferrara, Frascati, Pisa, Padova, Perugia); and the Japan-US Cooperative Research Project on High Energy Physics (Nagoya, Tohoku).

Motivation for SLD vertex detector upgrade

The SLD pixel vertex detector VXD2[1], placed close to the e^+e^- intersection point(IP), in conjunction with small SLC beam spots, has given SLD outstanding flavor-tagging performance for three years of operation. The successful operation of this 120 MPixel device is a validation of its suitability for the special SLC beam environment. The experience with VXD2 has answered the fundamental questions about the mechanical stability, hit efficiency, and resolution capability associated with a CCD-based pixel vertex detector. VXD2 has the world's best capability in many performance criteria. Nevertheless, due to the limitations of technology at the time of designing VXD2, limited resources, stringent time schedule, and some conservatism necessarily attached to a pioneering design, some aspects of the performance were compromised. The upgrade to VXD3 (illustrated in figure 1) will significantly improve performance and open new, exciting possibilities for physics at SLD.

Advances in the technology of CCD detectors have made it possible to design a vertex detector with much better impact parameter resolution, larger solid angle coverage and virtually error-free track linking. These will allow a world-class measurement of the polarization-enhanced forward-backward asymmetry for b- and c- quarks and improved precision in the measurement of the b-fraction in hadronic Z decays, sufficient for testing radiative corrections in electroweak theory. A wide range of measurements can be made which will make use of full separation of primary, secondary and tertiary vertices. The most exciting new possibility, afforded by the upgrade, however, is the search for B_S-mixing - leading to a measurement of the mixing parameter, x_S. A data sample of half a million Zs with the upgraded vertex detector and highly polarized beams will give SLD the capability to measure B_S mixing up to values of x_S of 15 or greater. The basis for this measurement is the large forward-backward asymmetry for $e^+e^- \to b\bar{b}$, provided by polarized electrons from SLC. With 78% polarization (the current average polarization at the SLD IP), a forward going meson has a 75% probability of being a B rather than $\bar{B}$. This allows a statistical tag of the $B/\bar{B}$ character of each B_S^0 at production, using the asymmetry. One may plot the forward-backward asymmetry versus decay time of the observed B^0. The value of A_{FB} will oscillate with a $\cos(x_S\, t/\tau)$ dependence. Detailed Monte-Carlo simulations of such a measurement show that VXD3 substantially improves the sensitivity to mixing for x_S between 10 and 20. The striking improvement with the upgraded vertex detector comes from the following effects:

(a) Better vertex resolution extends our sensitivity to higher x_S values.

(b) The improved vertex detector is expected to have a better efficiency of reconstructing the B^0 decays length. We estimate that the 26% efficiency of the current VXD2 will improve to around 50% with VXD3

(c) The larger acceptance of the new vertex detector, from $\cos\theta$ of 0.75 to 0.85, may appear to be small but in fact is quite significant. The number of B's accepted grows as $1+\cos^2\theta$, also the forward-backward asymmetry is larger at larger $\cos\theta$, and the usefulness of the new high $\cos\theta$ region accessed by VXD3 grows like A_{FB}^2.

These improvements have been achieved by the changes in the detector design discussed below.

VXD3 detector design and comparison with VXD2

The impact paramter resolution of VXD2 is illustrated in Figure 2. VXD2 has 4 barrels of loosely spaced ladders with barrel-2 ladders covering the azimuthal (ϕ) gaps of barrel-1, and barrel-4 ladders covering the ϕ gaps of barrel 3 (see Figure 3a). Thus VXD2 provides only 2-hit coverage for most of azimuthal region, with about 30% of the tracks having 3 or more hits. The present availability of large area CCDs allows a simplified ladder design using only 2 CCDs covering the entire length of the ladder, permitting a three layer system with practical mechanics. Each barrel provides complete azimuthal coverage, as a result of the 'shingled' structure between ladders (see Figure 3b). Due to the large number of CCDs on one VXD2 ladder(8), it was cost prohibitive to make ladders longer for increased solid angle coverage. So VXD2 provides a 2-hit coverage only up to $|\cos\theta| = 0.75$ (ladder active length 92.3 mm) (see Figure 4a). Having new CCDs with the 80 mm length (instead of 12.3 mm in VXD2), the active ladder length (with only 2 CCDs on each ladder) is 158 mm, which gives the $|\cos\theta|$ coverage up to 0.85 (see Figure 4b). The choice of $|\cos\theta|_{max} = 0.85$ was made to provide best matching to central drift chamber (CDC) coverage, which is necessary for VXD linking, thus providing uniform tracking over the whole sensitive $\cos\theta$ region. Deterioration of spatial resolution at small polar angles is not an issue thanks to the very thin active EPI silicon layer of 20 μ m on the CCDs.

Besides solid angle coverage, the track impact parameter resolution near the IP is the other driving consideration behind the detector geometry layout. The best way to improve the impact parameter resolution and coverage is to reduce the beampipe radius. However, SLD already has an inner beampipe radius of 25 mm. By moving the upgrade beampipe inner radius to 23.5 mm, a layer-1 radius of 28.40 mm is possible. In this configuration, the outer radius is chosen as a compromise between maximizing the lever arm of the tracking for improved impact parameter resolution, and maximizing the solid angle coverage with 80 mm long CCDs. We therefore selected a layer-3 radius of 48.26 mm to achieve the desired solid angle coverage, to $|\cos\theta|_{max} = 0.85$. Another major contribution to the impact parameter resolution is multiple scattering at low and intermediate track momenta. By using beryllium as the motherboard stiffener, and thinning the CCDs to 150μ m, the material radiation length for a VXD3 ladder is reduced to 0.4% (compare to 1.15% for VXD2 ladder). Experience gained by operating VXD2 also suggested reduction in the thickness of titanium liner of the existing beampipe (100μ m) by factor of 2, since the very soft photons which this liner is designed to absorb do not make a large contribution to the background. A similarly motivated reduction in the beryllium beampipe thickness from 1.0 mm to 0.75 mm is mechanically acceptable, and further reduces the multiple scattering. Lever-arm lengthening and the detector material reduction improve both transverse (x-y) and longitudinal (r-z) impact parameter resolution by more than a factor of 2 compared to VXD2 at low momentum. Lever-arm lengthening also improves the longitudinal impact parameter by a factor of about 2 at high momentum. The dependence on CDC phi angle measurement has also been reduced for the high momentum impact parameter resolution, making VXD3 closer to a standalone detector for impact parameter resolution with the global alignment between CDC and VXD becoming less critical. The shingled VXD3 barrel layout gives a more efficient and uniform azimuthal coverage such that the average inner hit radii are reduced compared to VXD2, and also corrects the problem of large lever-arm variation with ϕ in VXD2. The VXD3 layout is such, that in case one hit is lost, the resulting lever arm is still better than that achievable with the fully efficient two-layer VXD2. Figure 5

illustrates the comparison of vertex detector resolution of VXD2 and VXD3. Resulting impact parameter resolution as a function of momentum for two different $\cos\theta$ values (0 and 0.75) for both VXD2 and VXD3 are represented in Table 1.

Momentum (GeV)	$\cos\theta$	VXD2		VXD3	
		xy impact	rz impact	xy impact	rz impact
0.5	0.0	112.2	112.3	66.2	66.2
1.0	0.0	65.0	66.2	37.1	37.2
3.0	0.0	30.6	40.7	19.9	21.6
6.0	0.0	19.7	36.8	15.0	19.4
45.0	0.0	12.7	35.4	11.6	18.7
1.0	0.75	103.5	104.7	60.8	61.2
3.0	0.75	47.0	54.3	27.2	28.2
45.0	0.75	17.7	42.8	14.4	20.0

Table 1. *Impact parameter resolution in microns.*

Mechanical Structure

The vertex detector is supported by a structure made from instrument grade beryllium. The beryllium components are match pinned and doweled to achieve the stable environment. Mating surfaces are lapped with one μ m precision. The CCD ladders are supported at each end via beryllium rings mounted to the inner faces of the endplates. All joints between dissimilar materials are designed to allow for thermal contraction variation during cool-down. This support structure follows the previous VXD2 design, with some improvements.

The vertex detector is operated at cryogenic temperature (~—80°C) in order to completely suppress dark current and loss of charge transfer efficiency from radiation damage. The vertex detector cryostat is illustrated in Figure 1. Liquid nitrogen boiloff gas is piped in through a beryllium jacket surrounding the beryllium beampipe. The clearance between the two is 0.75 mm. A number of fine holes allow the gas to flow out through the outer jacket into the detector cryostat, creating a uniform flow of gas from the innermost to the outermost barrel of the detector.

The vertex detector is being surveyed with an OMIS II coordinate measuring machine. Every ladder is surveyed individually before assembly, and each barrel is surveyed following assembly to a few micron precision.

Electronics and Readout

The CCDs are n-buried channel devices fabricated on p-type epitaxial layer and having a p+ substrate. They have an active area of 80 mm x 16 mm. They are operated in a full-frame readout mode. The substrate resistivity is specified to be less than 20×10^{-3} ohm-cm to maintain short carrier lifetimes. The epitaxial layer is 18-22 microns thick with a resistivity of ~ 20 ohm-cm for adequate diffusion length, optimal diffusion/drift ratio, and clean high rate clocking. The pixel sizes are 20 um x 20 μm. The readout register operates on two-phase clocking and the imaging area on three-phase. There are 4 readout nodes, one on each corner of the device, with 800,000 pixels per node (see Figure 6).

The readout system for VXD3 represent a significant advance over that of VXD2 (see Figure 7). The pixel readout rate is 10 MHz (cf. 2 MHz for VXD2), so despite the

increase in pixel quantity, nearly a factor of two decrease in system readout time has been achieved without compromise in noise performance. Advances in electronics permit much more compact drive and readout circuitry. Most of the control and signal processing circuitry has been moved inside the SLD detector, eliminating most of the cable plant and simplifying commissioning and operation. The readout electronics consist of 16 analog-to-digital (A/D) boards , placed close to the CCDs, and connected with high speed optical links to FASTBUS Vertex Data Acquisition modules (VDA). A/D boards also have all necessary circuitry to generate CCD clocks and biases. Every A/D board has 24 channels of amplifiers with a gain of 100, and 24 8-bit flash ADCs, serving 6 CCDs. Digitized signals are organized into serial data using multiplexers based on XILINX programmable gate arrays, and are transmitted via 1.2 GHz optical data link (two per A/D board), using the Hewlett-Packard Gigabit Rate Transmit- Receive chip set, and FINISAR optical transmitters. Every board also contains a Motorola M68HC11 microcontroller, which is used to download the XILINX code, CCD image clock waveforms, DC offsets for amplifiers, and CCD enable-disable signals (to be able to disconnect defective CCDs from bias and clock sources). There is also a possibility to put the board into calibration mode, when pulses of known amplitudes are generated and connected to the CCD output nodes. The microcontroller is functional only during initial (after power on) download phase of operation, or on demand to change any settings. During readout of data, the microcontroller clocks are off, to reduce the possibility of noise increase due to crosstalk to amplifier inputs. During readout all functionality of the A/D board is provided by the fast logic sequencer, a device based on the AMD fast programmable logic MACH220 chip. VDA modules are a modification of those used in VXD2. The main function of the VDA module is to reduce the 307 Mbytes of raw data to a manageable size (< 100 kbytes). This is achieved by hardware reconstructing 2-d clusters of charge deposition and imposing a threshold that gives > 99% efficiency for minimum ionizing particles traversing 20μ m of silicon. Modification of the VDA boards involves usage of the faster processor (MC68040 instead of MC68020), larger front end and processor memory, new cluster processor design, and new front end design.

Test result of setup phase CCDs

Because of the unique requirements of the CCDs for VXD3, it is essential to have prototype devices fabricated and tested before production of the full batch of devices. The CCD manufacturering[2] is proceeding in two phases: the first phase for production of a few CCDs, which are methodically tested at SLAC to verify that all specifications are met. After positive results of this test, phase 2 production of the bulk of the CCDs has started. The first phase CCDs were manufactured with two designs of output node amplifiers (actually 2-stage source followers). The first stage employs either a surface channel or a buried channel FET. The advantage of the buried channel FET is its lower noise level. But this type of device requires a higher power supply voltage and, consequently, higher power dissipation on the CCD, which is not desirable due to the limited cooling system resources. In the February 1995 we received phase 1 devices, and results of the evaluation of these devices follows.

Noise.

The noise level for CCDs with a buried channel FET in the output node was about 27 electron charges rms, well below our specification of 63 e with a 10 MHz bandwidth. For the surface channel FET in the first stage output node, the noise level is about

45 e, which is also within specification. The optimum power supply voltage for buried channel - surface channel options are 22 V and 17 V respectively. Because of the power dissipation concerns, and because the surface channel option satisfies the specified noise level, it was decided to choose this type of devices for production.

Responsivity.

The detector responsivity was measured, using signals from an Fe^{55} radioactive source. The peak position of the amplitude distribution of these signals gave us the detector responsivity 3.1 μ V/e, which combined with the gain of 100 of amplifiers on A/D boards and the minimum ionizing particle production of 7200 e in the detector sensitive layer (20 micron) generates signal of about 360 mV on the ADC input, or about 45 ADC counts.

Charge transfer efficiency.

This parameter was measured both for transfer along R register, and through the image area. We used degradation in the cluster central pixel signal amplitude as a measure of charge lost from charge transfer inefficiency. The inefficiency in one transfer appeared to be less than $5x10^{-5}$ in the R register and less than $1x10^{-5}$ along the image area.

Spurious charge generation.

Due to defects in silicon or in manufacturing, there is a possibility of abnormal high charge accumulation in certain pixels during the detector integration time. We call such pixels "hot", and a maximum number of such hot pixels was included in the specifications. Most of the phase 1 CCDs have very few hot pixels (typically none, sometimes 1 or 2 per CCD). Another source of spurious charge generation was found in some CCDs, which generated current, leaking into the R register. Though the generated charge usually also was within specification, the manufacturer claims that they know the source of this charge (spurious tunnel diode structure, introduced as a result of a design error in the gate protection circuit), and will eliminate this in the production phase.

Detector efficiency.

The transfer of a small amount of charge without loss through a CCD is more difficult than transfer of a large charge. The smallest irregularities in the electric field in the silicon may create potential pockets, which will then retain some of the charge while it moves through. Because such defects may be randomly distributed across the CCD area, the probability for charge moving along the area to encounter such a "charge trap" is proportional to the length of the path the charge has to travel, and so it affects large area CCDs more than small devices. In the phase 1 CCDs we have observed a number of such charge traps. We have devoted a large effort to investigating the nature of these traps, and their effect on detector efficiency. Some of them absorb such a large amount of charge that the entire signal from a minimum ionizing particle is lost. Others just reduce the signal amplitude, so the signal still may be used to find the particle coordinate, but the precision of such measurement may suffer. Typical phase 1 CCDs have 1-2 completely blocked columns per node (out of 400) due to such traps; since the part of the blocked column between the location of the trap and the R register does not suffer, it leads

to a 0.125 - 0.25% inefficiency. Also about 3-5 columns with smaller charge loss usually were seen in every channel.

Though such inefficiency is quite acceptable, some modifications of the CCD design were made to reduce the number of these charge traps. The manufacturer believes that mask misalignments are the major cause of these traps. Overlapping of I-clock strips was minimized in the design to reduce the capacitance, and misalignment can produce gaps between I-clocks phases. These gaps may create traps due to charge accumulation in the silicon oxide passivation below the polysilicon I-clock strips. The overlap will now be increased slightly. Also, the supplementary channel, which was added to increase the radiation hardness of the CCD, will be removed, since it also may contribute to the observed trapping. From tests we have determined that the radiation hardness of our detectors is much better than we need, and the supplementary channels are unnecessary.

Radiation hardness.

One of the phase 1 CCDs was exposed to the radiation from a Co^{60} source with the total accumulated dose of 15 kRad. We measured the detector parameters a few times during the exposure and did not find any serious degradation in the detector performance. With the full dose, a small (~10%) loss of signal amplitude from the Fe^{55} source is observed.

Upgrade schedule

Production of the CCDs for VXD3 started in April, 1995 and will be accomplished in 9 batches. The first batch is scheduled for delivery in July. The final batch will be delivered in September. Ladder assembly, survey, and CCD testing will start immediately upon arrival of the first batch, and all assembly and commissioning of VXD3 will be finished by December 1995, when the next SLD run is scheduled to start.

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1. G.D. Agnew et al, "Design and Performance of the SLD Vertex Detector, a 120 MPixel Tracking System," Proceedings of the XXVI International Conference on High Energy Physics, Dallas, TX, 1992.

2. The CCDs are being manufactured by the EEV Company, Chelmsford, Essex, England.

LIST OF FIGURES

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5. Comparison of VXD2 and VXD3 impact parameter resolut ons. The boxes at from data with VXD2. The lower curves are the expected improvement with VXD3.

6. VXD3 CCD schematic drawing.

7. VXD3 electronics block diagram.

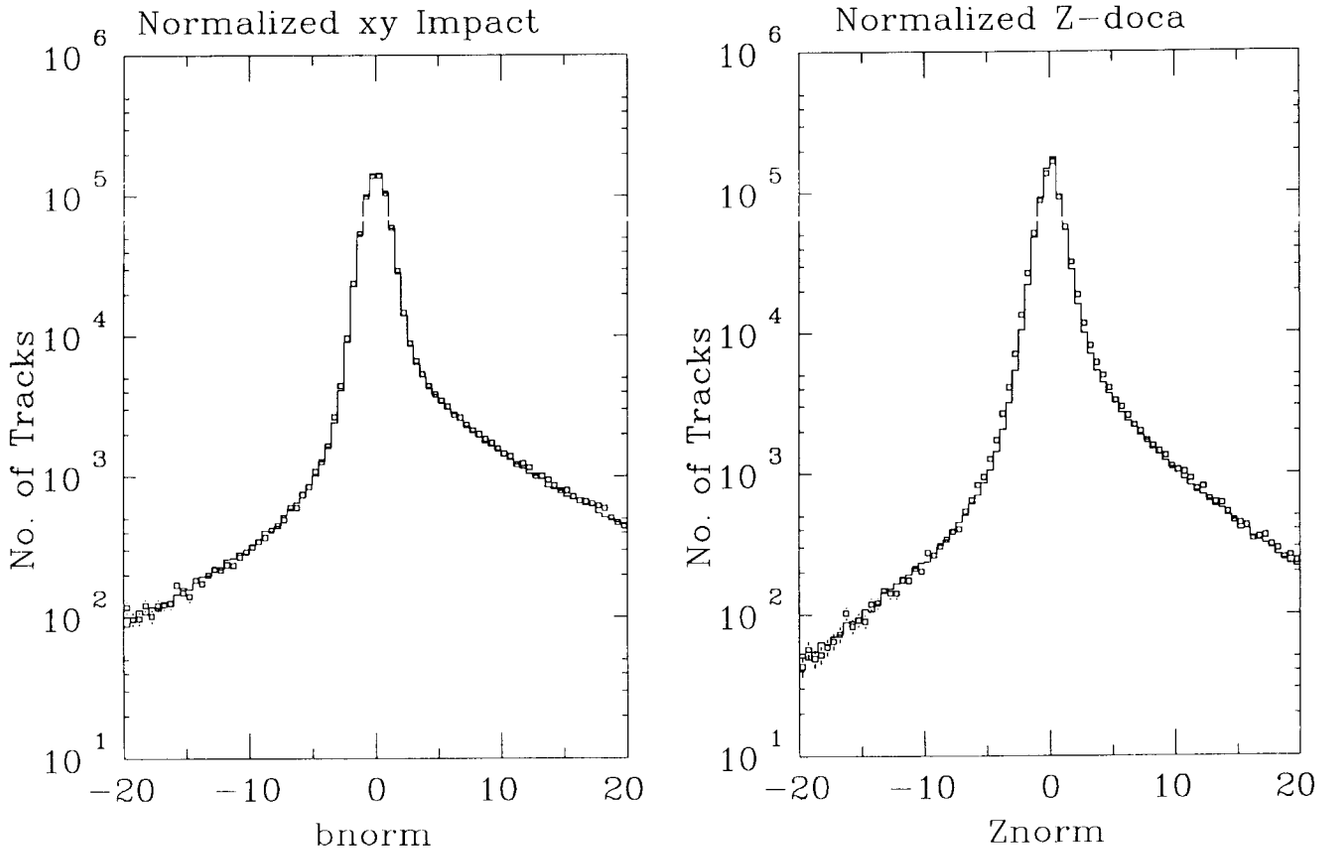


Figure 2

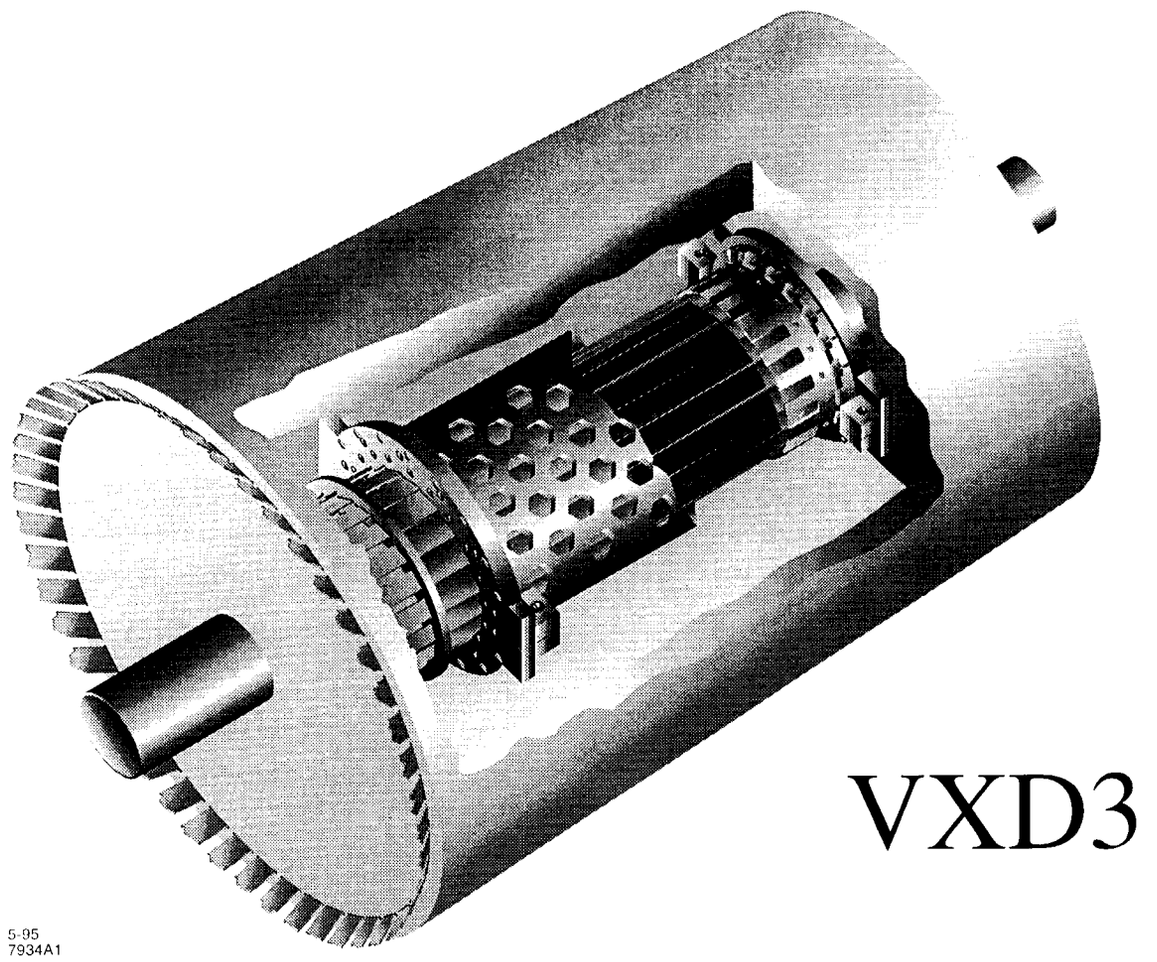


Figure 1

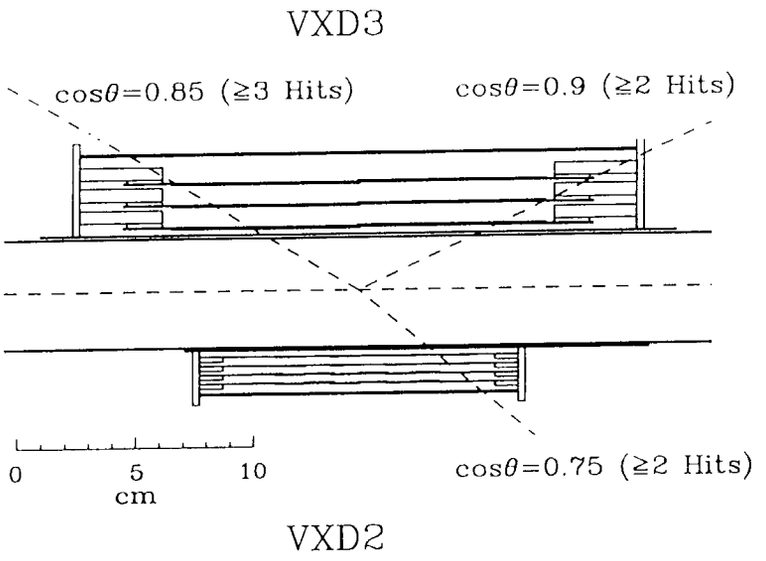


Figure 4. Comparison of VXD2 and VXD3 RZ profiles showing beam pipe, beryllium support structure, ladders, and CCDs.

Figure 4

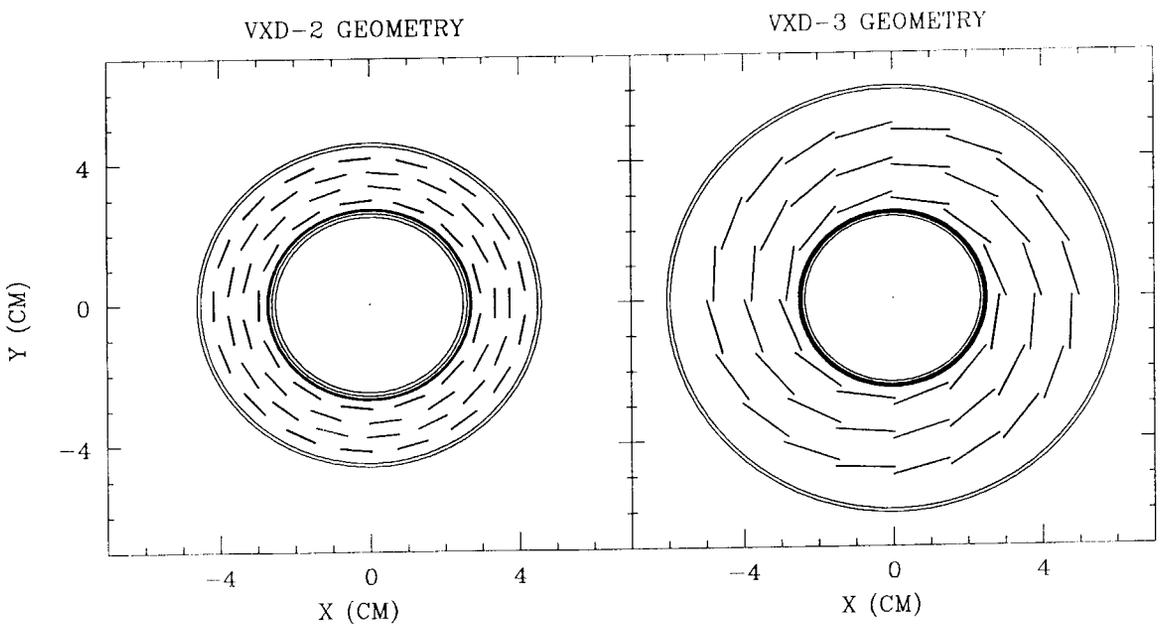


Figure 3

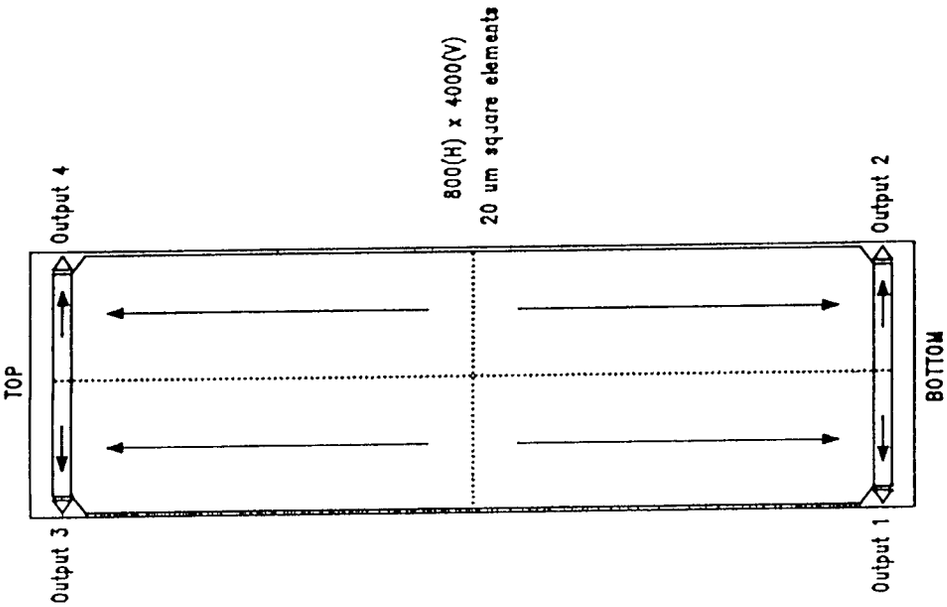


Figure 6

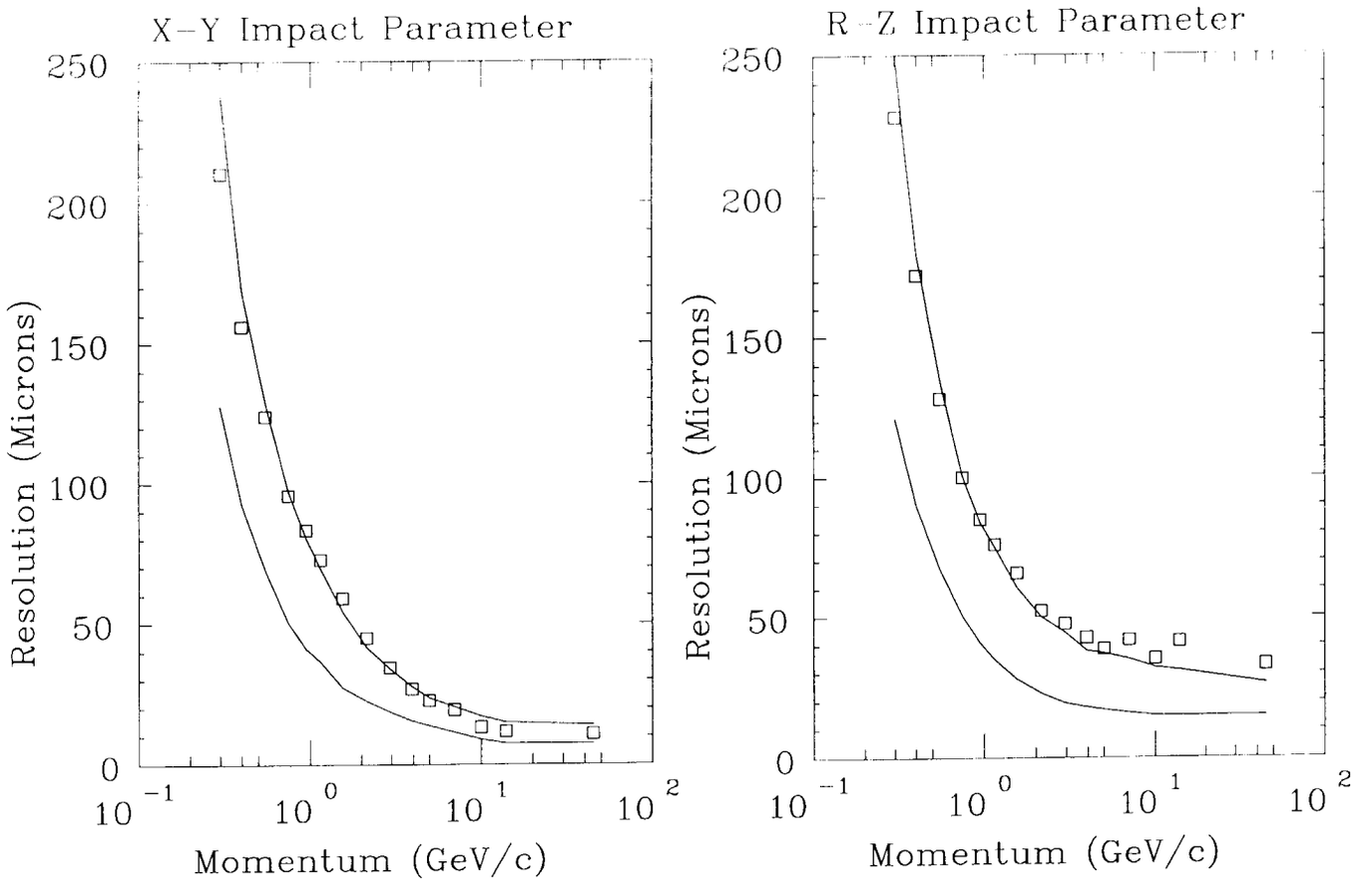
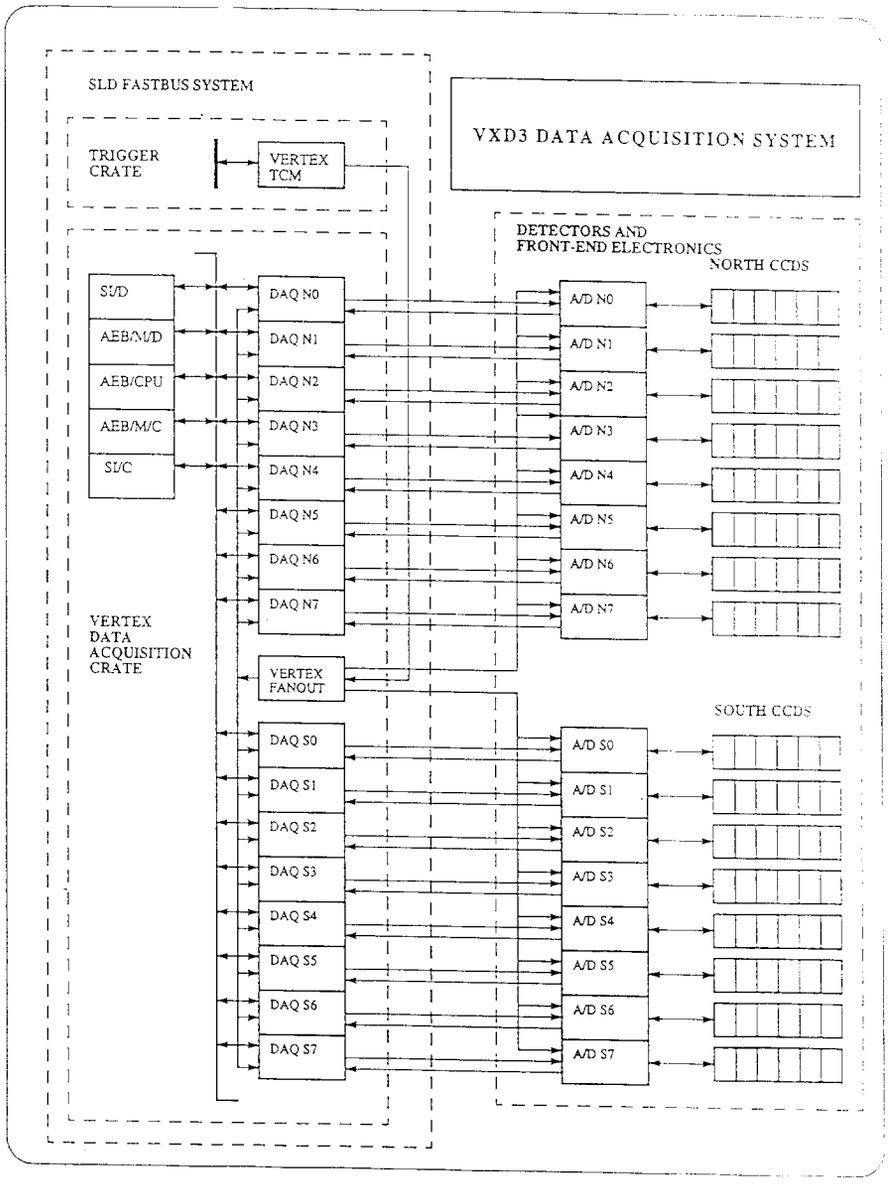


Figure 5


SLD FASTBUS SYSTEM
TRIGGER CRATE
VERTEX TCM
VXD3 DATA ACQUISITION SYSTEM
DETECTORS AND FRONT-END ELECTRONICS
NORTH CCDS
SI/D
AEB/M/D
AEB/CPU
AEB/M/C
SI/C
DAQ N0
DAQ N1
DAQ N2
DAQ N3
DAQ N4
DAQ N5
DAQ N6
DAQ N7
A/D N0
A/D N1
A/D N2
A/D N3
A/D N4
A/D N5
A/D N6
A/D N7
VERTEX DATA ACQUISITION CRATE
VERTEX FANOUT
SOUTH CCDS
DAQ S0
DAQ S1
DAQ S2
DAQ S3
DAQ S4
DAQ S5
DAQ S6
DAQ S7
A/D S0
A/D S1
A/D S2
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A/D S6
A/D S7

Figure 7