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The optimization, design and performance of the FBCM23 ASIC for the upgraded CMS beam monitoring system

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Abstract: We present the development of the FBCM23 ASIC designed for the Phase-II upgrade of the Fast Beam Condition Monitoring (FBCM) system built at the CMS experiment which will replace the present luminometer based on the BCM1F ASIC [1]. The FBCM system should provide reliable luminosity measurement with 1 ns time resolution enabling the detection of beam-induced background. The FBCM23 ASIC comprises 6 channels of the fast front-end amplifier working in transimpedance configuration, booster amplifier, and leading edge discriminator. The complete processing chain provides an overall shaping function equivalent to the CR-RC^3 filter. The paper will show the optimization of the design, overall architecture, and the detailed implementation in a CMOS 65 nm process as well as preliminary electrical performance.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Radiation-hard electronics; VLSI circuits

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Contents

1 Specifications and optimisation of the design

The primary role of the FBCM [2] system is accurate luminosity measurement with 1 ns time resolution that will provide the detection of beam-induced background. To meet this requirement from the physics point of view, the FBCM sensors should have a particular area and distance to the beamline, balancing occupancy, and acceptance. A good compromise between the area and the position of the sensor in the experiment is provided by a 1.7×1.7 mm silicon pad installed at a radius of around 14.5 cm [3]. The radiation environment in this position is rather harsh, and the detector modules should stand up to 200 Mrad of total ionizing dose (TID) and particle fluxes up to 2.5×10^{15} N/cm^2 1 MeV equivalent. Although the 65 nm CMOS process can stand the expected TID dose without major issues, the increase of the leakage and degradation of charge collection efficiency (CCE) from the heavily irradiated sensors have to be taken into account during the noise optimization of the front-end amplifier and final choice of the sensor thickness.

For the FBCM detector, a cost-effective solution will be to produce the sensors using either 290 µm material of the outer tracker or 150 µm wafers used by the pixel detector. Both solutions have advantages and drawbacks, and the FBCM23 ASIC has to support both options. The expected numbers for the leakage currents are in the micro-Amper range. The worst case values should be estimated using the figures published in [4] or [5] and scaled to the intended operating temperature of −35°C.[1] Operating the sensors at such temperatures sets some restrictions on the power dissipated by the ASIC. Although there are no hard constraints from the point of view of the designed cooling and power supply systems, it will be reasonable to limit the power dissipation of the ASIC below 100 mW and, consequently minimize expected temperature gradients on the detector module. For the 150 µm sensor working at −20°C after 2.5×10^{15} N/cm^2 one can expect the leakage in the range of 2 µA. The same leakage will occur for the 290 µm sensor and fluence of 1×10^{15} N/cm^2, which is most likely the maximum allowable dose from the point of view of CCE dropping to about 50 % (see predictions in [6]). That means that FBCM detector built with 290 µm sensors has to be replaced in the middle of the operation, which in fact will be possible on the occasion of the replacement of the innermost layer of the pixel detector. Although the degradation of the CCE and leakage will be lower for the thinner sensor (0.95 and 1 µA respectively after 1×10^{15} N/cm^2, see [6]), one should keep in mind that it will also provide a smaller charge before irradiation as well as it will show higher

[1] The figures presented in the literature are normalized to +20°C. The typical setups used for the characterization of the irradiated sensors work down to −20°C.

capacitance (around 4 pF to be compared to 2 pF for 290 µm sensor). The contribution of the shot noise coming from the sensor leakage to the total ENC is shown in figure 1. One can see that for the shaping time in the range of 4 to 8 ns and for the expected leakages below 3 µA, this contribution can be kept at a reasonable level, under 400 e^- ENC.

One can stress that the fast shaping times are important not only from the standpoint of the optimal filtering of the noise contributed by the sensor leakage but also from the point of view of the timing requirements. The time-walk for the leading edge discriminator (LED), which is the most robust solution for the binary system, connected to 8 ns peaking time CR-RC^3 shaper will be below 5 ns. This is what is compatible with the requirements of 1 ns rms time resolution.

In order to provide a reasonable Signal-to-Noise Ratio (SNR) above 10 at the end of the detector lifetime for any sensor option, the series noise contribution from the input transistor should be kept below 700 e^- ENC. Figure 2 shows the optimization[2] of the input transistor dimensions and the bias for the worst case of 5 pF input capacitance (4 pF sensor + 1 pF contingency for the parasitics). One can see that for 2000 µm width of the input transistor, chosen for the FBCM23 input stage, biased with 2 mA current, the maximum contribution of the series noise is below 600 e^- ENC. Figure 3 and 4 show the optimum peaking times for both options of the sensor thickness irradiated up to 1×10^{15} N/cm^2.

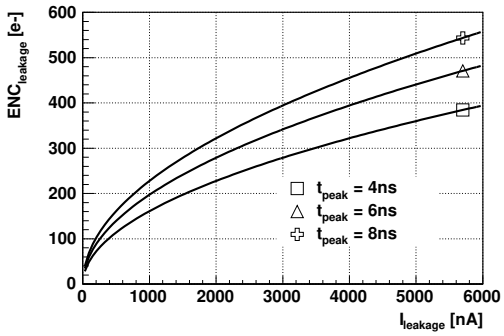

Figure 1. Noise contribution from the sensor leakage current for 6 and 8 ns peaking time and the CR-RC^3 shaping.

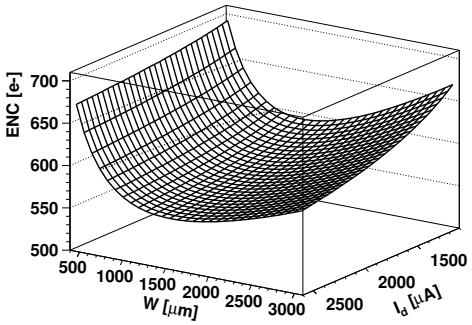

Figure 2. Series noise contribution for 8 ns peaking time and the CR-RC^3 shaping for 5 pF input capacitance (−20°C).

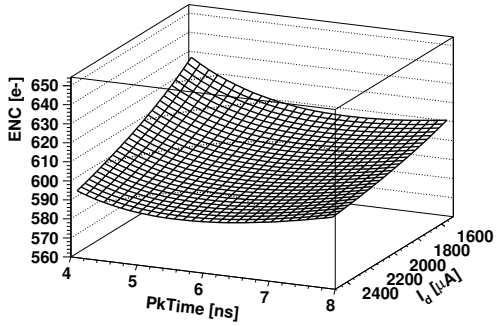

Figure 3. The total ENC figure showing optimum peaking time assuming 3 pF input capacitance and 2 µA leakage current at −20°C operation.

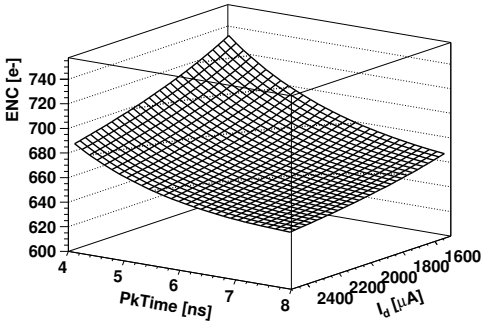

Figure 4. The total ENC figure for 5 pF input capacitance and 1 µA leakage current (−20°C).

[2]All noise calculations were performed using models described in [7] and [8].

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While the optimal peaking time for the 2 µA leakage is around 5 ns from the ENC standpoint (see figure 3), one should also watch the possible degradation of CCE due to ballistic deficit effect in the heavily irradiated sensor. For thinner sensors and lower leakage currents, the optimal peaking time is closer to 8 ns. Its further increase will be limited by the requested time resolution of the ASIC.

2 ASIC implementation

The binary architecture employed in the FBCM23 ASIC provides simplification of the off-detector electronics and allows for direct interfacing to the LPGBT chip [9], which is the core of the CERN standard digital transmission system. Because of the limited number of channels on the detector module (6), it is possible to read each single FBCM23 channel output by the LPGBT input, which is capable of sampling the data with 800 ps time bin resolution. This approach simplifies the design of the FBCM23 ASIC, which consists of six parallel binary front end channels associated with a number of peripheral blocks providing biasing of the amplifier stages, threshold control, and calibration function. The block diagram of the FBCM23 ASIC is shown in figure 5. The FBCM23 comprises 6 identical

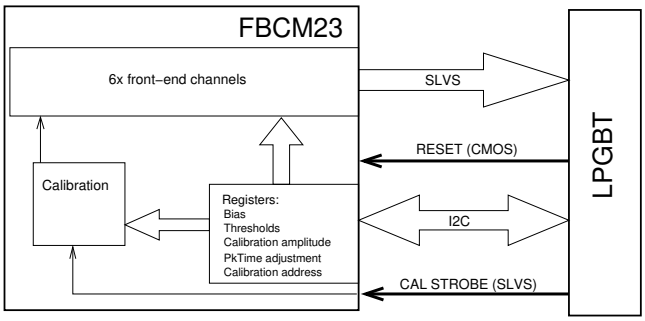

Figure 5. Block diagram of the FBCM23 ASIC.

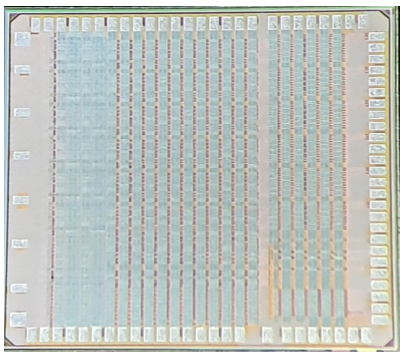

Figure 6. Photo of the FBCM23 ASIC.

channels layouted on the 3×3 mm^2 of silicon area. All bias and configuration registers are accessible via a standard I2C interface. The chip has been implemented and fabricated in 65 nm CMOS process. During the layouting of the ASIC, considerable attention has been drawn to the correct separation of the analog and digital domains using deep NWELL transistors and guarding techniques reinforced by blocking the substrate doping using the mask intended for the native devices. Special care has been put on the robustness of the power grids implemented with top, thick metals. On the photograph of the ASIC shown in figure 6 one can see the top metal vertical power grid occupying about 50 % of the top metal area. Another thick metal layer is used for the horizontal power distribution along the electronic channels. The analog part of FBCM23 consumes for the nominal settings around 32 mA, from which about 40 % is spent in the input transistors. About 28 mA is consumed by the digital part, mainly the SLVS output drivers. The simulated DC drops across the power bars are below the 1 mV range.

The schematic diagram of the preamplifier is shown in figure 7. The input stage is built with the regulated telescopic cascode amplifier, with the NMOS input transistor of 2000/0.2 µm biased with 2.1 mA and loaded with low voltage cascode PMOS sources. The simulated open loop gain and gain-bandwidth product (GBP) are around 69 dB and 3.5 GHz respectively, which allows for

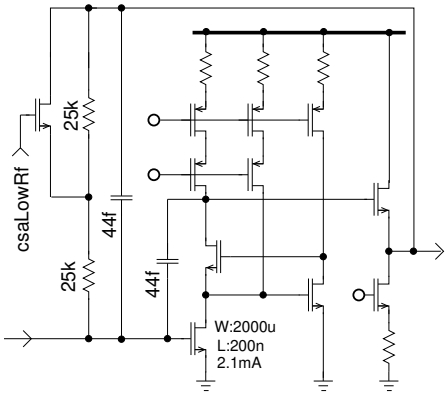

Figure 7. Schematic of the preamplifier.

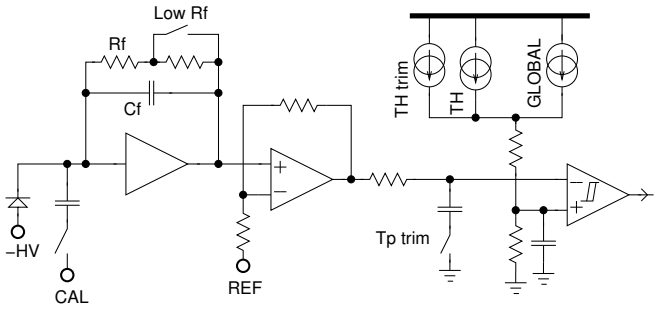

Figure 8. Schematic of one front end channel.

the fast shaping of the detector pulses. The preamplifier works in a transimpedance configuration with an adjustable feedback resistor (50 or 25 kΩ).

The simplified schematic diagram of the front end channel is shown in figure 8. The transimpedance preamplifier is DC coupled to the booster amplifier and leading edge discriminator. Although this intrinsically provides good stability of the baseline in case of high and variable hit rates, it is a less satisfactory solution from the standpoint of the mismatch variation which is amplified by DC-coupled amplifier stages. The DC variation at discriminator input is nearly 100 mV pk-pk and to compensate for this, two 8-bit threshold DAC's per channel have been employed. Another 8-bit DAC, common for the chip, is used for the global offset setting. The gain of the full chain for the nominal settings is around 60 mV/fC. The switchable RC filter (RC set range between 0 and 6) provides adjustment of the peaking time between 5 and 9 ns range, which helps in the optimization of SNR for various input load conditions (sensor capacitance and leakage current). The complete processing chain consisting of the preamplifier, booster amplifier, RC filter, and input stage of the discriminator provides an overall shaping function equivalent to the CR-RC^3 filter. The outputs of the discriminators are sent outside the chip through SLVS interfaces.

3 Test results

The initial evaluation of the ASIC has been carried out using the internal charge injection circuitry based on an 8-bit DAC supplying a DC current to the resistor which is short-circuited by an NMOS switch controlled by the strobe signal provided by an external pulse generator (Agilent 81110a). The calibration charge is injected into the front end amplifier input through on-chip, per channel 52 fF calibration capacitors. The output of the single channel is read out by the Agilent 53132A counter (noise and gain measurement) or by the Tektronix scope MSO64B (timing characterization). Gain and noise are extracted from threshold scan measurements at three different charges, 1, 1.5, and 2 fC. Each threshold scan is fitted with a complementary error function (S-curve) from which the median and width can be extracted. The gain is extracted from the dependence of the median on the injected charge whilst the noise is extracted from the fit to the noise occupancy scan. The timing variation of the front end as a function of the injected charge (time-walk) is measured as a delay of the output pulse with respect to the strobe signal for different injection charges and the discriminator set to the operating threshold.

Figure 9 shows the threshold scans performed for 1, 1.5, and 2 fC injected signals together with the fit to the complementary error function for one particular setting of RC filter. The medians of the fitted S-curves as a function of the injected charge for three different settings of the RC filter are shown in figure 10. The gain extracted from the scans agrees well with the simulated values, e.g. measured 60.2 mV/fC and simulated 58.5 mV/fC for RC = 3. The example of the noise occupancy scan for the bare channel and RC set to 3 is shown in figure 11. From this figure, one can extract not only the output noise but also the peaking time of the shaper response. The latter can be estimated from the maximum frequency of the noise hits at zero threshold using the Rice formula [10]. A summary of this theorem from the standpoint of the front end signal processing chains can be found in [11]. The peaking time calculated for this particular setting of the RC filter is around 5.3 ns which agrees well with the simulated value. The 2.9 mV output noise combined with the channel gain of 60 mV/fC gives the ENC of 300 e^- which has to be compared with the simulated 320 e^-. Figure 12 shows the measurement of the time walk for the signals between 1.2 and 11 fC for the threshold of 1 fC. The 4.5 ns time walk agrees well with the simulated numbers.

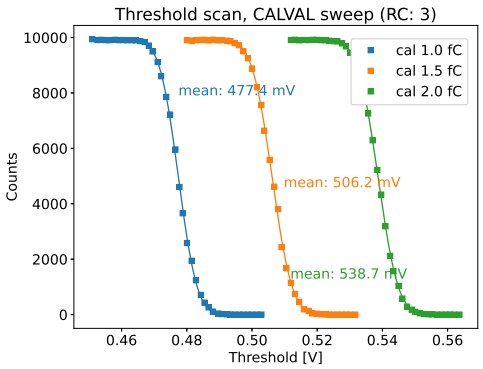

Figure 9. Threshold scans for 1, 1.5, and 2 fC charge injection and RC set to 3. Channel with unloaded input.

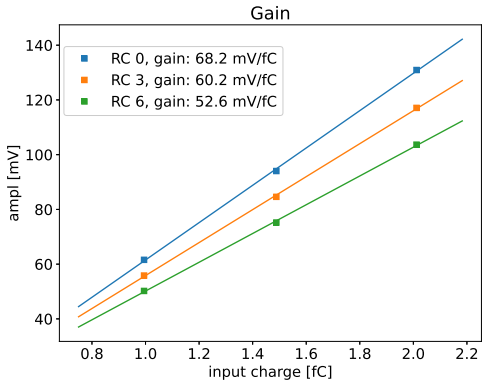

Figure 10. The gain measurement for RC set to 0,3 and 6.

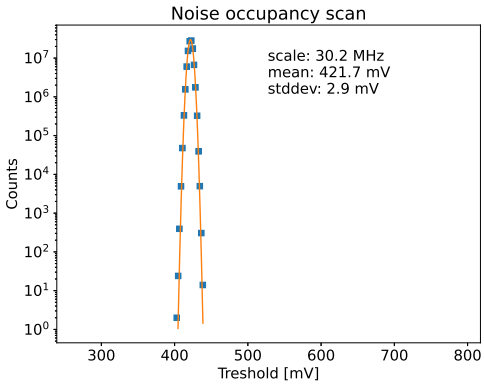

Figure 11. The noise occupancy scan for the channel with unloaded input and RC set to 3 (nominal configuration).

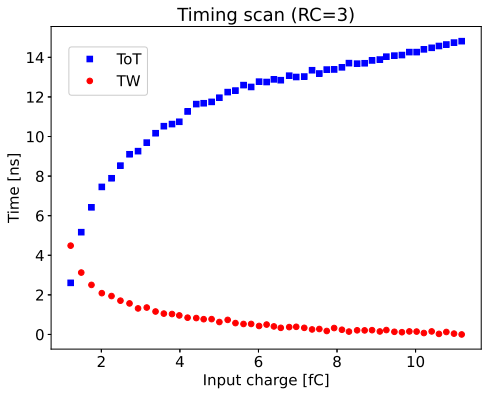

Figure 12. Time walk and time over threshold measurement for RC set to 3 (nominal) and threshold set to 1 fC.

4 Summary

The FBCM23, a CMOS 65 nm radiation tolerant readout ASIC has been designed and fabricated for the FBCM detector of the CMS experiment. The initial characterization of the ASIC confirms that the FBCM23 performance in terms of time resolution and noise levels is within the specifications. A more elaborated readout system using CMS tracker data acquisition modules is under development. It will allow for testing simultaneously of all ASIC channels i.e., it will provide higher statistics in a shorter time and will be also used in the upcoming test beams. The X-ray irradiation of the FBCM23 ASIC is planned in the coming weeks.

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