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SAMBUCA: SENSORS ACQUISITION AND MOTION CONTROL FRAMEWORK AT CERN

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Abstract

Motion control applications at CERN are often characterized by challenging requirements, such as high positioning precision (in the order of 1 ppm) in extremely radioactive environments (i.e., Total Ionizing Dose up to 30 MGray) and axes synchronization below one ms. These demanding specifications are particularly relevant for the Beam Intercepting Devices (BIDs), such as the Large Hadron Collider (LHC) collimators. With such radiation levels, reading or driving electronics need to be placed in safe areas up to several hundred meters away from sensors and actuators, while typical industrial solutions can work with cable lengths only up to a few tens of meters. A massive R&D phase lasting several years has been required to develop mechatronics solutions able to ensure the requested positioning precision in such a challenging environment. It includes the development of rad-hard actuators, new position sensors, novel reading algorithms, and actuator control solutions. The acquisition and control systems currently in operation for the LHC Collimators are based on off-the-shelf PXI cards, controllers, and chassis from National Instruments. In the frame of the control system renovation foreseen for Long Shutdown 3 (LS3), the high-performance field Sensors Acquisition and Motion Control synchronized all across the 27-kilometer length of the LHC. This synchronization achieves a positioning precision of just a few µm on a 30-millimeter movement range.

The same level of precision has been attained when reading the collimator position sensors, such as LVDTs and resolvers. This accomplishment can be attributed to the development of sophisticated signal-processing algorithms. It is worth noting the impressive nature of this performance, considering the extensive cable lengths between sensors/motors and the conditioning or driver electronics, which can span up to 1 kilometer [2].

Another notable development is for Piezo goniometers employed for crystal collimation in the LHC [3]. In this project, a mechatronic solution was developed to attain an angular positioning precision of 1 micro-radian (1 µrad) on a 20 milli-radian (20 mrad) stroke length. This level of precision is achieved through the utilization of advanced piezo actuator control methods and the implementation of Fabri-Perot based interferometry for angular measurements.

The existing control systems rely on software from the LabVIEW RT PXI platform and hardware from National Instruments, which have been effectively adapted and customized to meet the stringent reliability and availability standards required for CERN's critical missions [4]. However, as part of the comprehensive overhaul planned for framework (SAMbuCa) has been conceived and is currently under development. It represents a complete in-house, modular, and flexible hardware and software framework able to cope with the highly demanding requirements of motion control applications at CERN, optimizing development and long-term maintenance costs. It standardizes the R&D achievements and the return of operational experience of the last 15 years on BIDs mechatronics. After LS3, more than 1200 axes at CERN will be controlled with SAMbuCA. In this paper, the hardware and software framework architectures are described in detail as well as each building block. The development and deployment plan will be also detailed.

INTRODUCTION

Over the past 15 years at CERN, remarkable progress has been made in enhancing the precision of positioning and synchronization of motorized axes. The overall reliability and availability of the mechatronics systems have improved, as well as the ability to operate in highly radioactive environments.

One notable example is the Low-Level Control System (LLCS) for the LHC collimators [1]. In this system, more than 500 stepper motor axes are the

LHC collimator LLCS in LS3, there is a move away from the conventional "off-the-shelf" approach. This shift aims to avoid vendor lock-in and potential inaccessibility of firmware.

The proposed Sensors Acquisition and Motion Control framework (SAMbuCA) is designed to fulfil the existing and future requirements for mechatronics in the CERN Accelerator domain by considering feedback gathered through extensive operational experience with the LHC Collimator LLCS. The main objective is to deliver a modular, user-friendly, and flexible control solution for mechatronic devices. It will serve as the standard solution to reduce development time and long-term maintenance costs.

The framework features precise control capabilities of mechatronic solutions with control cables extending up to 1 kilometre, catering to a wide range of actuators including stepping, brushed, and brushless motors, as well as piezo actuators. Additionally, it offers accurate readings from an extensive array of field sensors, such as LVDTs, resolvers, potentiometers, switches, PT100 sensors, and strain gauges.

The next section will describe the SAMbuCa hardware architecture as well as its new building blocks, highlighting the improvements compared with the existing solution.

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In addition, we present the solutions developed to provide a user friendly and scalable abstraction layer for the low-level motion control software libraries and the steps taken to validate and secure the designs for mission critical systems, ensuring a long lived and robust system.

HARDWARE ARCHITECTURE

The key aspects of the SAMbuCa hardware architecture are shown in Fig. 1.

- **PXIe standard:** After having conducted an extensive technical market analysis, it was determined that the PXIe standard represents the ideal successor to both PXI and VME [5].
- **PXIe carrier card** for data processing and RT control. The PXIe carrier card is equipped with a robust System on Chip (SoC) designed to serve as the host for real-time processing. It forms the essential core of the control application. When designing the current LHC collimator LLCS, the controlling FPGA board was selected with a Mean Time Between Failures (MTBF) approximately one order of magnitude higher than that of the host controller, in addition to having a deterministic and robust real-time behaviour. The proposed architecture adheres to a similar philosophy, aiming to localize critical processing tasks onto the PXIe carrier's FPGA and less critical tasks on the CPU. This approach offers modularity, with the potential of dedicating a single PXIe carrier to each individual device.
- **FPGA Mezzanine Cards (FMC):** To interface with the instrumentation (LVDT, resolvers, IOs, strain gauges, Traditional high-density connectors are typically employed for linking digital/analog I/O with field modules. Unfortunately, they may be susceptible to issues like oxidation or corrosion, potentially compromising the integrity of the signals. In the proposed architecture, this obstacle has been addressed using robust external connectors such as Lemo or military-grade micro SUBD. This approach ensures a high level of reliability for the entire system. The same level of reliability extends to the expansion chassis, where FMC modules communicate to the PXIe carrier via redundant optical links, further enhancing system reliability and robustness.
- **White Rabbit synchronization:** A White Rabbit based PXIe timing card is foreseen to be installed in each PXIe chassis, ensuring ns level synchronization between the hundreds of motorised axes across the 27 km of the LHC. With a jitter at the nanosecond level, starting trigger pulses are distributed to every PXIe carrier via the PXIe backplane star trigger lines. Additionally, White Rabbit enables the synchronization of all PXIe carrier clocks, leveraging the PXIe internal 100 MHz clock feature. This synchronization ensures precise coordination when executing extended motion profiles across the axes, such as for the LHC collimators, where motion profiles can last up to 30 minutes.

interferometer reading, motor drivers, etc.) the FMC standard was chosen. It consists of a mezzanine card (84 mm by 69 mm in size) with two connectors (160 or 400 pins). The mezzanine cards will host the I/O logic, ADC or DAC, while a small front-panel space is available for external connectivity.

- **Scalability ensured by expansion chassis:** The proposed architecture modularity aligns with the high bandwidth requirements of the LHC collimator LLCS, where each PXIe carrier card is responsible for either motion control or sensor acquisition for a specific collimator device. This architecture is well-suited also for applications characterized by numerous field interfaces, which are distributed across expansion chassis housing multiple FPGA Mezzanine Cards (FMC) on dedicated carrier boards or peripheral boards. These FMCs are interconnected within the expansion chassis and linked to a System Board via the expansion chassis backplane.

To facilitate this interconnectivity, the System Board within each expansion chassis is linked to the PXIe carrier card in the front-end using a high bandwidth link, employing protocols like the Xilinx chip-to-chip protocol or dedicated Ethernet protocols. The optical link allows for a connection among several expansion chassis.

- **Improved field connectivity:** One of the most critical factors that could impact the reliability of the control system, is the connectivity between the control system I/O and the field modules.

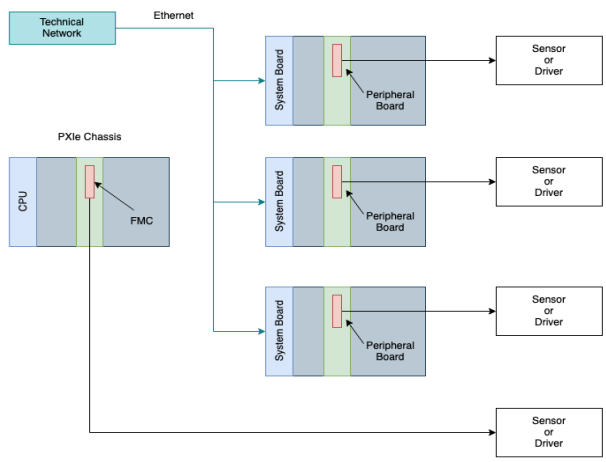

Figure 1: SAMbuCa hardware architecture.

PXIe High Availability Chassis

The PXIe chassis, shown in Fig. 2, is realized using an 8-slot PXIe-1082 backplane from National Instruments, built and designed by an external company, based on CERN specifications. It is aimed at high availability systems in critical missions at CERN. The design key points are:

- 2 redundant power supplies
- monitoring card for diagnostics (Ethernet)
- Redundant DC/DC power converter
- Rugged chassis

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- 2 redundant fan trays
- Daisy chained clock (BNC connector on the front panel in Fig. 2)
- remote reset power cycle input (BNC on monitoring card)

Figure 2: PXIe high availability chassis.

PXIe-COMe adapter

The PXIe system controller is based on a COM Express module. A generic 3U PXIe based COMExpress system controller has been developed and is available in Open HardWare Repository (OHWR) [6]. The CPU will run a Linux Debian 12 distribution the future standard OS for CERN accelerator complex front ends.

Figure 3: PXIe - COMe adapter.

PXIe FMC Carrier: SPEXI7U

The SPEXI7U PXIe FMC carrier is based on a SoC from the Xilinx Zynq UltraScale+ MPSoC family. It integrates a feature-rich 64-bit dual-core Arm® Cortex®-A53 Application Processing Units (APU), a dual-core Arm Cortex-R5F Real Time Processing Units (RTU) and Xilinx programmable logic (PL) UltraScale architecture. The PL hosts the time critical control algorithms, as well as control logic and peripheral I/O communication (e.g. ADC and DAC) with the FMC cards.

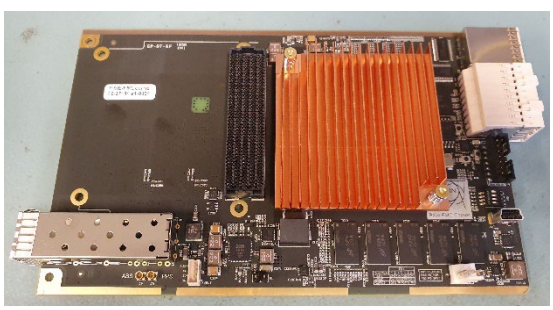

Figure 4: The PXI express FMC Carrier Board (SPEXI7U).

The motion control and sensor algorithms run on the APU while the configuration firmware (i.e., bootloader, hardware diagnostic, hardware settings) runs on the RTS.

The card has 4GB of DDR4 memory on the APU and RPU as well as 2GB DDR4 memory for the PL. It also features White Rabbit connectivity for deterministic communication between systems. The SPEXI7U design is available in the OHWR [7].

Expansion Chassis

The CERN Distributed I/O Tier (DI/OT) non-radiation-tolerant platform [8] is used as expansion chassis. This ongoing project aims at offering a low-cost, reusable, modular hardware platform to host electronic modules that interfaces directly with the accelerator equipment. The hardware used (Fig. 5) consists of 8 slot CPCI-S crates; an off-the-shelf CPCI-S 300W power supply; a non-radiation-tolerant System Board equipped with a SoC Xilinx Zynq Ultrascale + ZU7, fully featured White Rabbit node and an Ethernet high speed communication mezzanine. It can be customised adding specific peripheral boards as for instance the reading card up to 20 PT100 sensors. In addition, the FMC cards used for SPEXI7U can be mounted on a DI/OT generic peripheral board carrier, providing a low-cost, expandible solution that is suitable for motion control applications with multiple axes at a slower sampling speed.

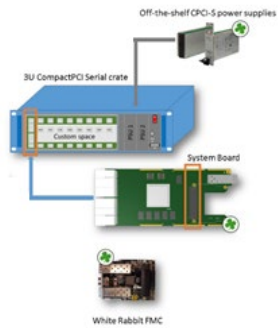

Figure 5: SAMbuCa expansion chassis: DI/OT non-radiation tolerant platform.

FMC Cards

The FMC mezzanine Motion Front-End (MFE) is one of the SAMbuCa core modules. It provides both analogue and digital interfaces able to control a large variety of multi axis motion control systems, such as:

- The most common position sensors (i.e., LVDT, resolvers, potentiometers).
- High speed incremental encoder interface.
- Limit and home switches.
- Analogue and digital I/O fields.
- Driving interfaces for motor drivers (i.e., STEP/DIR, analogue output).
- Interlocks compatible with the CERN beam interlock controllers [9]

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The FMC MFE can control up to 8 stepping motor axes and acquire up to 8 LVDT/resolvers or potentiometers at the same time. It can also be used as a general-purpose analogue/digital input/output module. The main characteristics can be found on the OHWR [10]. The FMC MFE, shown in Fig. 6, occupies 2 PXIe slots as the digital I/O interface, due to space constraints, was implemented on a separate module connected through flat cables to the FMC card. The two front panel connectors have 3 micro SUBD connectors of which one is for the analogue interface and two for the digital input and output.

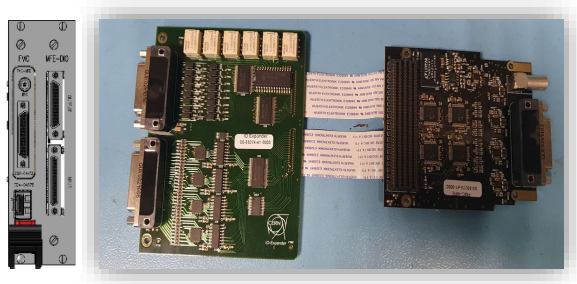

Figure 6: FMC motion front-end prototype.

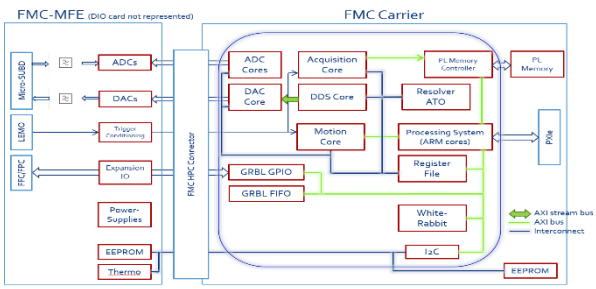

Figure 7: FMC motion front-end block diagram.

The main card functionalities as well as the main IP cores implemented on the SPEXI7U SoC PS are summarized in Fig. 7. A more detailed description of the gateware architecture implemented for the sensors reading and the motion control is given in the software architecture section.

Additional FMC cards are foreseen for specific applications such as PT 100 readings [11].

Motor Driver

The motor drive has been designed to accommodate all motor types (brushed and brushless DC, stepper) with special emphasis on having many different electrical phases on the same board and reducing electromagnetic interference (EMI) by employing high-voltage ceramic capacitors.

The board has 8 phases which can run independently up to 130 V and 5 A (continuous) on each phase. A DC link pre-charge circuit is added to avoid premature power connector failures.

The power side is electrically isolated from the low-voltage side (control system, communication, etc.) which operates from a single 12V external power supply.

The board is designed as a 220x100mm card and is compatible with the DI/OT chassis. The front panel has a 7-segment display and power connectors for input power and 8 electrical phases. Other low-voltage signals such as digital inputs and outputs, analogue inputs, and communication signals, have sockets on the backside which connects to the DI/OT chassis backplane. The board is not strictly limited to the DI/OT chassis form factor; we also foresee a dedicated backplane for standalone applications.

The rear connectors feature: (1) 2x UART and 1x SPI communication protocols, (2) 3x external encoder inputs, (3) 16x 12-bit analogue inputs, and (4) 10 digital inputs. Industrial communication protocols such as RS-422/485 or Profinet are not directly implemented on the board but can be implemented via the UART protocol.

The firmware for the microcontroller (C2000 family from Texas Instruments) is a full, in-house design, aimed at adapting the motor driver to any application within its hardware constraints. The main feature that distinguishes this motor drive with respect to similar off-the shelf solutions is the ability to compensate cable lengths up to 1 km. This feature is the key for precise positioning for stepping motor applications in radioactive environments [1]. Other notable features [12] are:

- Detection of steps lost and torque estimation based on Kalman filters.
- Closed loop control for encoder/resolver.
- Switching between closed and open loop control running in case of position feedback failure.
- Field Oriented Control (FOC).

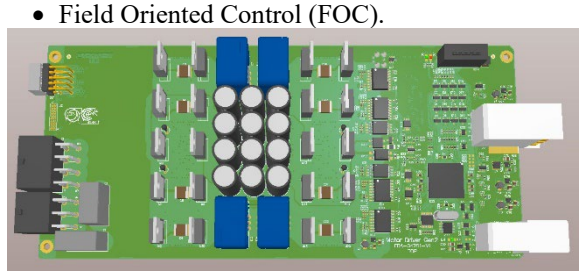

Figure 8: Top side of the motor driver.

SOFTWARE ARCHITECTURE

The SAMbuCa framework software architecture is summarized in Fig. 9. The PXIe system acts as a front-end, hosting the CERN FESA based control application [13]. The motion application development is simplified by the use of our high-level motion library (motion-lib) that provides a user-friendly abstraction of all the functionalities of motion control and field sensor acquisition. The library interacts with the hardware layer through a low-level driver that automatically gets generated by the SPEXI7U FPGA registers.

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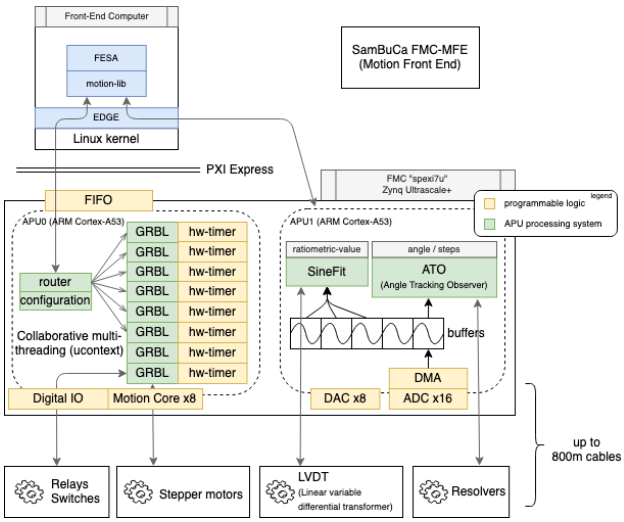

Figure 9: SAMbuCa software architecture.

Motion-Lib

The motion-lib is a C++ based library intended to abstract underlying hardware and to ease the business logic implementation of motion control applications by providing high-level device objects such as Axis motion, Position Sensors, and Triggers.

It implements all the required drivers and setup to communicate with the hardware, using appropriate low-level drivers and utilities provided by the in-house developed Encore Driver Generator (EDGE). This takes a text description of a memory map as input and automatically generates a Linux device driver, a user-space library, and a test program. Updates of the driver following a change in the memory map are also trivial and can be regenerated.

The motion-lib also embeds an HTTP/REST API that exposes the entire interface and allows advanced hardware inspection and debugging; this API is also extensively used in the functional and integration testing phase of the SAMbuCa framework. The UML API diagram is described in Fig. 10.

The motion-lib is designed to be scalable and implement additional hardware and features when needed. It is organized in three parts:

- a public interface, composed of a MotionController that is used to configure the library and access devices such as Axis for motion control configuration, a PositionSensor for the settings and acquisition of the supported position sensors, a GPIO for general purpose I/O management and an internal DeviceStore.
- an internal set of abstract platforms (e.g. PositionPlatform, GpioPlatform, Motionplatform) constructed through a PlatformFactory. They define the framework and interface for back-end implementors.
- the platform implementors that depend on the targeted hardware (e.g. SamBuCaPlatform, GrblPlatform) that are actual implementations of the above mentioned interfaces

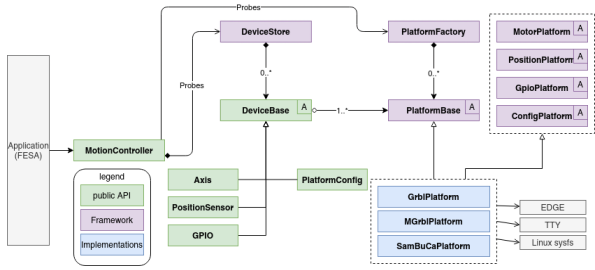

Figure 10: Motion-lib UML API diagram.

Position Sensors readings

The position sensors (LVDT or resolver) reading is performed by sampling the output signals at 550 kS/s on the FMC MFE, and streaming data via DMA for processing on the APU. The DAC output stage ensures the proper amplitude and frequency excitation according to the sensor model. Proper algorithms have been studied and implemented on the APU to reach the high precision reading required by CERN applications over cables up to 1 km in length. For the LVDT sensors, the amplitude demodulation of the two secondary signals is based on a sinefit algorithm and ratiometric reading of the linear position [2].

The resolver reading is instead obtained with an Angle Tracking Observer (ATO) algorithm [14]. A low-pass filtering stage is added on both the sine and cosine signals with a pre-processing stage added to compensate eventual phase-shift and signal offset; this stage requires the synchronization between the resolver excitation and the output signal acquisition to sample a complete period in each buffer. Signal offset is then deduced by performing an integral over the sampled values, with the mean value of the absolute sampled values used, thus eliminating any phase-shift and reducing background noise.

Value extracted from this pre-processing stage is then processed using the ATO algorithm.

Stepping motion controller

The motion-core relies on a GRBL-Hal [15] open-source project to generate the motion profiles, providing advanced features such as a motion-queue, backlash compensation, and homing sequences.

GRBL is designed to drive motors in a synchronous way, always considering the movement as a global motion, adapting each motor speed for all the axes to arrive at the same time; even though this feature is interesting in some use-cases, CERN applications sometimes require to have totally independent axes control. The open source implementation has therefore been customised on the APU to embed one instance of GRBL per axis, dynamically, deciding on which instance is driving which motor, leaving the flexibility to synchronize axes together or not.

A dedicated hardware timer implemented on the PL has been used to generate steps for each of those instances, and a collaborative multi-threading approach relying on the open-source library libucontext [16] has been used on the APU to sequence the dispatching thread.

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VALIDATION

A comprehensive testing methodology (Fig. 11) is being followed to guarantee that SAMbuCa meets the reliability requirements for CERN critical missions. It comprises three main stages: prototypes testing, series/pre-series testing, and continuous operational monitoring.

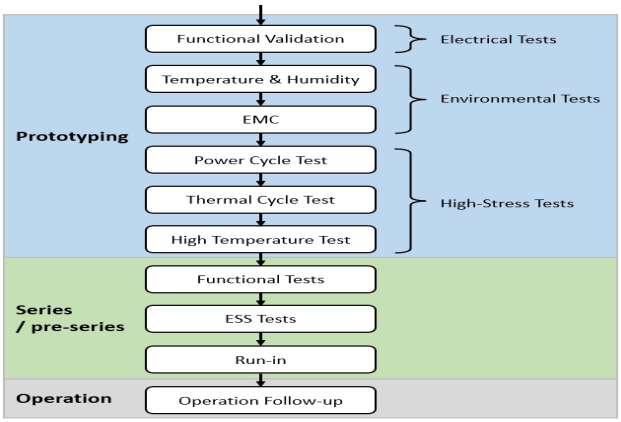

Figure 11: SAMbuCa testing methodology.

Prototypes Testing

Functional Validation tests are performed on all the SAMbuCa building blocks as soon as a mature prototype version is released. Individual modules are rigorously assessed to confirm that they perform according to the design specification and are pushed to their limits, ensuring they perform within the required parameters. The entire system is then tested under optimal operational conditions.

RobotFramework [17], an open-source test automation framework, is used to write and automate test plans using a low-code, behavior-driven development (BDD) style, making the test scripts human-readable and easy to understand. Several test suites have been implemented to both validate and ensure that features and requirements are met. This has been done using a versatile set of reference instrumentation (e.g., Palmers, encoders, logical analyzers) and software test utilities and interfaces (such as EDGE).

Once the functional validation is completed, the *reliability tests* start by subjecting the electronics to both temperature and humidity min/max cycles. Both single modules and entire PXIe chassis equipped with SPEXI7U, and FMC cards are tested. The tests are performed while the system is powered and operating under heavy load in a climatic chamber.

After the environmental tests, high-stress tests are conducted. The primary objective of these tests is to subject the system to conditions exceeding nominal parameters, thereby inducing failures that would not typically occur under normal operating conditions. The goal is to uncover failure mechanisms and vulnerabilities, ultimately leading to iterative design improvements to enhance system reliability. Primary failure sources from the literature [18][19][20], have driven the formulation of the following distinct high-stress tests:

- Power Cycling Tests, in which modules undergo 100 power cycles, simulating repeated on/off switching to evaluate their resilience.
- Temperature Cycling test, in which modules are subjected to temperature cycling, ranging from 0 to 80°C, with cycles occurring between 20 and 200 times, to assess the system ability to withstand thermal stress.
- High-Temperature Test, where the temperature is continuously increased until destruction. It's essential to note that this test is conducted on a limited number of samples due to its destructive nature. It specifically targets systematic rather than stochastic failures.

These high-stress tests collectively serve as crucial tools for identifying weaknesses to allow design changes to enhance system robustness and, as such, the overall reliability during nominal operation.

Pre-series and series testing

Once the prototypes successfully pass the stress-tests, the next step is pre-production testing. This involves three distinct steps: Functionality Tests, Environmental Screening Tests, and Run-in Tests. These tests are automated through an in-house developed Production Test Suite (PTS) based on Python. The PTS design comprises a generic component, which is reused across all modules and subsystems, alongside a layer tailored to execute specific tests on individual modules. The PTS facilitates exhaustive testing of one system at a time. The primary objective of *Environmental Stress Screening (ESS)* is to subject 100% of the SAMbuCa modules to stress levels recommended for critical systems that aim at triggering and discovering premature failures, often related to assembly defects [20][21]. Among the many different industrial production tests available, thermal screening emerges as the most common ESS test, capable of detecting a wide array of defects. During this test, the system undergoes cycles of temperature variations, with various temperature ranges, thermal rates, and number of cycles, determined according to the stress strength formula outlined in [21]. After the ESS test, a *Run-In* phase is executed. This has two main objectives: to make sure that the failure rate of the systems is below the expected limit (passing the initial, high failure region of the "bathtub curve") [21][22], and to calculate an upper failure rate towards the right-hand side of the bathtub curve. The principle of the run-in test is to cumulatively run the systems for a targeted amount of time by running several systems in parallel in nominal conditions. This step allows the calculation and validation of the Mean Time To Failure (MTTF) of the system. It will be carried out directly after the installation with continuous operation over several months before the start of the accelerator beam operation.

The combination of the ESS and Run-in test aims for a "zero-failure rate" when the systems are deployed in operation.

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Continuous operational monitoring

After the installation of the new systems, a hardware commissioning phase, taking place just before beam commissioning, is a crucial step to validate all the operational functionalities of the new control systems based on SAMbuCa when used in their final operational scenarios. Monitoring, preventive and corrective maintenance tools will also be developed to help the early identification of any critical issues in the framework or the developed applications.

USE CASES

In the coming long shutdown 3 of the LHC (2026-2028) SAMbuCa is targeted to be deployed for two critical motion control applications that will be described below.

LHC Collimator low-level control system consolidation

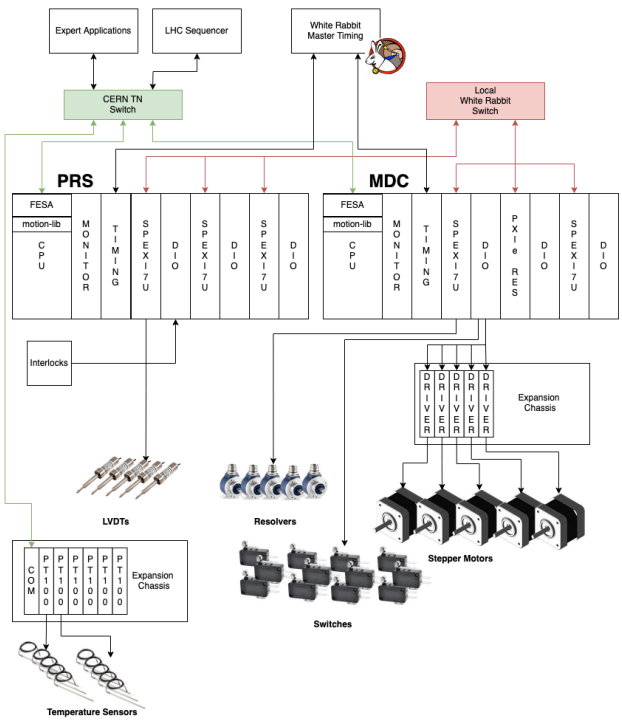

Figure 12: The new LHC collimator low level control system architecture SAMbuCa based.

The LHC collimator LLCS [1] will reach its end-of-life in LS3 and is planned to be consolidated with SAMbuCa. As in the current architecture, a couple of PXIe front ends will control up to 3 collimators (Fig. 12). To ensure the requested level of reliability, one PXIe system will be responsible for the Motor Drive Control (MDC) whilst the other one will be responsible for the Position Readout and Survey (PRS).

The MDC takes care of the motion control for up to 3 collimators, as well as the acquisition of resolvers and limit and anti-collision switches. A SPEXI7U card, equipped with an FMC MFE, is responsible for the motion control of the 5 stepping axes of one collimator.

The PRS handles the LVDT sensors reading of up to 3 collimators, performing an RT monitoring of the collimator jaw position at 100 Hz and comparing it with the safety limits. A SPEXI7U card, equipped with an FMC MFE, is responsible for reading the 7 LVDTs of one collimator as well as for driving the related beam permit outputs.

The White Rabbit (WR) timing card will ensure the synchronization at the sub-nanosecond level between all the PXIe chassis in all the front ends (i.e., MDC and PRS) all around the LHC, guaranteeing the synchronization of the motion and position survey profiles. The start trigger and machine information will also be distributed to each front end via the WR network. The SPEXI7U cards of both MDC and PRS in the same rack will be connected to a local WR network to allow deterministic data exchange such as for stop commands from the PRS to the MDC.

The stepping motor drivers to drive the axes of up to 3 collimators (i.e. 15 axes) could be potentially hosted in only one DI/OT chassis.

The LHC collimator temperatures will be read out by a dedicated DI/OT chassis equipped with PT100 reading cards.

The LLCS consolidation hardware will consist of 150 PXIe systems equipped on average with two SPEXI7U and FMC MFE cards per system.

FRAS low-level control system

In the framework of the High Luminosity (HL) LHC project, foreseen for implementation in LS3, nearly 1.2 km of the current accelerator will be replaced with new equipment relying on innovative technologies. A Full Remote Alignment System (FRAS) [23] is being developed to perform the remote alignment of the new HL-LHC components. Improved alignment using FRAS allows the number of corrector magnets required to be reduced, while the possibility of remote alignment also reduces the radiation doses for surveyors working in the tunnel.

This motion application is characterized by less stringent timing requirements than for the LLCS, but instead has a large number of axes (~90) requiring controlled from a central location.

The architecture is based on a central PXIe based SAMbuCa front-end and 3 or more expansion chassis, controlling up to 90 motorized axes per system. Each system is equipped with stepping motors, resolvers, limit switches, and possibly force sensors. The low-level control/acquisition task (i.e. stepping axis motion control, position sensor acquisition, and load cell acquisition) will be distributed among the DI/OT expansion chassis and orchestrated from the PXIe master. Each DI/OT chassis can independently control up to 32 stepping axes and acquire 32 resolvers. However, we will install 16x2 stepping motors drivers in two separate DI/OT chassis to better balance the load on each system over time.

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SUMMARY

This paper has described the new hardware and software framework, SAMbuCA, foreseen for precise critical motion control applications at CERN. The framework is currently under development and many of its building blocks have reached the validation stage. Mass production will start end of next year. After LS3, more than 1200 motorized axes will be controlled with SAMbuCA.

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