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THE MICRO-SERVICES OF CERN'S CRITICAL CURRENT TEST BENCHES

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Abstract

In order to characterize the critical-current density of low temperature superconductors such as niobium–titanium (Nb-Ti) and niobium–tin (Nb_3Sn) or high temperature superconductors such as magnesium-diboride MgB_2 or Rare-earth Barium Copper Oxide REBCO tapes, a wide range of custom instruments and interfaces are used.

The critical current of a superconductor depends on temperature, magnetic field, current and strain, requiring high precision measurements in the nano Volt range, well-synchronized instrumentation, and the possibility to quickly adapt and replace instrumentation if needed. The micro-service-based application presented in this paper allows operators to measure a variety of analog signals, such as the temperature of the cryostats and sample under test, magnetic field, current passing through the sample, voltage across the sample, pressure, helium level etc.

During the run, the software protects the sample from quenching, controlling the current passed through it using high-speed field programmable gate array (FPGA) systems on Linux Real-Time (RT) based PCI eXtensions controllers (PXIe). The application records, analyzes and reports to the external Oracle database all parameters related to the test.

In this paper, we describe the development of the micro-service-based control system, how the interlocks and protection functionalities work, and how we had to develop a multi-windowed scalable acquisition application that could be adapted to the many changes occurring in the test facility.

INTRODUCTION

The upgrade project for the Large Hadron Collider (LHC) aims to achieve higher luminosity [2], necessitating the use of superconducting magnets with higher magnetic fields, for which Nb_3Sn was chosen as the conductor material of choice. It's worth noting that Nb_3Sn is more brittle and challenging to manufacture into cables compared to the Nb-Ti conductor material used in the current LHC magnets.

Additionally, this high luminosity LHC project (HL-LHC) includes the installation of eight Superconducting Links (SC) comprised of high-current magnesium diboride (MgB_2) cables cooled by helium gas, and connected to rare-earth-barium-copper-oxide (REBCO) cables that can operate at 60K [3].

To ensure the proper assembly of these various wires and tapes, especially for the creation of Rutherford cables for magnets and round cables for the SC Link, comprehensive characterization of these materials is crucial. The critical-current density (J_c) is the main parameter for assessing superconductors, and depends on various factors such as temperature, strain, and magnetic field. The most effective method for measuring the critical current is the transport method [1], in which current flows through the sample, and the voltage is measured along its length. A typical result of such tests is illustrated in Figure 1.

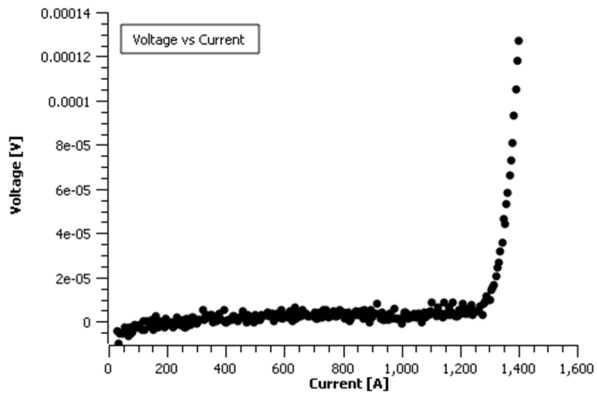

Figure 1: Plot of voltage vs. current for a typical superconductor sample measured at CERN.

To compare different superconductors, the critical current (I_c) is divided by the cross-sectional area (A) of the conductor, defining the critical current density (J_c) [1]. The selection of the area and other methods for calculating critical current density fall beyond the scope of this article.

Historically, four small cryostats were employed to test the critical current density of superconducting strands, while one large cryostat, FRESCA (Facility for the Reception of Superconducting Cables), was dedicated to characterizing the critical current of superconducting cables.

The existing measurement systems used in these test benches had become outdated, relying on older computers running SELinux and LabVIEW® 2012. Furthermore, the need to incorporate systems for characterizing High Temperature Superconductor (HTS) tapes and the introduction of a new FRESCA2 system prompted a renovation campaign in 2020. In this paper, we will elaborate on the new demands and the developments associated with this campaign.

RENOVATION CAMPAIGN

The diverse range of measurement equipment already in existence most of them delivered by NI, much of which has been calibrated during previous measurement campaigns, often relies on fixed and challenging-to-replace power converters. Consequently, it was determined that employing PXIe chassis as the primary platform, coupled with NI

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embedded controllers running the NI Linux RT operating system, would be the most suitable approach.

The PXIe platform can be configured with NI field programmable gate array (FPGA) cards, which support high-speed analogue inputs and outputs, along with digital lines that can function as digital inputs or outputs. These capabilities are vital for both reading and configuring the status of the system, facilitating seamless communication with the instrumentation.

Voltage Measurements

Because of the low voltage across the sample during the tests, measured in the range of μV-mV, the most important measurement device is the high sensitivity nano voltmeter (NVM) connected as shown in Figure 2.

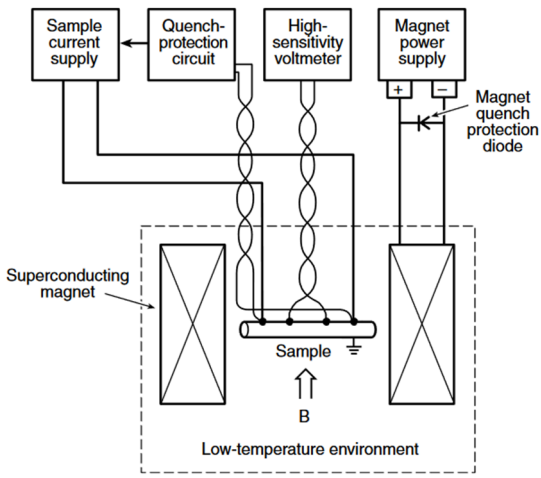

Figure 2: Critical-current density measurement instrumentation diagram. [1]

Achieving the required precision at the necessary readout speed is a demanding task, and there are only a few vendors on the market capable of meeting these stringent criteria. In this context, the Keithley® 2182A was chosen primarily due to its exceptional attributes, including low noise and high repeatability [5]. Nevertheless, the measurement system is designed to offer full compatibility with various instrumentation options, including alternatives such as the Keithley® 182 or instrumentation from other vendors.

For measurements that necessitate lower precision but demand a faster response, NI FPGA cards equipped with amplified, 16-bit resolution analogue inputs were employed. These transient readings are frequently employed to detect phenomena in the samples under examination, particularly when specific parameters such as heat treatment have been altered, however, it is important to note that they are not typically utilized for quality control of superconductors.

Sample Protection

As shown in Figure 1, the transition speed of the superconductor is highly reliant on the current ramp rate. Given this, the sample protection system must react as fast as possible to prevent any potential burning or damage to the sample.

As such, an algorithm for quench protection was implemented on the FPGA. This algorithm collects data from the analogue input, eliminates 50 Hz noise from the measurement data using a notch filter, calculates a moving average (with up to 2000 points to achieve a rate of 1 point per 1 microsecond), and incorporates a deadtime typically set at 50 microseconds. The deadtime serves to eliminate spurious data points that could lead to premature halts and incorrect measurements. Importantly, all these parameters are configurable via dedicated interfaces and files, allowing system experts to fine-tune the settings.

It's worth noting that FRESCA utilizes the Universal Quench Detection system (uQDS), a standardized protection system developed at CERN [7]. This system offers similar features to the sample protection system. Since FRESCA also relies on uQDS for some of its magnet protection, a specialized version of the control system has been developed incorporating control and configuration of the uQDS system. The protection of superconducting magnets is not in the scope of this article.

Current Control

Many of the test benches utilize TDK-Lambda® power supplies. However, FRESCA uses Danfysik® based power supplies, interfaced via CERN's internal Function Generator/Controller (FGC). Additionally, one of the HTS test benches is equipped with batteries capable of delivering up to 1000A.

To effectively control the power supplies, a specialized algorithm has been implemented on the FPGA. This algorithm operates by adjusting the current based on a reference voltage value sent through the analogue output. This approach not only facilitates the potential replacement of different power supplies in the future, as it is supported by most vendors, but also enables the implementation of step and hold algorithms for precise control.

However, it's worth noting that since Danfysik® power supplies can drive currents of up to 32kA and the analogue output provides only 16-bit resolution, a different method for power supply control was configured for FRESCA. In this setup, the control cycle is transmitted via the CERN Controls Middleware (CMW) to the FGC, which subsequently communicates through a WorldFIP fieldbus with the power supplies to deliver the correct current reference at the precise time. This synchronization is achieved through the use of standard CERN timing cards.

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Other Measurements

Figure 3: Ic Test bench control rack.

Cernox® sensors have been installed to measure the temperature within the cryostat, and these sensors are seamlessly interfaced with Lakeshore® 224. This choice was made primarily due to the Cernox® accuracy and its ability to withstand magnetic fields, which is crucial in the context of the experiment.

Furthermore, the measurement system is designed to manage additional cryogenics data such as pressure and helium level. These parameters are monitored by external PLC (Programmable Logic Controller) systems that have been custom developed at CERN. The measurement system subscribes to these PLC systems via CMW (Controls Middleware).

The measurement system plays a pivotal role in overseeing the current supplied to the magnet, which is instrumental in determining the magnetic field. This current monitoring is facilitated by a DCCT (Direct Current to Current Transformer), which is connected to the NI DMM (Digital Multi Meters) cards as shown in Figure 3. Additional DCCT provides feedback on the current being applied to the sample.

The measurement system is versatile in handling various types of data. For instance, it can monitor strain using a DAQ (Data Acquisition) card, as well as manage digital inputs and outputs through industrial DIO (Digital Input/Output) cards or Counter cards. This flexibility allows the system to capture and process a wide range of information pertinent to the experiment.

In terms of control, the system takes charge of regulating the magnetic field through various types of magnet controllers while simultaneously verifying the status of the magnetic field to ensure optimal experimental conditions.

SOFTWARE

The FPGA cards are mainly implemented using LabVIEW® and the LabVIEW® FPGA module. Python 3.6 is also used for scripting and to facilitate automatic analysis of the measurements.

The orchestration of the tests can be split into two components: a microservices application manager running on the Real-Time target, which is responsible for conducting the test, and a client application housing the graphical user interface (GUI). The GUI aims to streamline the operation and workflow of the test bench, enhancing the experience for operators, as illustrated in Figure 4.

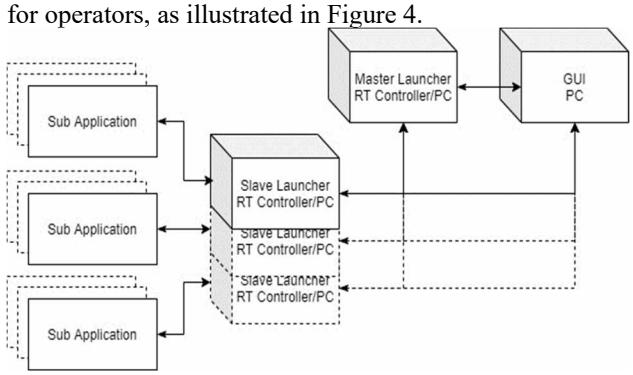

Figure 4: System overview.

Architecture

The software industry has undergone a significant transformation. In the past, developers favoured monolithic architectures tailored to address specific problems for which applications were designed. In contrast, modern industrial systems, comprising numerous interdependent instruments, rely on multiple autonomous processes operating independently. This programming architecture is commonly referred to as microservice architecture.

Given that critical current test benches encompass a diverse array of unrelated instruments, and for enhanced security, it was decided to adopt a microservice architecture for the real-time target application development.

However, there is a constraint with NI Linux RT, which allows only one LabVIEW® application to run at a time. This limitation posed a challenge for developing standalone services on a single target. To circumvent this issue, a primary application, capable of compilation and execution on any Intel x86-based target, functions as both a launcher and a repository for all sub-applications that it launches or depends on. This launcher can operate as either a node or a master. All node applications automatically report their status to the master, as defined in the configuration files. This setup allows certain modules to run on multiple distinct targets connected within the same network. For instance, the FRESCA test bench comprises a PXIe controller serving as a master, six PC-based nodes interfacing with uQDS, and two CompactRIO nodes controlling the interlock chain.

All modules can be controlled using a set of commands, transmitted through TCP as ASCII or via CMW. TCP communication was introduced to streamline internal messaging among modules operating on the same target and to accommodate tests conducted outside CERN (a local network is required in this case since the data is not encrypted). The system is designed to easily incorporate new communication types by creating additional child classes that override relevant methods.

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This approach offers several advantages. Each module can be independently tested, and it simplifies the development of the client application, which can reuse the same methods to access and subscribe to data on the targets. This flexibility proves invaluable for critical current measurements, as it enables swift implementation of new types of instruments.

Framework

To simplify the implementation of the microservice architecture the development was based on an existing framework. Over the years, the LabVIEW® community has proposed many frameworks, with two becoming dominant: Actor framework based on Actor model, and Delacor Queued Message Handler (DQMH®) based on event-based producer consumer design. Since DQMH® comes with scripting tools creating testers and permits users to create their own templates, this framework was used as the main design concept in the application.

The DQMH® framework had to be adapted to permit triggering events via the network, hence a separate communication submodule had to be lunched before any DQMH® module.

Object Oriented Programming

LabVIEW® 8.2 introduced object-oriented programming (GOOP) to build modular and scalable applications and made it possible to abstract similar instruments into hardware abstraction layers (HAL) [4]. This programming design makes it easier to replace or add instruments as the core functionality stays the same through the abstraction layers. For example, the module responsible for measuring the voltage across the sample can use DMM or NVM from many vendors, and if needed any data acquisition card measuring voltage can be used which can be done just by creating a new class and overwriting a few methods.

Real-Time Target Application

Different test benches control different hardware modules. For instance, the HTS test bench lacks a magnet control module, as it doesn't involve superconducting magnet control. However, every master module must run the login manager module to be recognized correctly by the GUI client application. This module plays a crucial role in ensuring that only one operator can control the software at a given time. While many clients can monitor the test bench(es) simultaneously, a new operator seeking control must demote the previous one to a monitoring role.

Several modules are indispensable for ensuring smooth operation of the critical current test bench. These include the sample protection module, the sample power controller module, and the DMM manager module, responsible for managing readings from all DMMs/NVMs. These modules must always remain operational to protect the test system and its samples.

The standard configuration of the test bench would allow operators to measure only one sample at a time, which is impractical for tests conducted at CERN. Typically, several experiments and tests are performed to ensure the quality of the superconducting cables. At least two samples are measured in parallel: the extracted sample taken from the cable after production to qualify the latter and the virgin strand to qualify multifilamentary billets [8]. Conducting two separate cooldowns for these samples would be operationally expensive and time-consuming, therefore the microservice framework has to be flexible enough to run in multiple configurations.

To address this challenge, the concept of the sample control channel was introduced. A specialized module can be launched to track the preset sample number, which is then broadcast over the network. Other modules, such as channel information modules, subscribe to this number and assign correct sample information to the control channel number. The input data for the samples is retrieved from an Oracle database, identified by the operator-specified group ID before initiating the test. Furthermore, the channel information module manages the matrix card, adjusting its channels to predefined presets based on the test type. This card is linked to the NVMs and the analog channels of sample protection. The channel information module broadcasts all its data over the network.

Another critical module that listens to the sample control channel is the digital output module. It activates concurrent digital output channels connected to the industrial card or the counter card corresponding to the specified control channel number. These digital outputs are used by the current switches to ensure correct current flow through the respective sample during the test. Some test benches can measure up to 10 samples during a single cooldown.

All other modules connected to the matrix card must subscribe to the control channel number to notify subscribers of changes in the generic data name, which publishes the measured parameters to the operators.

In addition to the sample protection, the test bench is protected by digital signals coming from multiple systems. These signals, such as the cryogenic conditions, cooling water temperature, or air pressure for the current distribution rack, are handled by different instruments. The FPGA module considers the state of the whole interlock chain and protects both the system and the samples. The other digital signals that are routed outside the FPGA are connected to the industrial I/O or counter card. These signals are monitored by an interlock security module. This module, as with the FPGA, also creates its chain of interlock signals which control the interlock relays. All main interlock signals are also physically chained by relays and redistributed to other systems where needed.

Every software module that measures physical signals also publishes a set of descriptive metadata, such as header values, units, names, timestamps, and aliases. This data is transmitted across the network and published at a regular interval. Subsequently, this information is read by the log module, which stores the measurement and interlock data in binary TDMS files. These files are then transmitted to an external cloud storage system at CERN known as EOS via the files uploader module. The saving process is initiated and halted based on conditions created by the condition manager module. This module subscribes to the same

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data as the saving module but solely checks whether specific conditions specified by the operators have been met. In the case of critical current measurements, the most common condition to trigger measurements is when the current exceeds 5 A.

Host Application

The user interface application can be compiled and run on any Intel x86 based computers running Windows or Linux operating systems. At the start of the application the software requires users to enter correct credentials for the operation or monitor as shown on Figure 5.

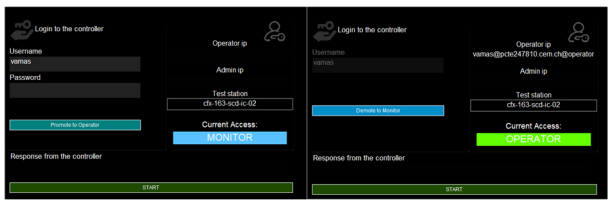

Figure 5: Login module a) before entering correct credentials b) after entering correct credentials.

When correctly logged in, the software subscribes to the master launcher to obtain information of each module running on any of the controllers. If found, it tries to establish communication with all data channels as well as to the channel information. The master launcher also publishes the information about the host panels allowed to operate selected test bench, to block the possibility of operators controlling the hardware that is not connected to the specific test bench.

If all the conditions are met, the software opens all host config files which location is connected to the account. The software is reading and checking the files to verify that all data channels specified by the operators exist on RT application and highlights those that are not valid.

The software continuously analyses which modules are allowed to run by the type of operation, for example user monitoring the test bench should not be allowed to run the power supply panel, and if user is demoted during the operation, it should close operational and configuration panels.

Assuming that operation conditions are correct the test bench shows the main panel which is just used as a launcher of the host panels and the logger of the statuses of RT application.

All the users can run monitoring modules such as time value plots, or time value saving modules, where the users identify signals to plot or to save. The operators can run modules to show sample power, magnet power, interlock security control or control channel to have a full control of the program during the test. They can also run modules responsible for the sample information to select the correct group of samples dedicated to the test, as well as a matrix panel to specify combinations of the measuring channels. The program also supports fully automated tests run via a sequencer. To fully automate tests, the users must select current cycles and give them a number, the same for protection values, and signals used for analysis. Afterwards the users identify the magnetic field and other values, and can start the sequence. Every step is monitored by Analysis which checks if the line of the sequence can be validated. If not, the measurement is repeated if needed. The analysis panel with sequencer is shown in Figure 6 and 7.

Figure 6: Sequencer panel

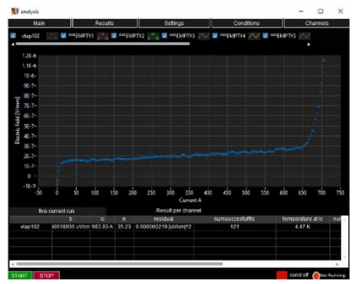

Figure 7: Analysis panel.

CONCLUSION

The microservice based software for characterizing superconductors has been successfully implemented, commissioned, and deployed at CERN. It can effectively evaluate both low-temperature superconductors such as Nb-Ti and Nb_3Sn, and high-temperature superconductors such as MgB_2 or REBCO, both before and after the production of superconducting cables.

The automated nature of these tests empowers operators to conduct more tests and, consequently, evaluate a larger number of samples. These automated tests now perform the stable testing of approximately 200 measurements per day.

Integrating additional hardware into the system is now a straightforward process via the GOOP based scalable architecture and abstraction layer. In case of any issues, each submodule can be independently tested, helping identify and resolve potential problems. Currently, the application has been operational for a year without any significant disruptions affecting its performance.

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