WP/iw

MPS/SR/Note 73-38

16.11.1973

# NEW RF ACCELERATING SYSTEM:

# THE PLUG-IN "AVC" (No. 5)

W. Pirkl

## 1. Introduction

The building blocks composing the Automatic Voltage Control (AVC) are concentrated in one NIM plug-in. The aim of this subsystem is to keep the envelope of the RF voltage across the gap at a programmed value despite of distrubances like beam load, ripples in the feeding line, changes of the ferrite losses (due to frequency, temperature, power level etc.).

It consists of (see Fig. 1) :

- a precision amplitude detector which senses the RF envelope at the distant cavity;

- the feedback system which compares the amplitude information from the detector with the programmed reference value; the error signal is amplified in an equalizer whose correcting networks assure the stability of the loop;

- an RF modulator which acts on the input signal coming from the beam control system. The RF is modulated according to the error signal and in addition passed through a gate to assure a fast switching-off;

- the accessories which form the interfaces for the analog signals and for the interlock.

These subgroups are discussed in the following paragraphs; the block diagram of Fig. 2 gives a more detailed view and the overall scheme is given in Fig. 3.

## 2. The RF Detector

### 2.1 Required Performance

Under the assumption of a high gain in the feedback loop, the precision of the detector determines the precision of the RF amplitude across the gap. The specifications of the system [1] dictate ± 2% deviation down to an RF amplitude of 5% of the nominal voltage; hence a very linear detector with a dynamic range of at least 26 dB is required for the frequency range 2.5 - 10 MHz. In addition, there should be a negligible phase shift between the RF envelope and the corresponding output signal up to a modulation frequency of 20 kHz, the envisaged unity gain crossover of the servo [1] .

The simplest solution would have been a diode mounted directly on the cavity, working at high impedance in the linear range. In this special case, an exception from the general philosophy "no radiation sensitive equipment in the ring" would be feasible in view of the low cost of such a diode which could have been replaced by routine after a few runs. However, a precise sample of the RF at the gap is anyway needed in the central building for the phase control loop

a system much too complex and too costly to be mounted on a throw away basis in the tunnel. Therefore, the use of a remote detector seems more advantageous.

At the end of the matched cable, the 100% RF level is in the 0 dBm range for reasons of the broadband probes. Normal diode circuits turn out to be much too non-linear as AM detectors at this level, even when imbedded in feedback linearizing circuits. Therefore the synchroneous detector approach now used in many high quality communications equipment has been choosen. D. Boussard designed the prototype circuit.

## 2.2 The Circuit

The heart of the demodulator is a multiplier MC 1596 used as a controlled polarity switch; its transfer function is switched from + V to - V for every half wave (Fig. 4 ), so that the output is a full wave rectified signal with a DC value proportional to the amplitude of the incoming RF sinus. Since the switching is controlled by a high performance limiter and not by the crossing of a diode turn-on voltage as is a conventional full wave rectifier, excellent linearity and stability are achieved.

The incoming RF (Fig. 3) is split into two paths :

- the signal path, formed by C2 and a cable with a delay of 13 nsec (the same delay as in the lower amplifiers), terminated in R 13. The signal to be rectified is thus single ended on pin 1 of the multiplier, the second signal input pin 4 is on AC ground but at the DC level controlled by trimpot R 10 to minimize the direct feed-through to the output;

- the control path going via C 1 in the high impedance input pin 3 of the first limiter MC 1035. After 2 further amplifier/limiter stages the signal is fed via C 5 in the control input 7 of the multiplier and its push pull counter part pin 8 tied to the same DC potential by R 22.

The symmetry of the square wave at the output is controlled by the DC feedback loop R3, R2, R1 and R5 with the reference set by R7. A single circuit MC 1035 contains three individual limiting amplifiers, especially designed for this purpose; cascading these three stages directly results in self oscillations at UHF frequencies which increase considerably the noise level at the rectified output of the detector. Putting a second IC with decoupled supply voltage eliminates this problem at the expense of 3 unutilized amplifiers.

The gain of the multiplier and thus the conversion factor AC/DC is set by trimpot R18. The full wave rectifier signal appears push-pull at pins 6/9, any DC offset of the chain is compensated by proper setting of R23.

The filter C8/C9, L3/L4, C10/C11 eliminates the RF components which would overload the input of the buffer amplifier 741.

The circuit has an overall error well below $\pm$ 1% FS down to RF levels of 5%. The dynamic behaviour is characterized by a pole at 450 kHz and a time lag of $\sim$ 170 nsec and does not impair the overall servo performance.

## 3. Equalizer

### 3.1 Required Performance

In [1] a unity gain crossover of 20 kHz together with a DC gain of > 40 dB is specified. After the prototype measurements a unity gain frequency of 50 kHz seemed attainable and was therefore given as goal in the specifications of the invitation for the tenders [2]. After some experience with the final system, however, the very first specification is more realistic due to

- cable delay
- ferrite Q variations
- cavity detuning

limitations which are briefly discussed in the following sections.

3.11 Cable Delay

As a consequence of the centralized system, the time delay in the cables between the ring centre and the cavities is twofold involved and results in a total lag of 2.43 μsec (including amplifiers); this figure is the essential limitation for the performance of the servo due to the introduced excess phase .

Assuming that the closed loop gain should not increase near the cut-off frequency by the μβ-effect, then a phase margin of $60^{o}$ is necessary corresponding to $120^{o}$ total phase shift. Since $90^{o}$ are already present in the normal 6 dB/oct. configuration due to single pole rolloff, there are only $30^{o}$ available for the excess cable shift. This would limit the maximum crossover frequency to 34.4 kHz in this case.

Inspection of the open loop frequency and phase caracteristics of such an uncompensated servo in Nichols chart shows, however, that the curve touches the permissible borderline for 0 dB μβ effect at only one point near to the 0 dB gain, and that the gain margin is unnecessarily large. Introducing a step network which increases the phase margin at the expense of the gain margin brings considerable improvement. Systematic investigation of several step networks on a desk-top calculator showed that the unity gain frequency can in that way be raised up to $\sim 45^{o}$ cable phase. The optimum configuration in the present case is zero 124 kHz/pole 620 kHz and permits a crossover at 51.5 kHz. Such a step is provided in the equalizer.

3.12 The Ferrite Q determines the load resistance of the final amplifier since the internal resistance of the power tetrode is comparatively high. Any change in the ferrite quality will consequently influence the RF as well as the servo loop gain. Measurements at various power levels and frequencies show a gain variation as high as 8.5 dB together with a variation

in the 3 dB bandwidth between 24 - 64 kHz (Fig. 5 ). It is interesting to note that the cavity response and the corresponding low-pass-transformed servo gain at high loop frequencies (> 100 kHz) is constant, regardless of the "DC" gain of the ferrite; it can be shown that the same correspondence gain/bandwidth holds for arbitrary RF frequency, provided the cavity C remains the same over the band.

In the extreme case where there is very little excess phase shift due to cables, the unity gain crossover can be put in the constant region above the highest cavity rolloff. The servo speed will therefore not be impaired by any imperfections of the ferrite, neither due to temperature nor to frequency. If at the other extreme the delays in the system demand a unity gain frequency of less than the lowest cavity rolloff, than the full variation of the ferrite resistance will be reflected in the resulting servo speeds.

The cavity rolloff is clearly too high in frequency to provide a suitable open loop caracteristic; a leading pole has therefore to be put into the equalizer and the cavity bandwidth compensated by a fixed frequency zero. In the first extreme, this zero could be located at 64 kHz and a unity gain crossover at, say, 400 kHz would again be independent of the ferrite. At the other extreme, the zero had to be below 24 kHz and no automatic trade of gain/bandwidth would occur.

The present case lies between these extremes. Systematic calculations show that the zero can be put up to 34 kHz with moderate suppression of ferrite effects, the unity gain frequencies being 34 and 58 kHz (Fig. 6 ). However, there is already a + 1 dB $\mu\beta$ effect for the lowest RF frequency so that this zero location is the highest practicable.

### 3.13 Cavity Detuning

So far the cavity was supposed to be exactly in tune, this means that the vectors of the two AM sidebands $f_c \pm f_{test}$ ( which are generated

above and below the RF carrier frequency $f_c$ by a servo test frequency $f_{test}$) are always conjugate complexes with respect to the carrier (Fig. 7 ). If, however, the cavity is detuned, the two sidebands are no longer equal, neither in amplitude nor in phase (Fig. 8 ). The locus of all vector end points becomes an ellipse which can be interpreted as the sum of a FM and an AM modulation acting at the same time. The AM component has been calculated for different relative detuning (Fig.9 ) : the gain can be seen to be higher than in the tuned case above a certain modulating frequency, with the practical consequence that the loop becomes unstable if the cavity is detuned. Fig.10 shows closed loop response to test pulses at a detuning of 1.75 $f_{3dB}$ (stable) and at 3.9 $f_{3dB}$ (unstable).

Unfortunately, this is not an unrealistic situation since the present fine tuning system is not yet capable to suppress short tuning errors which may occur in the period of high f (after injection) or during beam gymnastics at the flat top. It is hoped that the ferrite properties will allow to improve the fine tuning speed by an order of magnitude, but at present the AVC gain is simply lowered to avoid oscillations during excessive detuning. Fig. 11 gives the open-loop characteristics for this mode of operation, where the gain is reduced by $\sim$ 10 dB from the normal setting, and Fig. 12 the corresponding pulse response.

An additional step network which increases the low frequency gain of the loop by 20 dB is easily feasible and was therefore included in the design; the upper corner frequency was choosen at 1.2 kHz, far enough from the unity gain frequency to avoid noticeable phase shifts from this 12 dB/octave section. The total equalizer has therefore the following pole/zero configuration :

| Purpose | Pole | zero |
|---|---|---|
| - leading pole | 120 Hz | |
| - step network to increase the DC gain | 120 Hz | 1.2 kHz |
| - cancellation of the cavity rolloff | | 34 kHz |
| - compensation of the cable lag | 620 kHz | 124 kHz |

## 3.2 The Equalizer Circuit

With the given pole/zero configuration, the total gain of the amplifier must be ∿ 80 dB, including a margin for the gain set potentiometer.

Two IC amplifiers with a voltage gain of 100 each are used; earlier versions were build around the 709 type, but their limited frequency response introduced noticeable excess phase shifts already at 50 kHz and were therefore replaced by the faster 702/712 type. However, given the poor common mode input range of these amplifiers, the usual differential input is not feasible to form the error signal. Therefore the resistive divider R 30/R 31 and R 46, R 47, R 48, R 49, R 50 together with opposite polarities for detector and reference amplifier are used instead. R 30 is a trimming resistor to compensate the build-up of tolerances in this divider chain. It is determined during the adjustments with all the other elements already in the circuit (see adjustment procedure). The required frequency response is achieved by the components in the local feedback paths. Since the frequencies of the singularities are quite distant one from the other, the interaction between the components is negligible : R 33 and C 21 determine the leading pole, C 21 and R 34 the cancellation zero and R 34, R 35 and L 11 the step for the cable compensation. Emitter follower Q1 provides the current to drive the gain set potentiometer R 38 and the feedback path.

Special precautions are necessary in the design of the output stage: the signal delivered to the modulator has to be positive under all circumstances since negative voltages would open the modulator illegally with a phase shift of $180^{o}$. In addition, a definite zero equalizer output should be feasible despite all DC drifts, in order to achieve zero RF voltage at the cavity. The local feedback loop is therefore split into two path :

- Q2 together with the step-circuit elements R 40, R 41 and C 27 form the normal local feedback. This path is only operating for positive outputs, when $Q_2$ is conducting.

- D1 and R41 close the local feedback path around the output stage for negative IC outputs. Q2 is off under this condition and presents a zero gain-control voltage to the modulator. Note that the overall loop is then out of operation by lack of RF at the cavity and the working points of the amplifiers are undefined, as the unavoidable drifts of the detector, the reference - and error amplifiers are multiplied by the full gain. A separate path, D1000 and R43, is therefore provided to replace the normal return signal and to prevent the amplifiers from catching at negative polarity. A delay of as much as 20 µsec would result before the AVC loop can react, and it is this combination of diodes D1 and D2 which allows a smooth locking-in at the begin of each machine cycle.

## 4. The Modulator

### 4.1 Requirements

As the RF voltage at the gap can vary by as much as 30 dB, the necessary modulator range is close to 50 dB worst case, since it must compensate all build-in amplitude reserves as well as ripples in the frequency response or non-linearities in the final amplifier. Within this range, the DC/RF conversion factor should be as constant as possible to avoid alterations of the AVC loop gain. Moreover, the RF output phase should not vary by more than $\sim 5^{o}$ so that the individual cavity gets always the same phase, regardless of the RF level.

Circuits with AGC transistors and various configurations of FETS (both in amplifier and in resistance mode) were tried but could not meet the specifications. Finally, a neutralized circuit around a MC 1596 multiplier satisfied all the requirements.

## 4.2 Circuit

Since the modulating process is based on the use of a non-linear caracteristics (in this case the current-dependent transconductance of a transistor quad), the input signal has to be relatively small to avoid the generation of harmonics; input divider R 72/R 86 brings the + 10 dBm RF coming from the beam control down to14.8 mV peak, a level small enough to keep the distortion factor at the output below - 30 dB. The multiplier is driven single ended at pin 8, the corresponding push pull port pin 7 being at the same DC level but at AC ground. From the two gain controlling inputs, pin 1 and pin 4 there is again only one used for the modulating signal coming from the equalizer. The other, pin 1, serves as offset compensator and is fed by potentiometer R 82, followed by the divider R 80/R 81.

The effect of the offset compensation and of the neutralization can best be discussed by the vector diagram of Fig.13. For the untrimmed amplifier, the locus of the RF output voltage lies on a straight line passing at some distance from the centre. For high gain control voltages the output will be in the direction of V $\infty$ but as the control voltage is decreased, the angle changes and reaches $90^{o}$ error for the minimum output. As first step, the offset potentiometer is trimmed until this minimum output occurs at zero gain control voltage. Then the remaining quadrature component is eliminated by injection of an opposite quadrature current stemming from the capacitive divider C 44/C 45, coupled to an output by C 46. Which of the two push pull outputs X or Y is connected to point V depends on the direction of the quadrature stray coupling; the other output should be connected to point V for capacitive symmetry. As a result, the output is typically some 70 dB reduced for zero gain control voltage; the corresponding phase error over a 40 dB- range is $\sim 2^{o}$. Gain linearity deviations are virtually unmeasurable as far as this servo application is concerned (but could be evaluated by some distortion - factor method). Full advantage of the push-pull configuration of the multiplier

is taken by the use of the long tailed transistor pair Q 4/Q 5 of the output to reduce the even harmonics; current generator Q 8 can be cut off by a - 12 V signal at the gate terminal and serves as fast RF gate with an attenuation in excess of 40 dB. The output stage consists of a Darlington pair and is straight forward. Special care was necessary to suppress oscillations in the UHF range, which normally would pass undetected but cause minor random deviations of the multiplier operating point and make a proper nulling impossible. The data sheet of the MC 1596 suggests the suppressors C 48/ R 76 and C 49/R 77 to be used, but this proved unnecessary because of the low impedance terminating resistances already present at these points. On the contrary, the difference amplifier could only be silenced with use of the damping resistances R 90 through R 93 and R 103, R 105, R 109.

## 5. Accessories

### 5.1 Input Reference Amplifier and Limiter

The AVC reference voltage which programms the gap voltage is first passed through a difference amplifier (in the standard configuration) to eliminate cable interferences or to use a negative programming voltage if so desired. A two-stage limiter is provided to clip all illegal peaks to a maximum of 103.5% referred to a programming voltage of 100% ≙ 7.00 V; at 100% programming voltage, the gain compression as set by R 48 is as low as 2%o.

### 5.2 Instrument Driver

There are four instruments per accelerating station to monitor the gap voltage; since they are low impedance and connected via long cables with considerable capacitance, a separate instrument driver amplifier with emitter-follower output is provided. R 120 and R 123 render it short-circuit proof while the relatively heavy compensation R 125, C 70/C 71 assures

stable operation for capacitive loads up to 1 μF.

5.3. AVC Alarm

This fast acting protection device avoids the potentially catastrophic consequences of little sparkovers in the cavity: in case of such a breakdown, the AVC increases the RF drive in an attempt to keep the envelope at the programmed value, and finally puts the full available RF power in the negative impedance characteristic of the arc. The destructive power of 95 kW was involuntarily demonstrated by an arc, initiated from a faulty insulator, which welded a hole of 1" diameter in the aluminium-cast feeder of the cavity.

Any abnormal situation can however be detected by a comparison of the RF drive and the resulting voltage across the gap. This is done in an uncompensated 709-operational amplifier, connected as a comparator. The gap voltage information at the detector output is first inverted in a 741- op amp and then fed to the inverting input pin 4. A fraction of the gain-control voltage, set by potentiometer R113, is brought to the direct input pin 5. If the gain control voltage is too high in relation to the gap voltage, the comparator switches from negative to positive saturation and cuts the RF drive within 10 μsec by opening the RF gate via diode D8.

With the RF gate opened, the RF at the gap is ∿ 100 V max and the detector output drops to about ten millivolts. By contrast, the reference voltage is still at the original value and therefore drives the error amplifier, equalizer and gain control voltage into saturation. The circuit thus latches in the disabled state and needs a special recovery procedure for the automatic lock-in upon the next machine cycle. A reed relay is therefore provided,which is powered by Q3 at the same time as the RF gate; its contact shorts the reference voltage after a trip time of half a millisecond. During this time, control was taken over by the interlock system. The alarm condition was transmitted by R66 / R67 to the "crate interlock" in plug-in # 11 which disables the "release" by going high, keeping the RF gate disabled via R 70, R 69 and D 7.

Transistor Q 3 is thus held saturated even if the local self latching is removed after tripping of the reed relay. A new start follows the normal routine as given by the interlock system.

False alarms would occur during the first microseconds after a positive step of the reference voltage, when the gain control voltage is already positive but no return from the cavity is sensed because of the time delay in the cables. During this time, a detector return is simulated by the differentiator C 33, R 59/R 60; diode D 6 passes only the positive slope in order to avoid sensibilization of the alarm during the fall time of the reference. R 63 provides an offset corresponding to $\sim$ 8% RF voltage across the gap and eliminates uncertainties at zero voltage.

The overall function of the AVC alarm was checked with the aid of test wires, switched between the energized gap and ground by the aid of a high power vacuum relay : copper wires as small as 0.1 mm diameter withstand intact such short circuits at full operating RF voltage.

## 5.4 Test Supply and Test Switches

A stabilized supply formed by zener diode D 10 and output emitter follower Q 9 proved to be useful for test purposes. Two 3 way switches allow open-or closed loop operation with internal or external references and give rapid diagnostics in the case of a fault. The Lemo test connector at the input of the modulator allows the injection of a test signal provided by a separate plug in. The loop gain can thereby be checked at any operating line, in the dead time of the CPS cycle between looking-in of the loop and proton injection.

Acknowledgements

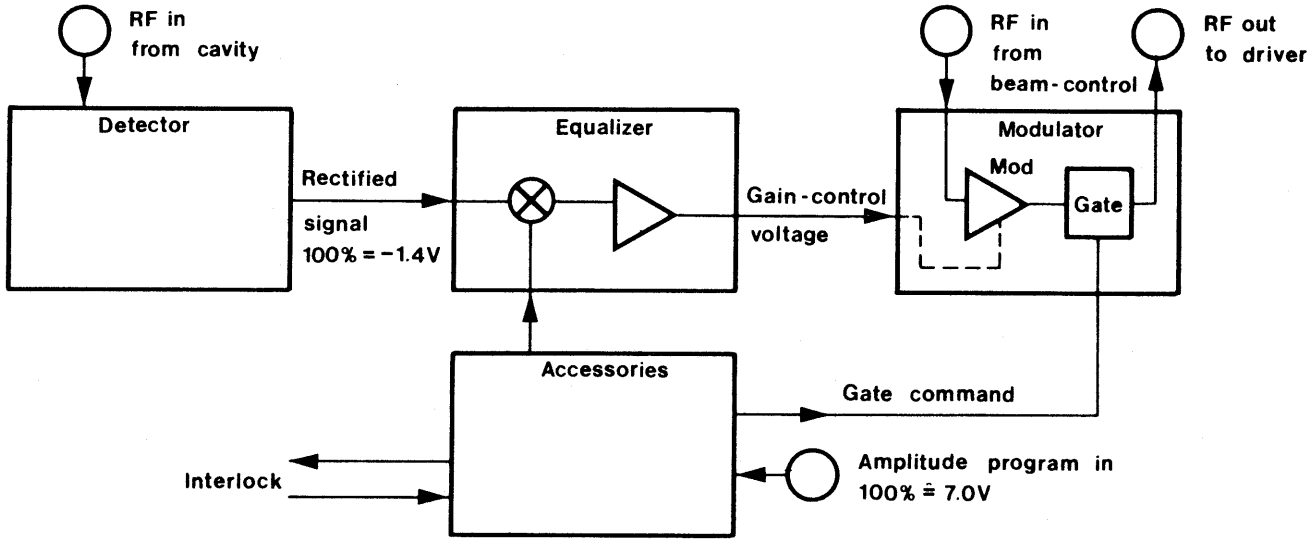
The help of Mr. D. Boussard for the design of the precision detector, Mr. J. Jamseks support in the documentation and H. Herdrichs efforts in testing are gratefully acknowledged.

References

(1) MPS/B Mi 67-11

(2) MPS/SR/SPEC/69-4

FIG. 1: AVC - Plug-in Summary block diagram

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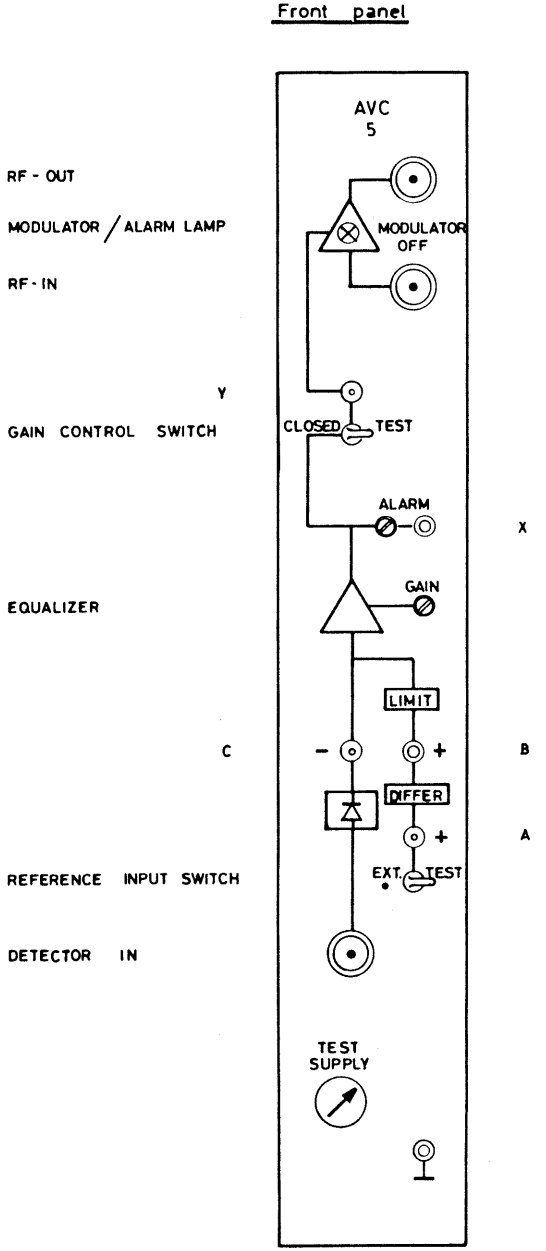
Front panel




AVC Plug in

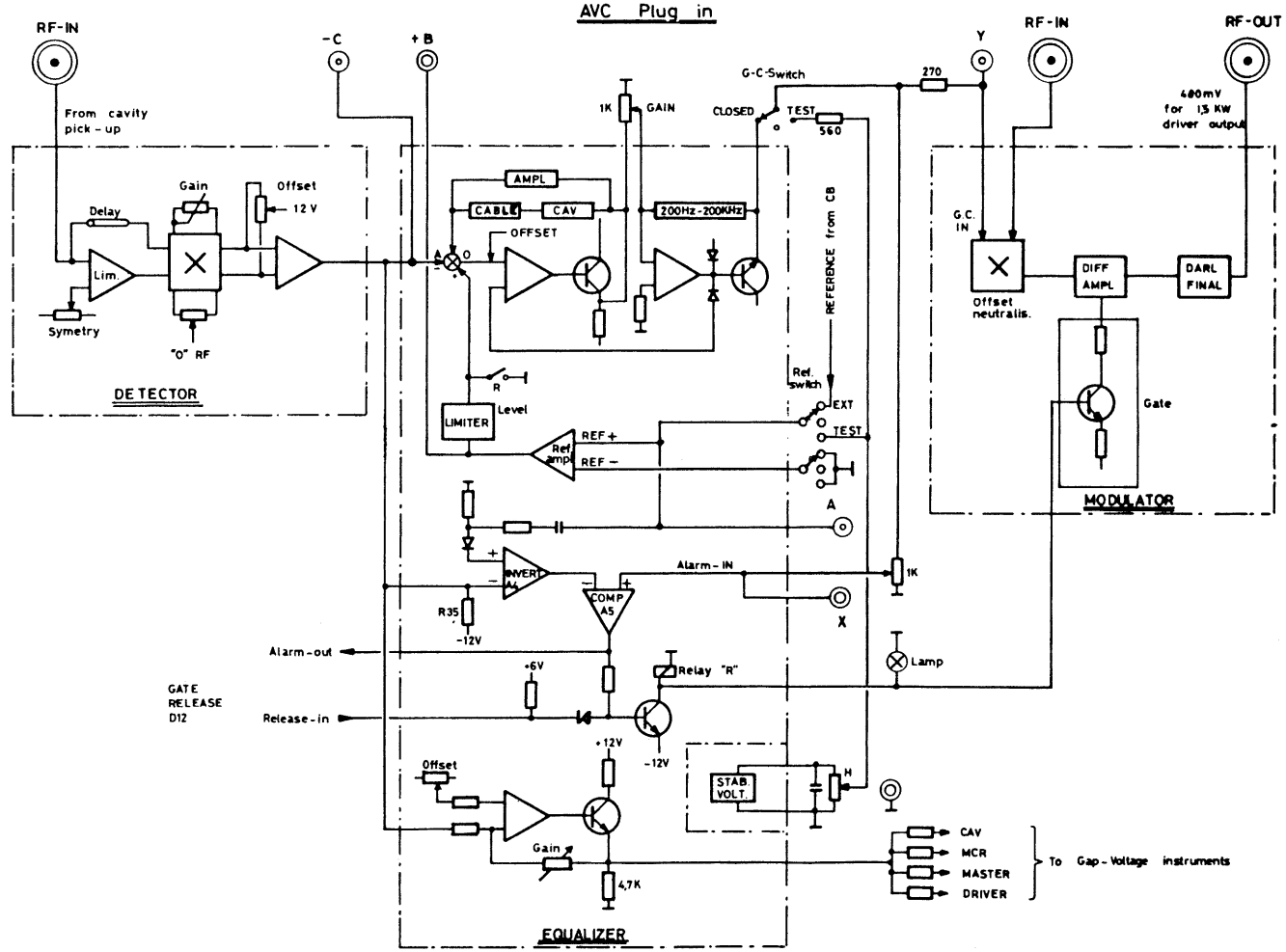



FIG. 2

LED

BNC

LEMO

BANANA

ADJUSTMENT

B - Mise à jour le 13-11-1973

A - Mod. le 21-06-1973

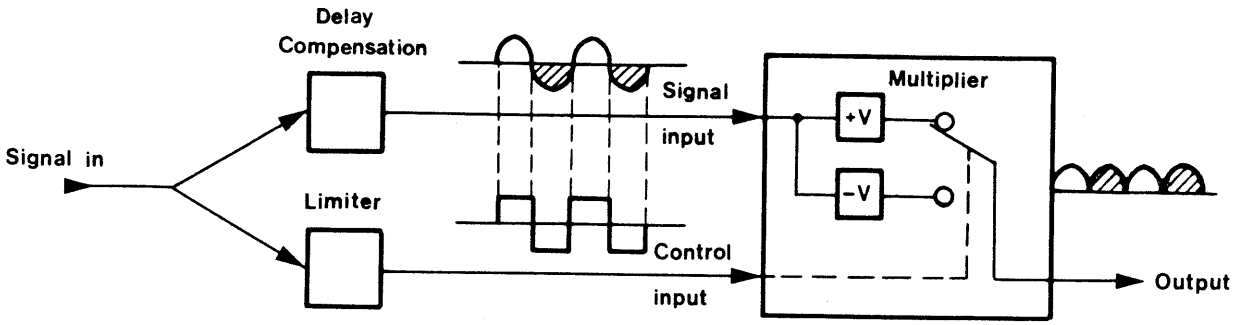
AVC Amplifier
Bloc diagram
Plug in Nº 5

| | | |
|---|---|---|
| DESSINÉ | 26-10-1972 | |
| CONTROLÉ | | |
| VU | | |
| REMPLACE | | |
| REMPLACÉ PAR | | |
| RÉDUCTION | | |

CERN ORGANISATION EUROPÉENNE POUR LA RECHERCHE NUCLÉAIRE - GENÈVE

M.P.S. SR-7330-RF50-3 B

FIG. 4: Principle of the multiplier-detector



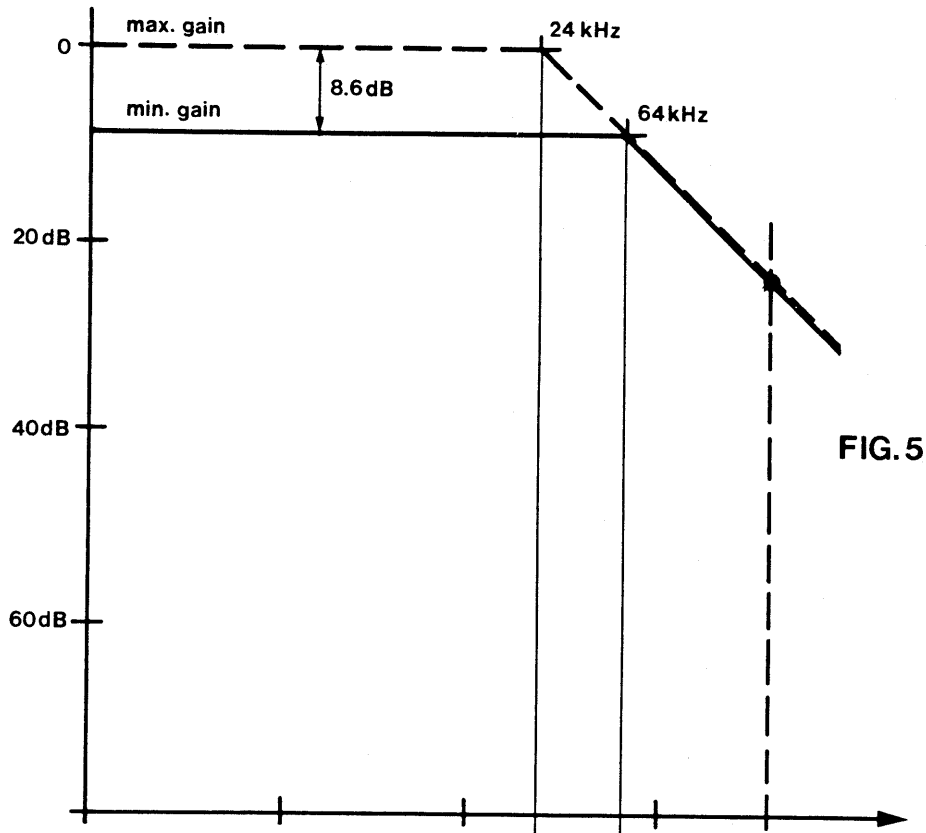




FIG. 5: Broken-line approximation of the cavity rolloff for two ferrite loss resistances

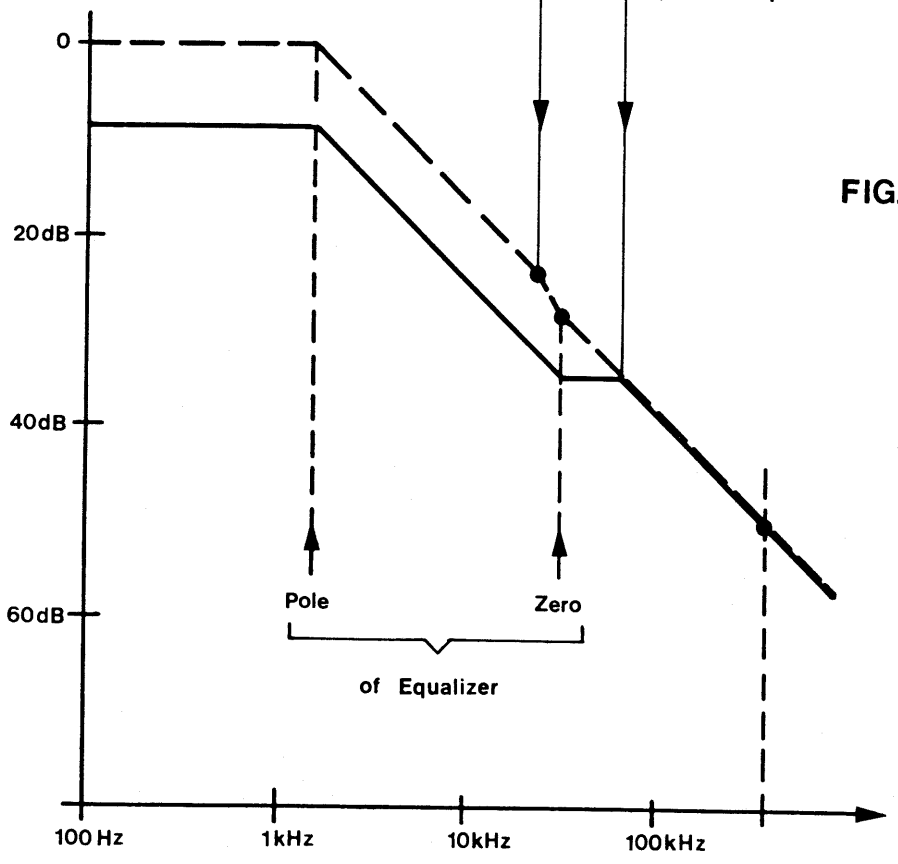



FIG. 6: as Fig. 5, but compensated by a Pole 1.6 kHz
Zero 34.0 kHz

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FIG. 7: Vector diagram for tuned cavity $\psi$ degrees after maximum of drive

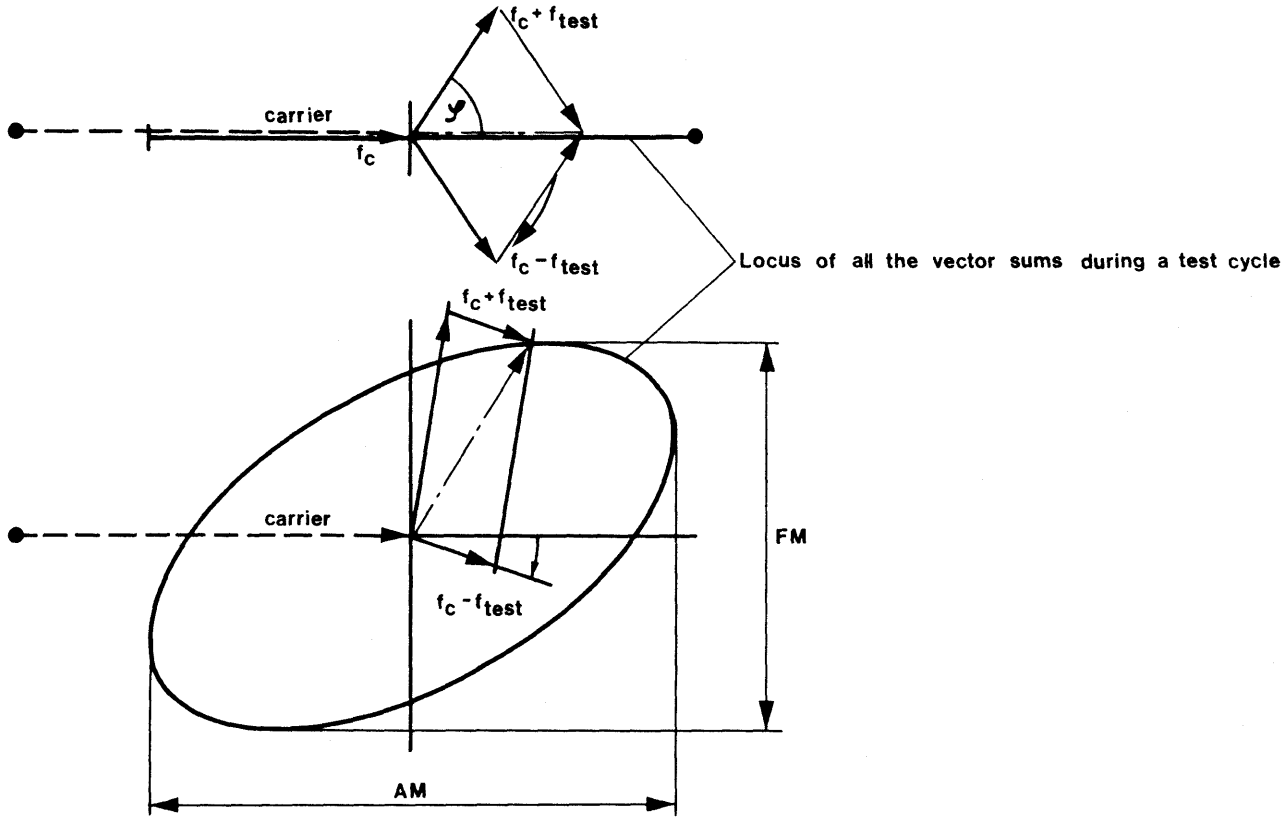



FIG. 8: Vector diagram for detuned cavity

FIG. 13a: Multiplier unadjusted

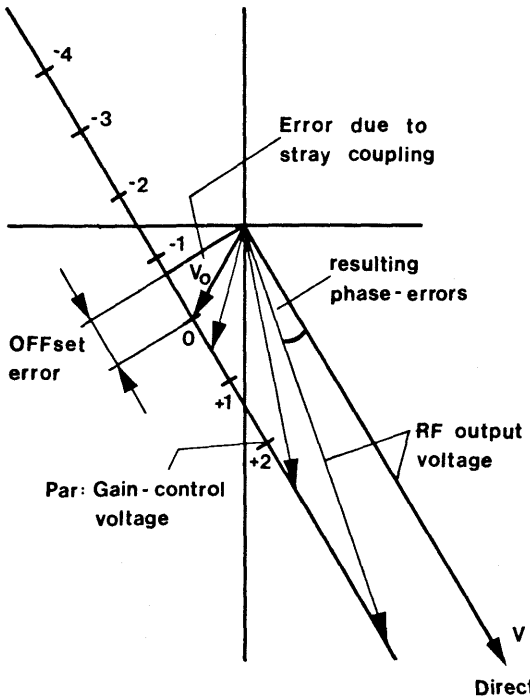



FIG. 13b: Multiplier after OFFsetadjustment

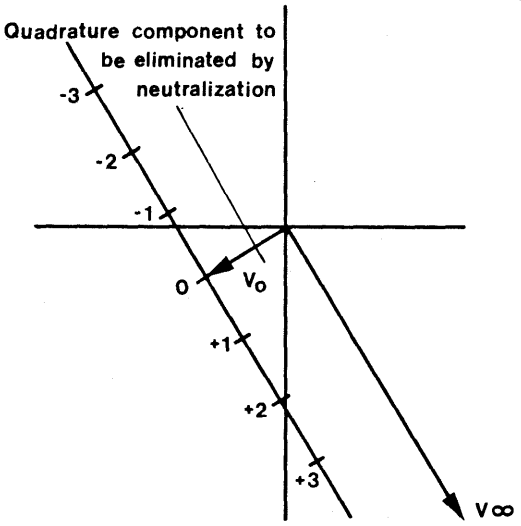
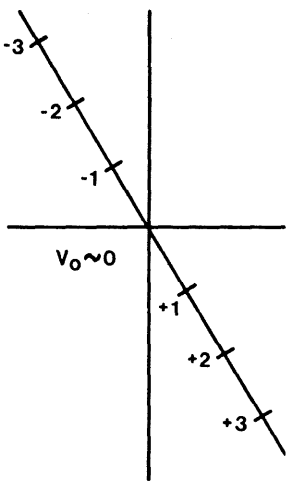



FIG.13c: Multiplier after OFFset and Neutroadjustment

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K-645 17.1.74 Falone

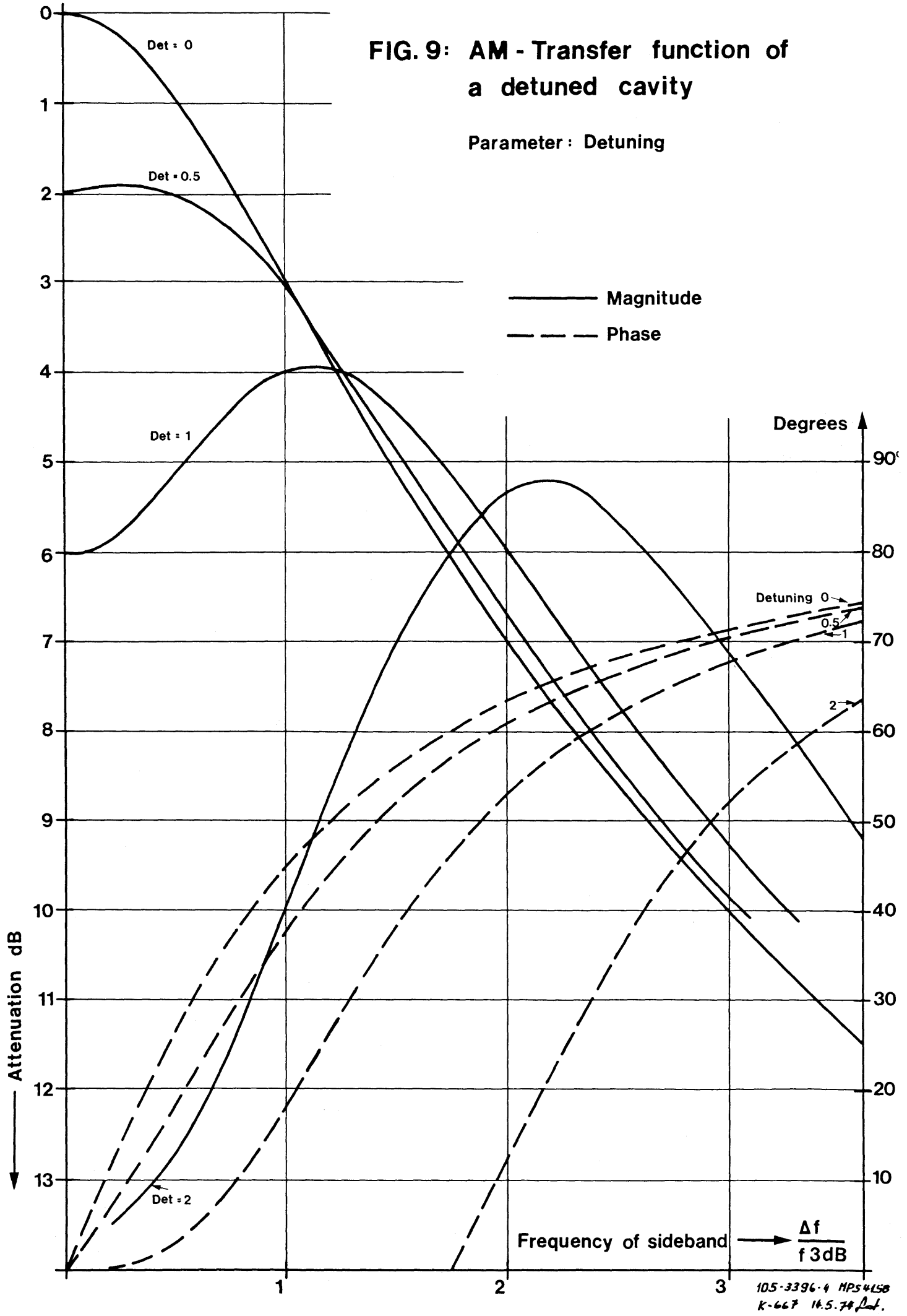
FIG. 9: AM - Transfer function of a detuned cavity
Parameter: Detuning
Magnitude
Phase
Det = 0
Det = 0.5
Det = 1
Det = 2
Detuning 0
0.5
1
2
Degrees
90
80
70
60
50
40
30
20
10
0
1
2
3
4
5
6
7
8
9
10
11
12
13
Attenuation dB
Frequency of sideband → Δf / f 3dB
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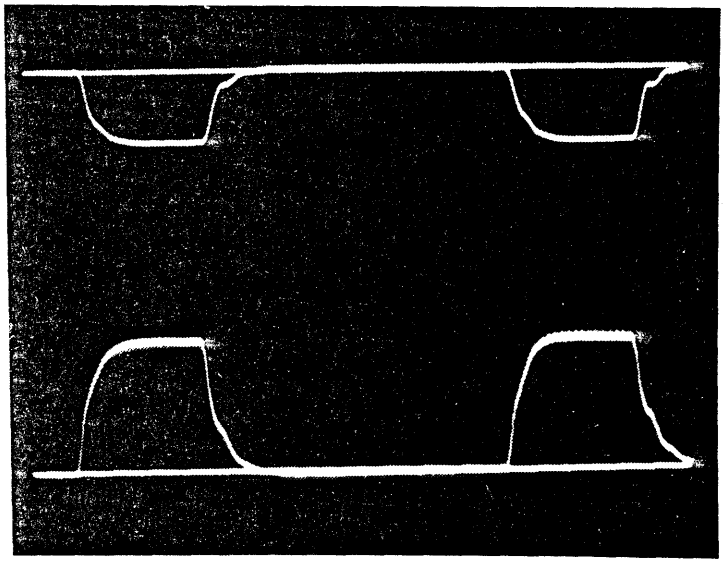
Fig. 10 Closed loop pulse response for detuned cavity
Top trace: detector output (gap voltage) 0.5 V/div ≙ 35.7% RF
Bottom trace: signal at modulator input (gain-control voltage) 0.1 V/div

hor: 50 µsec/Div

Detuning
+ 1.75 $f_{3dB}$

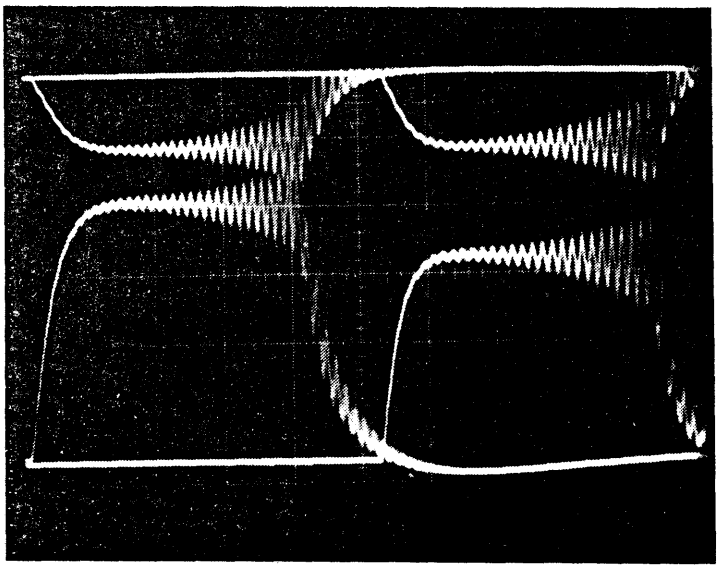
Detuning
- 1.75 $f_{3dB}$



Loop stable

Detuning
+ 3.9 $f_{3dB}$

Detuning
- 3.9 $f_{3dB}$



Loop unstable
Note increase in the gain-control voltage (bottom) to keep the pulse output at the same level as above despite the lower loop gain due to the detuning

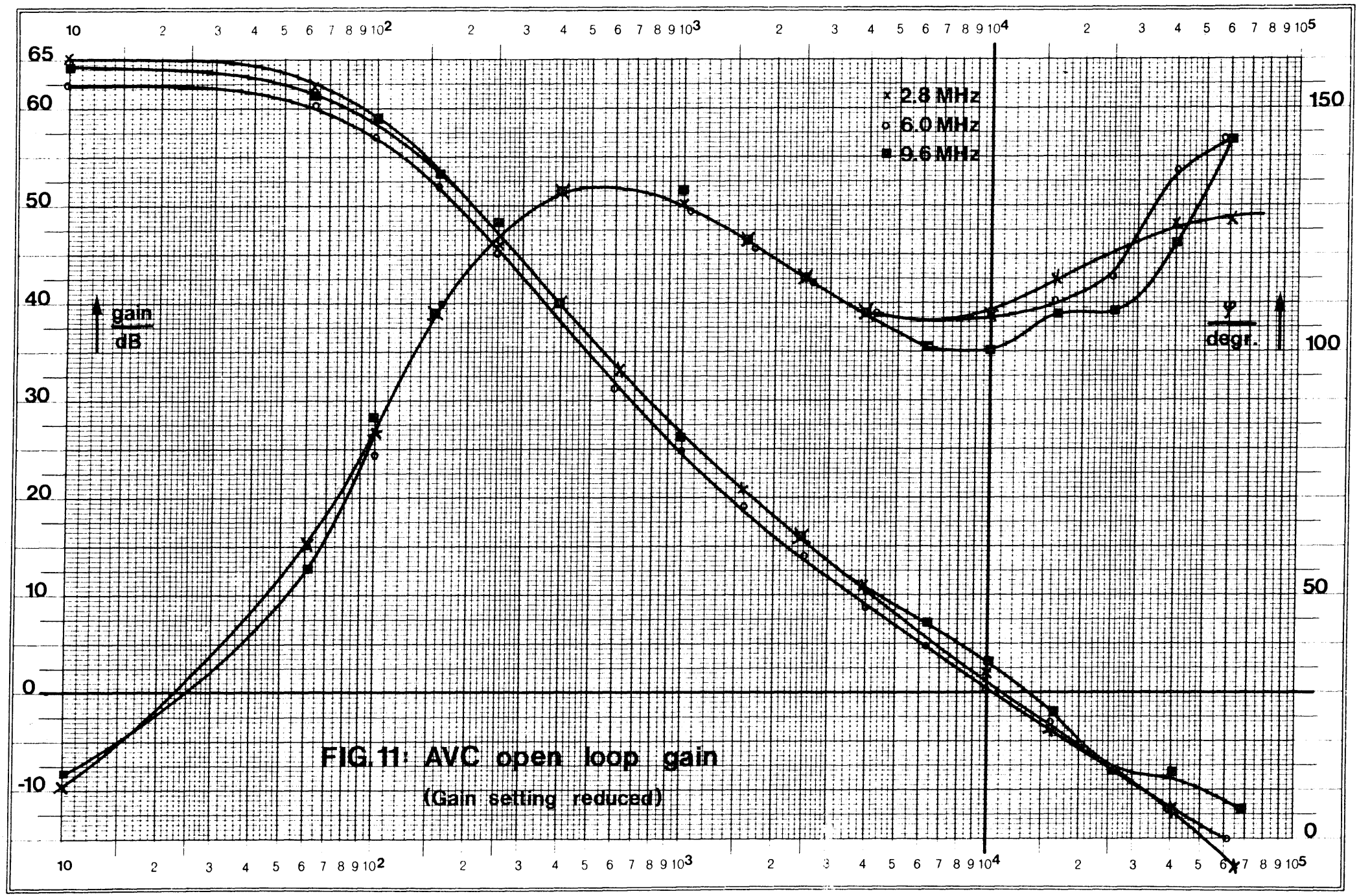



**FIG. 11: AVC open loop gain**

**(Gain setting reduced)**

Logar. Teilung / Division 1-10000 Einheit / Unité 62,5 mm

Ed. Aerni-Leuch, Bern Nr. 526

105-2399-4 HPS 4458

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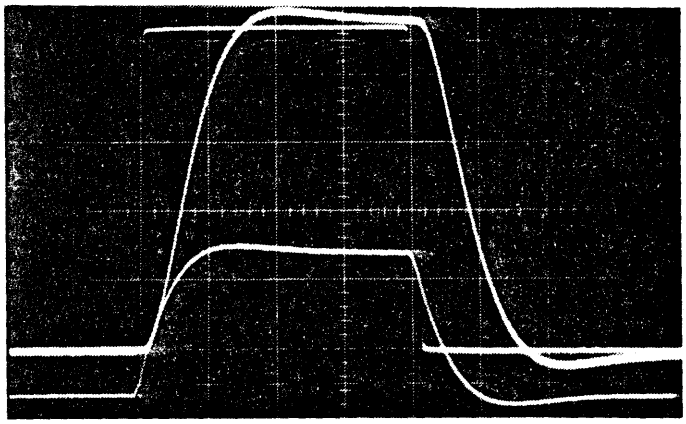
Fig. 12 AVC Pulse Response (cavity in tune, gain lowered) time domain behaviour corresponding to frequency domain data of Fig. 11




OV

f = 2.8 MHz

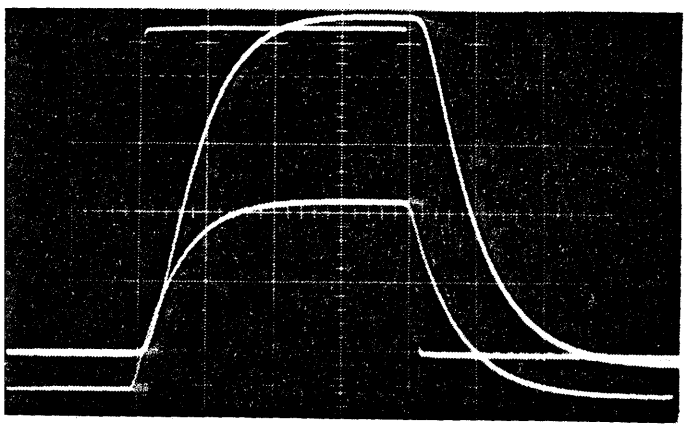
$U_{Det}$ = 100 mV/DIV
(140 mV$\hat{=}$1 kVp)

$U_{Ref}$ = 0.5 V/DIV

$U_{mod}$ = 50 mV/DIV

t = 20 µs/DIV

The overshoot in the output pulse is due to the reduction of the loop gain by which the cross-over occurs at low frequencies with relatively low phase margins.



OV

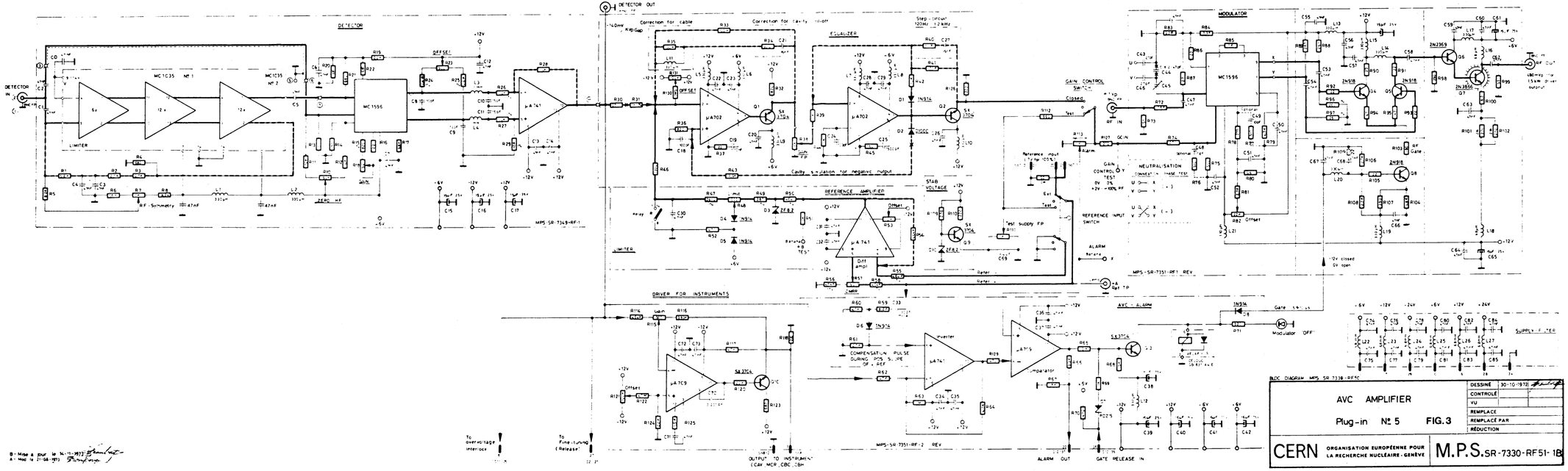
f = 9.6 MHz

$U_{Det}$ = 100 mV/DIV

$U_{Ref}$ = 0.5 V/DIV

$U_{mod}$ = 50 mV/DIV

t = 20 µs/DIV




BDC DIAGRAM MPS SR 7330-RFAC

| | | |
|---|---|---|
| AVC AMPLIFIER | DESSINÉ | 30-10-1972 |
| | CONTROLÉ | |
| Plug-in N° 5 FIG. 3 | VU | |
| | REMPLACE | |
| | REMPLACÉ PAR | |
| | RÉDUCTION | |

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M.P.S. SR-7330-RF51-1B