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PROPOSAL FOR A COMPUTER COMPATIBLE EJECTION TIMING SYSTEM

WITH POSSIBLE FURTHER APPLICATION IN THE PS

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Introduction

The FAK needs an operational computer compatible timing system in early 1975.

In summer 1972 it was agreed with B. Kuiper and G. Plass that I should study the FAK timing problems after the running-out time of the "Fast Ejection Serpukhov" (FES) project and before my departure to the USA. This decision was taken due to a lack of time to study these problems in the FAK section, actually charged with the completion of the FAK H.V. hardware and bringing it into operation.

The study was to be carried out in a general line, considering existing timing systems and new methods. Since the "Fast Ejection Timing" is the most complex in the PS, it can be supposed that its facilities can be used also for other equipment.

On the main specifications of a computer compatible timing system for PS applications the following statements can be made :

- The timing system must be set and checked entirely by the computer.

- It must be built in a modular form for easy adaption to different computer and data transfer systems.

- The different local timing systems of the new type must be independent from each other and from the existing timing systems.

- The new timing system must be insensitive to PS time reference and machine cycle modifications.

- A complete operation and service documentation must be available when the timing hardware is commissioned.

- Manufacturing must be done in a firm which also accepts succeeding orders for the same material over a long time period.

The tight boundary conditions for a fast ejection timing system lead again to the preset counter as the basic timing element. Due to the relative short time at our disposal for manufacturing of prototypes and series, a moderately advanced design philosophy was adopted. To keep the costs low and to shorten the industrial development time, a multipurpose counter card using TTL logic is proposed. The mechanical parts for the crate and plug-in units are standard Camac items but the electrical layout of the crate differs from a Camac crate.

1. Computer comptability of Timing System

The decision to control and operate the CERN proton acceleration and storage system (Linac, Booster, PS, SPS, ISR) with an allied multi-computer system required computer-accessible hardware. The transformation of the existing manually-controlled hardware into a computer controlled one is not merely a question of required effort, but often physically impossible, especially for data intensive electronics. The introduction of data highways for setting and read-out purposes leads to new circuits and mechanical layouts.

The "Fast Ejection Serpukhov" (FES) timing system is a reproduction of the "Operation Straight Flush" (OSF) timing equipment with minor modifications. Both systems would be very difficult to convert to computer accessible ones due to the high density packing of components.

The FES timing system is mentioned because, as a complete manufacturing and up-to-date service documentation is in existance, minimum CERN manpower would be necessary for industrial manufacture for CERN applications.

For other timing equipment still in operation, similar statements are valid.

2. Hardware Back-Up Setting of Timing Systems

A major question arises immediately with the computer integration of a timing system : whether or not it is desirable and possible to have direct manual access to the timing preset counters for emergency cases by by-passing the computer.

It would be an advantage to lay down a general and binding hardware back-up setting philosophy.

A non-homogeneous back-up setting helps little if the process computer breaks down. In such a case, all scheduled equipment should be manually operated for continuing the run properly.

The complexity of the future machine cycle composed of different sub-machine cycles leads to different settings within one super machine cycle (i.e. sequencing with different settings of one and the same equipment in one super machine cycle). Therefore, a simple manual setting will be impossible.

A hardware back-up setting in parallel with the computer setting system represents an important block of material at a substantial cost. These reflections lead straight away to a completely computer-integrated timing equipment without a hardware back-up setting.

3. Computer Integration of Timing Systems

Computer integrated means - the system is entirely set and checked by the computer. All arithmetic operations which are necessary for, e.g. the ejected bunch selection, must be done by the computer, too.

All hardware knobs and indicators are used for local maintenance and trouble shooting. System faults will be detected by the computer and given to a data display where it can easily be interpreted.

4. Timing References

Best operation facilities can be obtained only by a coherent design on all components of a timing system, i.e. all the computer hard- and software, the data transfer and timing equipment and the PS-time references.

This paragraph gives a statement on the actual PS-time references which is followed by some critical remarks and a proposal for slightly modified PS-time references.

4.1 Status of the Actual PS-References

M-Pulse Train

The PS ring magnet is powered by a rotating group, an asynchronous motor and a synchronous alternator on one shaft. The magnetic cycle of the ring magnet is the pilot event for all timing incidents in and around the PS. The angular velocity of the group shaft varies about $\pm$ 2% around its nominal value in one machine cycle. The magnetic cycle length deviates not more than 100 ppm from its preselected nominal value. A disc is mounted on the group shaft containing a marked magnetic tape and symetrically distributed permanent magnets. Magnetic pick-up heads excite 2 continuous pulse trains with mean frequencies of $\simeq$ 300 Hz and 9000 Hz. These pulse trains are especially designed for the ring magnet power supply synchronization. However, the 300 Hz pulse train is also distributed in the PS area. The pulse train is called M-300 train and has a mean resolution of 3.3 ms. Each new machine cycle start is marked with 9 missing pulses in the M-300 train. At the moment, all key machine pulses are referred to one master preset counter for M-pulses which determines the PS magnetic cycle length with a preselectable coincidence (MR). Other machine key pulses (MW, MO, M30 and MS) are generated with fixed coin cidences on the same M-master counter or a sequence of preset M-counters started with the key pulse MS. These key pulses can be commonly distributed all over the PS area (see CERN 71-20 "La Nouvelle alimentation de l'Aimant du Synchrotron à Protons du CERN chapitre IV, by O. Bayard).

B_{up}- and B_{down}-Train

The voltage induced in a measuring coil mounted in the reference ring magnet unit 101 in the reference room is continuously converted into

a B_{up} resp. B_{down} pulse train corresponding to a rising or falling magnetic field in the reference magnet. Both pulse trains can be distributed over separate cables all over the PS area.

The distributed B-trains are stopped with the MW pulse and restarted with the output signal of a peaking strip set at 50 Gauss. Some 10 ms before the peaking strip generates its signal, an artificial B_{up} pulse burst of 49 pulses is sent out. This pulse burst replaces the actually measured B-pulses in the region of the PS magnetic cycle where the field measurement is not defined. The artificial B-pulse burst prevents a counting offset of the $B_{up/down}$ counter. The B-pulses are available in 2 qualities :

B10 (10 Gauss per step)
B1 (1 Gauss per step)

RF-Pulse Train

The bunch structure of the PS proton beam is given by the RF voltage in the accelerating cavities. The position of the bunches on their orbit is strictly linked to the RF voltage. The frequency of the RF voltage is a function of the proton energy and varies between 2,85 and 9,54 MHz. If the RF voltage is used for synchronization, we are interested to know that the RF has a small variation for proton energies between e.g. 10 GeV and 28,88 GeV, namely from 9,507 to 9,538 MHz (MPS/Int SR 68-7 by H.H. Umstätter).

For timing purposes two RF reference voltage sources are available with different characteristics :

- The summed RF voltage derived from a passive network in the accelerating cavities.

- The "beam control RF voltage" derived from a frequency programmed oscillator.

The summed RF voltage (S-RF) follows a frequency, phase angle and amplitude programme specific for proton acceleration. After the moment of debunching or after the beam is lost up to the next MW pulse, the S-RF is suppressed (i.e. no voltage on the cavities).

The "beam control RF voltage" BC-RF is derived from a frequency programmed oscillator which is synchronized to the voltage of a beam pick-up during the acceleration up to the moment of debunching or total beam loss. The amplitude of the BC-RF voltage is constant. During acceleration until debunching, no phase jumps occur (the BC-RF voltage is phase locked to the longitudinal position of the bunches on their orbit). After debunching or after a total beam loss, the BC-RF corresponds to the free running frequency of the programmed oscillator.

4.2 Critical Remarks on Actual PS Time References

M-Train Resolution

The M-300 Hz train resolution of 3,3 ms is no longer sufficient for modern power supplies, e.g. fast resonant charging power supplies. Additional analog or digital fine delays must be brought into operation.

With more complex machine cycles, the timing schedules become also more complicated. The thinking on timetables in units of 3,33 ms is tiresome and a serious error source.

M-Train Frequency Stability

The M-train with its inherent frequency variation of 2% around a mean value cannot be used as clock in a timing for an equipment which is sensitive to time interval variations between its timing pulses.

Dependence of Different Timing Systems to Each Other

The use of different key machine pulses and marking holes in pulse trains in a local timing system for internal synchronization purposes (e.g. readout and setting) brings it into setting dependence, e.g. of the power house timing system. These cross links can strongly restrict the freedom for future modification of the linked systems at both, the hardware and software levels.

RF-Reference Voltage

The use of the summing RF voltage as clock in a timing system can cause missing preset pulses if the RF is suppressed. Missing timing pulse can lead to troubles in H.V. equipment (e.g. H.V. flash-over, spontaneous break-through of H.V. switches etc.). The phase shift correction of the summed RF voltage used for an RF timing system is a nasty problem because normally a beam pick-up voltage linked to the bunch structure is not available at a local timing position.

4.3 Proposal for Slightly Changed PS Time References

The M-300 Hz pulse train is essential for the ring magnet power supply synchronization and cannot easily be changed. To greatly increase the resolution of the M-train is not very advantageous due to its inherent frequency variations. A M-1000 Hz train distributed in parallel with the M-300 Hz train is the most convenient solution.

The M-1000 Hz train is a PS standard pulse train (blocking oscillator) and has no missing pulses during the machine cycles. If the timing equipment needs a gated train for readout and setting purposes, the gating occurs locally.

The zero time reference for all local timing systems is the key machine pulse MR (machine cycle reset pulse). The MR pulse is the only

distributed key machine pulse (PS standard pulse, blocking oscillator).

A M-timing system must be used for all equipment which is sensitive to the rest ripple of the ring magnets. Interferences which could occur between a free running clock and the alternator frequency are a priori suppressed in an M-timing.

T-1000 Hz Train

The MR pulse resets and restarts just after the reset a modulo 10'000 divider which divides a 10 MHz crystal clock train down to a non gated 1 KHz pulse train, the T-1000 Hz train. The jitter of the T-1000 Hz train compared with the MR pulse is max. |100 ns|. The distribution of the T-1000 Hz train occurs with PS standard pulse blocking oscillators.

A T-1000 Hz timing must be used for equipment which is sensitive to time interval variations between its timing pulses.

Resolution of the M-1000 Hz and T-1000 Hz Pulse Trains

A further reason for the choice of a 1 ms resolution for the M-1000 Hz and T-1000 Hz train is the counting capacity of preset counters. The future super machine cycle length can grow to 10 secs. A preset counter which must cover the whole super machine cycle needs a counting capacity of 10^4 counts (14 bit). For a 10 times better resolution of the M and T trains the same counter must have a counting capacity of 10^5 counts (17 bit). The PS computers are standardized to 16 bit data words. The PS 17 bit counter must be set with a double word which complicates the setting and read-out processes disproportionally to the gain in resolution.

10 MHz Reference Voltage

The same crystal oscillator which feeds the modulo 10'000 divider with its associated line drivers for the T-1000 Hz train supplies also the line driver power amplifier for the 10 MHz reference voltage distribution. The distributed 10 MHz reference voltage is a pure sine wave voltage of

10 Vpp into 50 Ω and is not gated. A sine wave distribution is proposed for having better transmission properties than for a shaped 10 MHz pulse train.

The 10 MHz voltage must be used in conjunction with the T-1000 Hz train as clock frequency for precise digital delays which have no jitter against each other. In conjunction with the key machine pulse MR and the M, T, B-pulse trains, all kinds of delicate jitter and absolute time measurements can easily be realized.

RF Reference Voltage

For RF timing purposes the ungated "beam control RF voltage" BC-RF must be used. The distributed BC-RF is a pure sine wave voltage of 10 Vpp into 50 Ω. A sine wave distribution is proposed for having better transmission properties than for a shaped RF pulse train.

The bunch labelling occurs with the RF/20 pulse train. A pulse derived from PS inflection or another PS revolution trigger resets and restarts a modulo 20 divider just after the reset. This divides the RF pulse train by 20. The distribution of the RF/20 pulse train occurs with a special, fast blocking oscillator.

A RF timing must be used for equipment sensitive to the longitudinal position of the bunches on their orbit, e.g. fast kicker and fast beam diagnostic equipment.

Summary of Proposed Synchronization Pulses

M-1000 Hz train	PS standard pulse train	ungated
MR key machine pulse	PS standard pulse	
T-1000 Hz train	PS standard pulse train	ungated
10 MHz reference voltage	Sine wave distribution 10 Vpp into 50 Ω	ungated
$B_{1\ up}$ train	PS standard pulse train	ungated

$B_{1\ down}$ train	PS standard pulse train	ungated
$B_{1/10\ up}$ train	Special pulse, fast blocking oscillator	ungated
$B_{1/10\ down}$ train	Special pulse, fast blocking oscillator	ungated
B reference pulse	PS standard pulse	
RF reference voltage	Sine wave distribution 10 Vpp into 50 Ω	
RF/20 pulse train synchronized to inflection	Special pulse, fast blocking oscillator	ungated

5. Specification for a Computer Compatible Timing System

5.1 Computer Compatibility

A computer compatible timing system must be set and checked by the computer. The check must be carried out on the counter content and the output voltage of the line driver for the present pulse.

To keep the danger of induced setting faults due to parasites to a minimum (H.V. flash-over and spontaneous break-through of switching elements), a computer compatible timing system must be checked and set in each machine cycle.

The operation facility (OSF, FES) of having pre and post preset counters attached to a master preset counter must exist also in a new timing. The distinction between the master preset counter and its associated pre and post present counter must be made by computer software.

> Modular software must be developed for easy translation from a special PS operation time schedule into a computer timing programme.

5.2 System Layout

A computer compatible timing system must be easily adaptable to different computers and data transfer systems. Therefore, and for easy

debugging, the timing system must be built in a modular form. During runs, the change of plug-in units must be possible in a powered timing crate without causing component damage.

The M and T preset counters (M-1000 Hz, T-1000 Hz train) must have a counting capacity of 10^4 counts for covering a super machine cycle of about 10 sec duration. If the preset counter counts binary, which is feasible for computer read-out and setting, it must have a counting capacity of 14 bits.

The $B_{1\ up/down}$ preset counter must cover a magnetic field from 0 to $\approx$ 12 KGauss which corresponds to $1{,}2 \cdot 10^4$ counts or 14 bit if a binary counter is used. The same counting capacity is also sufficient for the $B_{1/10\ up/down}$ counter due to its limited operation range around the PS inflection.

An extension of the counting capacity to 10^4 for the RF preset counter compared with the OSF and FES counting range of 10^3 counts is desirable, e.g. for the synchronization of medium speed pulsed beam transports for ejected bunches with magnet pulse lengths of several 100 µs.

During the read-out and setting process the timing preset counters are blocked.

The read-out and setting process of the preset counter can be inserted at any time in the machine cycle. The counting offsets caused by this insertion are corrected by the computer with a numerical setting correction.

The computer and its associated timing system must be synchronized with a common synchronizer working exclusively with the PS synchronization signals mentioned in chapter 4.

5.3 Timing Operation Facilities

The timing system (hardware and software) must offer the following facilities :

M,T Master	preset counter with inhibit,	computer checked and set
M,T Pre-pulse	preset counter with inhibit,	computer checked and set
M,T Post-pulse	preset counter with inhibit,	computer checked and set
$B_{up/down}$	preset counter with inhibit,	computer checked and set
RF Master	preset counter with inhibit,	computer checked and set
RF Pre-pulse	preset counter with inhibit,	computer checked and set
RF Post-pulse	preset counter with inhibit,	computer checked and set
Modulo n driver	preset counter,	computer checked and set
Digital delay	preset counter,	computer checked and set
Cable delay line		computer set

5.4 Excluded Operation Facilities

The timing system fulfills timing functions only. Fast and slow interlocks on the timing pulses must be executed locally by supplementary hardware in the equipment which is synchronized by the timing.

Not included in the timing system are the fan-in units for collecting the timing pulse for different shots or cycles and feeding them into the equipment which is fired several times in one cycle. Also not included in the timing system are the fan-out units for distributing one timing preset pulse to more than one equipment block. These fan-in and fan-out units vary with different equipment and cannot be standardized.

A hardware manual back-up setting will not be provided.

5.5 Hardware

The developing costs of electronics hardware, once subtracted from system engineering costs, grow proportionally to the number of printed

circuits which must be designed. The same is true for maintenance and spare part costs. Therefore, the number of printed circuits must be kept to a minimum. This can be done by looking for a multi-purpose counter ((M,T), RF, B, 10 MHz) on one hard-wire programmed printed board for the timing system. A timing system with a multi-purpose counter will have insignificantly more material with regard to a system with individual counters for each application.

5.6 Data-Transfer System

The timing crates can be placed anywhere in the PS area. An individual cable must link the data transmission system terminating box to each timing crate. This prevents short-circuits on the data line, due to unpowered timing crates. The adaption of the timing crate to different data transfer systems occurs in 4 specific plug-in units.

6. Timing Equipment and its Operation

6.1 Timing System

A typical timing system connected to the EMAS computer via the DTS data transfer system is shown in the block diagramme Fig. 1. Each timing crate is connected via 50 Ω coaxial cables to the timing and computer synchronizer.

Three types of timing crates are proposed :

- The timing crate A (Fig. 2, Fig. 3) housing the preset counters (M,T), B, RF, the modulo n divider and the digital delays up to 16 units per crate, the crate controller and four specific data transfer interface units 22, 23, 24, 25.

- The timing crate B (Fig. 4, Fig. 5) housing the cable delay relay drivers up to 8 units per crate, the crate controller and four specific data transfer interface units 22, 23, 24, 25.

- The twin cable delay crates (Fig. 6) which are driven by the cable delay relay driver in the timing crate B via multicore cables.

6.2 Timing Crate

In the timing crate A five types of preset counters can be inserted from the left side,up to 16 units per crate :

- M,T preset counter
- $B_{up/down}$ preset counter
- RF preset counter
- Modulo n divider preset counter
- Digital delay preset counter

The remaining 9 places on the right side of the 16 counter places contain the crate controls :

- Crate controller
- Data transfer interface 22
- Data transfer interface 23
- Data transfer interface 24
- Data transfer interface 25

Figs. 2 and 3 show the front view of the timing crate A and Fig. 7 the rear panel.

All preset counters for the (M,T),B, RF and 10 MHz pulse train are equipped with the same multipurpose printed circuit board (PCB). The RF and 10 MHz incoming sine wave voltage is converted into a pulse train in the crate controller. These boards must be hard-wire programmed (wire bridges) before they can be brought into operation. Four types of pro-

grammed PCB must be distinguished :

- M,T preset counter card
- $B_{up/down}$ preset counter card
- RF preset counter card
- Digital delay preset counter card

The programmed status of each multi-purpose PCB is indicated by its plug-in unit front panel colour and text. The modulo n divider plug-in unit is equipped with a special printed circuit board which differs from the multi-purpose PCB for the preset counters.

The distinction between master M,T preset counters and pre- or post M,T preset counters is made by software in the computer.

The M,T preset counter is the only unit which can be used independently of other preset counters. The $B_{up/down}$ and RF preset counter, as well as the modulo n divider, must be used in conjunction with other preset counters (e.g. M,T counter).

The $B_{up/down}$ preset counter must be plugged into the crate on the right side of M,T preset counter without leaving a space. The combination is called a M,T preset pulse, gated $B_{up/down}$ preset counter (M,T gated B counter). This means the $B_{up/down}$ preset counter can send out its pre-selected pulse only when the counter output gate is opened by a preceding M or T preset pulse. The M or T preset pulse decides which of the possible pre-selected $B_{up/down}$ pulses of the tracking $B_{up/down}$ preset counter must appear at its output. With one M,T preset counter, one $B_{up/down}$ preset counter can be gated. On the right side of the $B_{up/down}$ preset counter M,T counters can again be inserted into the crate and produce their preset pulses independently of the preceding units on the left side.

The RF preset counters must always be gated by a M,T or a M,T gated $B_{up/down}$ preset pulse (M,T gated RF counter or M,T gated B gated RF counter). As many RF preset counters can be gated with a M,T or M,T gated

B counter in an uninterrupted line as there are places available in the crate on the right side of the preceding unit. If not all free places are occupied by RF preset counters, the remaining places can be filled with M,T or a new combination of M,T-B-RF preset counters. The distinction between the master RF and pre or post-RF preset counters is made by software in the computer.

In conjunction with a M,T or a M,T gated B preset pulse gated modulo n divider, a divided 10 MHz train is applied to a digital delay. The gated modulo n divider divides the internal or external clock frequency by a computer pre-selected ratio (1:1, 1:10, 1:100, 1:1000, 1:10000). The succeeding digital delays to the right of the gated modulo n divider behave identically to M,T gated RF counters or M,T gated B gated RF counters.

All four types of preset counters ((M,T), $B_{up/down}$, RF and digital delays) are equipped with three lamps on their front panel.

When the top lamp lights up, the preset counter is inhibited by the computer. The centre lamp lights up when the output line driver (blocking oscillator) of the preset counter is fired at the correct time with its correct voltage level. The lamp extinguishes when the preset counter is reloaded from the computer.

The bottom lamp on the front panel flashes when the blocking oscillator is triggered back by parasites on the output cable at a different time than the pre-selected one.

With a toggle switch on top of the front panel in the display frame of the controller, the setting or read-out data can be selected for display on a direct hardware LED display.

The second frame from the top contains the address selection switches for the preset counters whose setting or read-out data is being displayed. The selected address is displayed on a LED check display.

The preset counter address number is identical to the crate place number 1 - 16.

The first toggle switch from the left side in the lowest frame on the crate controller front panel enables selection of the M-1000 Hz or T-1000 Hz pulse train for the whole crate. With the second toggle switch from the left in the lowest frame, the RF preset counter can be synchronized to the PS inflection (revolution trigger), or this synchronization can be suppressed. The chosen mode is valid for all RF preset counters in one crate.

With the third toggle switch from the left in the lowest frame, the internal or external 10 MHz clock can be selected. The selection made is valid for all modulo n dividers with their associated digital delays in one crate.

With the two toggle switches on the right side in the lowest frame, the RF and 10 MHz internal shaped pulse trains can be selected for gating by a PS standard pulse applied to a coaxial plug on the rear panel of the timing crate A.

Two solutions were studied to interface the timing system to the EMAS computer :

- Connection of the timing crates A and B to the EMAS computer via the DTS.

- Connection of the timing crates A and B to the EMAS computer via a PDP 11 unibus extension.

All input and output plugs for the timing crate are mounted on the rear panel. All coaxial 50 Ω BNC plugs are insulated from the chassis. On the right side of the crate rear panel in one frame, the 16 BNC coaxial plugs (50 Ω) for the preset counter outputs are mounted. The outputs are transformer-coupled and therefore insulated from the crate and electrical ground of the counter circuit. On the left hand side of the crate rear panel are mounted : 2 Burndy 104 pin plugs for the data branch and coaxial plugs for the machine synchronization signals and the internal shaped RF and 10 MHz pulse trains gating pulses (Fig. 7).

6.3 Cable Delay Control Crate

In one cable delay control timing crate B (Fig. 4, Fig. 5) up to 8 units of twin cable delay relay drivers can be housed. These drivers excite the reed relays in the twin cable delay crate (Fig. 6). The crate controller and the data transfer system interface are rudimentarily equipped units, similar to those used in the timing crates A. On the rear panel of the cable delay control crate the 8 Burndy plugs are mounted for the multi core cables leading to the twin cable delay crates.

6.4 Twin Cable Delay

The twin cable delay crate (Fig. 4, Fig. 5) contains two independent cable delays insulated from ground. The coaxial cable lengths are switched with dry or mercury wetted Reed relays. The resolution of the cable delay is 1 ns and its max. delay is 127 ns plus a fixed delay of about 6 ns due to connections.

6.5 Timing Synchronizer

In the local timing synchronizer the continuous PS synchronization pulse trains are gated for read-out and setting purposes. The gating occurs with the help of (M,T) and $B_{up/down}$ preset counters. For each of the 3 pulse trains M,T and (B_{up}, B_{down}) two preset counters (two M preset counters, two T preset counters and two (M,T) gated $B_{up/down}$ preset counters) in connection with a flip-flop are gating the M,T and (B_{up}, B_{down}) pulse trains. This enables a hole to be artificially placed in the four pulse trains at any time in the machine cycle. The difference of the two setting values of a pair of preset counters attached to one train corresponds to the hole width and the numerical offset correction of preset counter setting values given by the computer.

6.6 Timing Software

A detailed software proposal containing the computer organization,

the modular software for easy translation of timing schedules into timing computer programmes and the man-machine interface will be made and published by H. Kugler, P. Pearce and H. Riege

Man Effort and Prices

The analysis of two detailed tenders from two different firms on the timing system proposed in this report is summarized in Tables 1 and 2. The cost estimates for the prototypes and the series are separately listed. This allows a transparent planning to manufacture the timing system. In Tables 1 and 2 three specific kinds of working hours must be distinguished :

- Laboratory hours
- Drawing office hours
- Workshop hours

Such a detailed estimation enables the CERN representatives to judge whether a firm is able or not to do the job in an adequately short time.

The firms worked out their tenders with the help of a CERN price inquiry form and on the base of block and detailed circuit diagrams of the proposed timing system.

Final Remarks

The detailed circuit diagrams and the commercial documentation are not of general interest and therefore not attached to this report. (D. Bloess has got full documentation.)

Some circuit diagrams for special apparatus (e.g. synchronizer) have still to be done. Since no laboratory tests on the crucial parts (RF distribution, RF synchronization, etc.) have been done, a good electronic engineer must spend 3 to 5 months for completion of the design and manufacturing files. Small modifications of the circuit design or in the plug-in and

crate arrangement will certainly be necessary, but have no significant influence on the overall system price and the total man effort.

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SIGNAUX ET AUTOMATIQUE SA BERNE

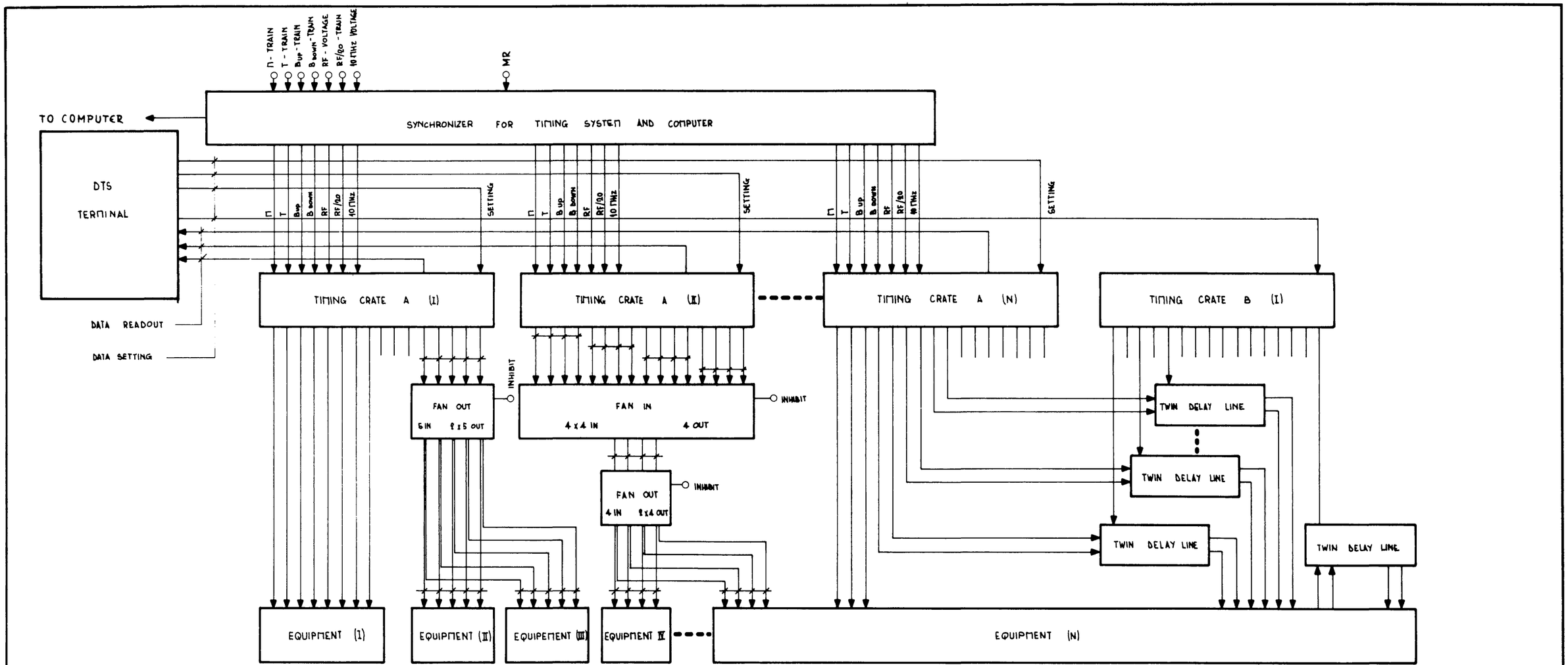
	BUREAU TECHNIQUE h	ATELIER h	LABO h	TOTAL h	PRIX		PRIX TOTAL FIRME		MATERIEL CERN SFr.	PRIX TOTAL SFr.
					TRAVAIL S Fr.	MATERIEL FOURNI P. FIRME S Fr.	SANS ICHA S Fr.	+ 4% ICHA SFr.		
PROTOTYPE	942,4	355	242	1539,4	55'418,4	4'986.-	60'404,4	62'820,6	3'520.-	66'340,6
SERIE	—	3'267,2	1040	4307,2	155'059,2	52'740.-	207'799,2	216'111,7	154'100.-	370'211,7
TOTAL	942,4	3622,2	1282	5846,6	210'477,6	57'726.-	268'203,6	278'931,3	157'620.-	436'551,3

TABLE 1

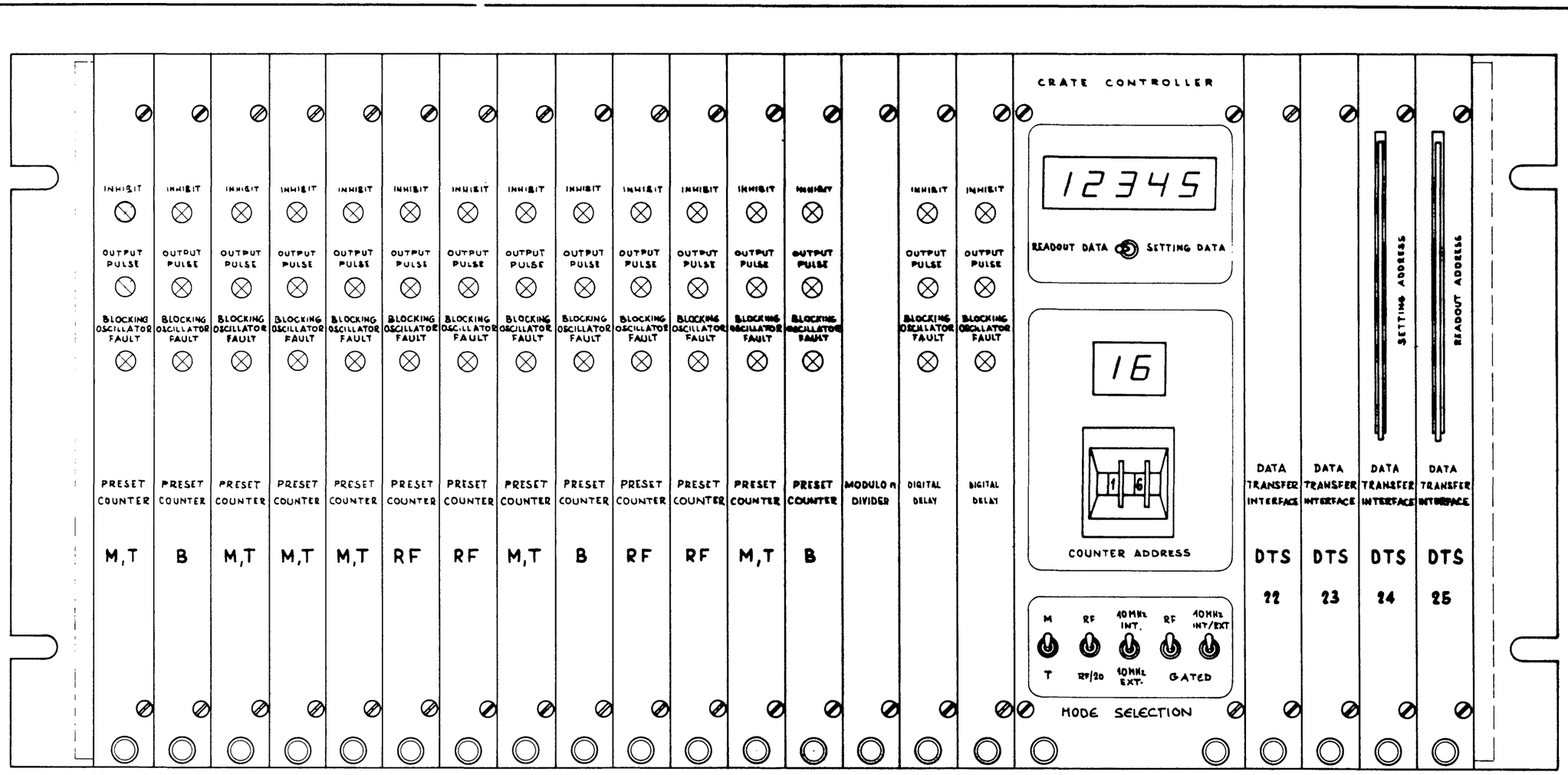
EIDGENÖSSISCHE WAFFENFABRIK BERN

	BUREAU TECHNIQUE h	ATELIER h.	LABO h	TOTAL h	PRIX		PRIX TOTAL FIRME		MATERIEL CERN SFr.	PRIX TOTAL SFr.
					TRAVAIL SFr.	MATERIEL FOURNI P. FIRME SFr.	SANS ICHA SFr.	4% ICHA SFr.		
PROTOTYPE	1'402	461	620	2'483	89'188.-	3'230.-	92'418.-	96'114,7	3'520.-	99'634,7
SERIE	—	2'430	1560	3990	143'640.-	45'800.-	189'940.-	197'017,6	154'100.-	351'117,6
TOTAL	1'402	2891	1'980	6273	232'828.-	49'030.-	281'858.-	293'132,3	157'620.-	450'752,3

TABLE 2



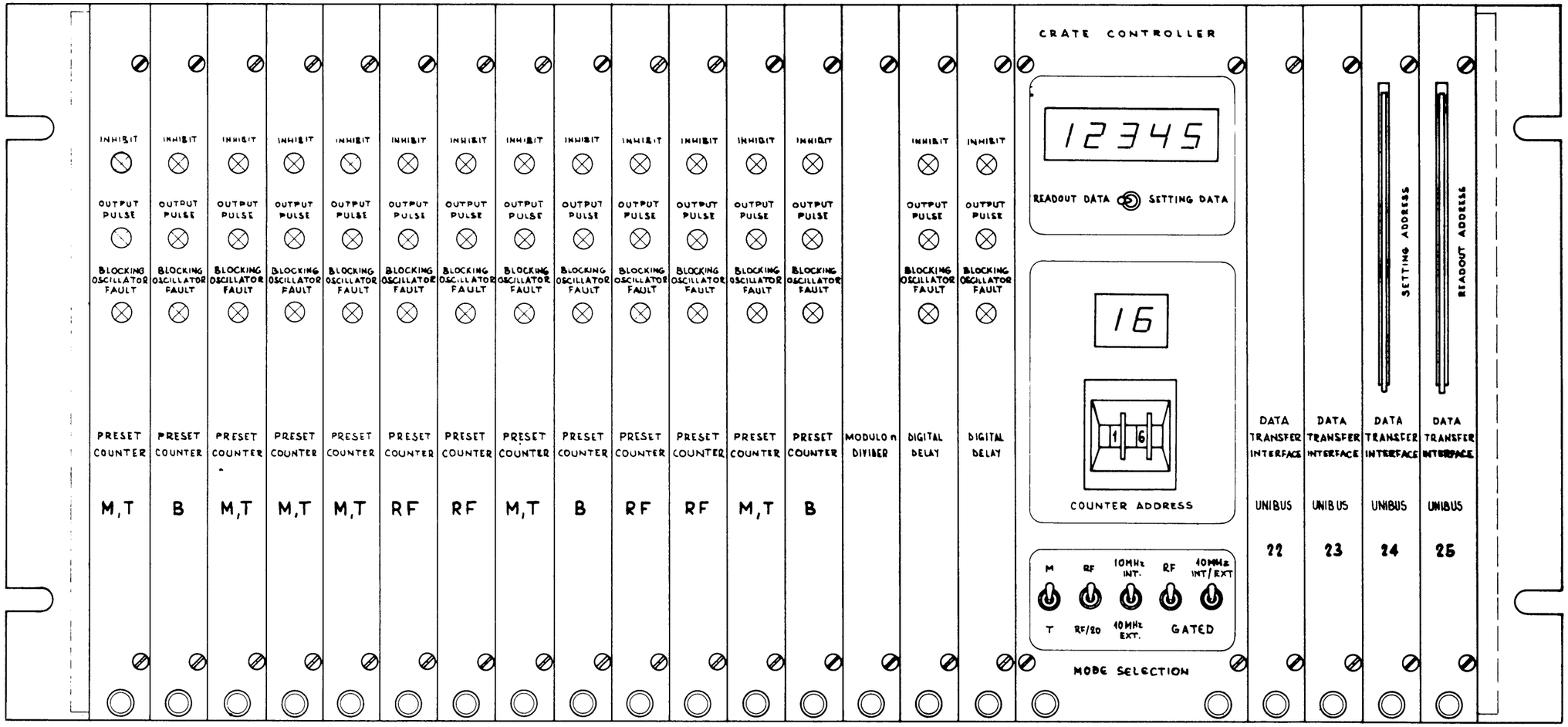
TIMING BLOCK DIAGRAM INTERFACED TO THE EMAS COMPUTER VIA THE DTS DATA TRANSFER SYSTEM FIG 1



TIMING CRATE A

INTEREFACED TO THE DTS SYSTEM

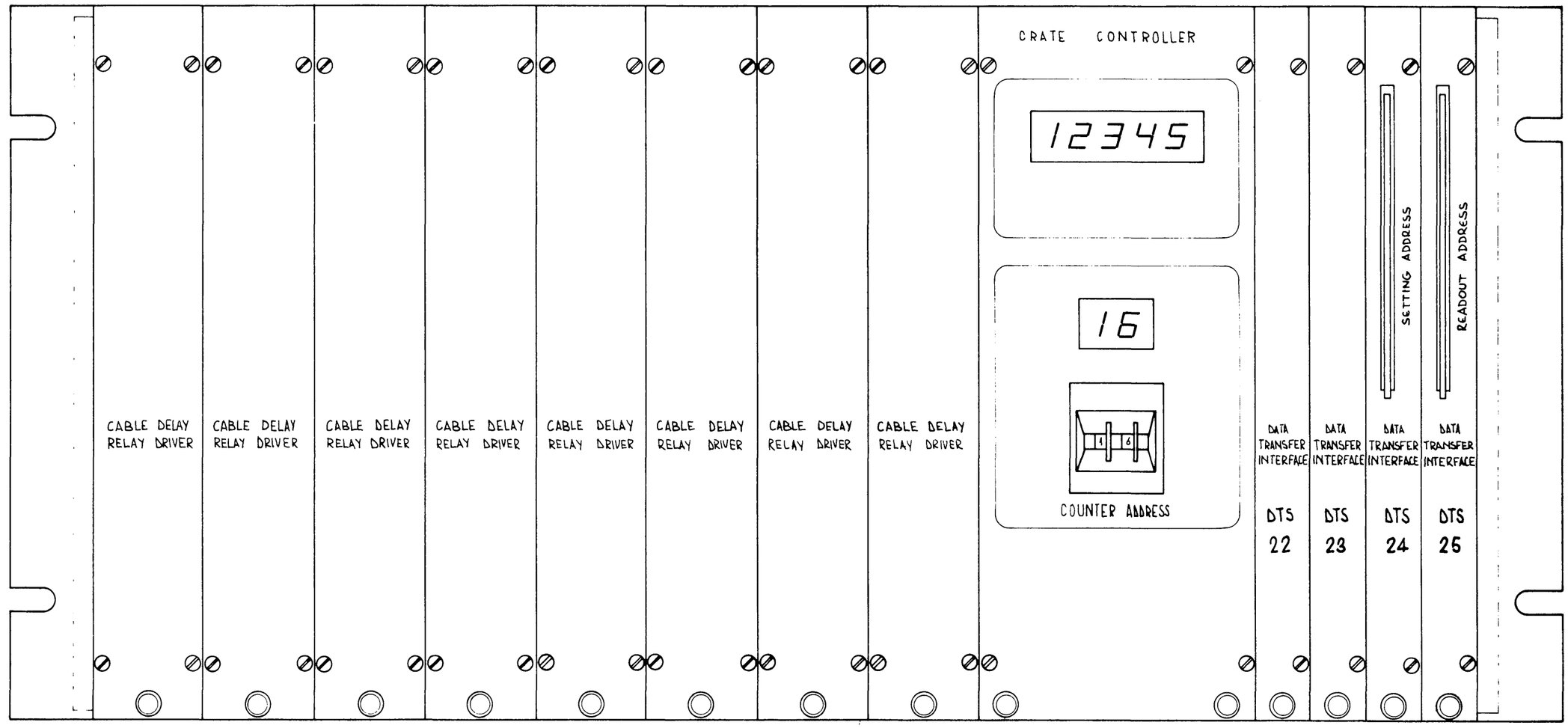
FIG. 2



TIMING CRATE A

INTERFACED TO THE UNIBUS EXTENSION OF THE PDP 11/45 (ETAS COMPUTER)

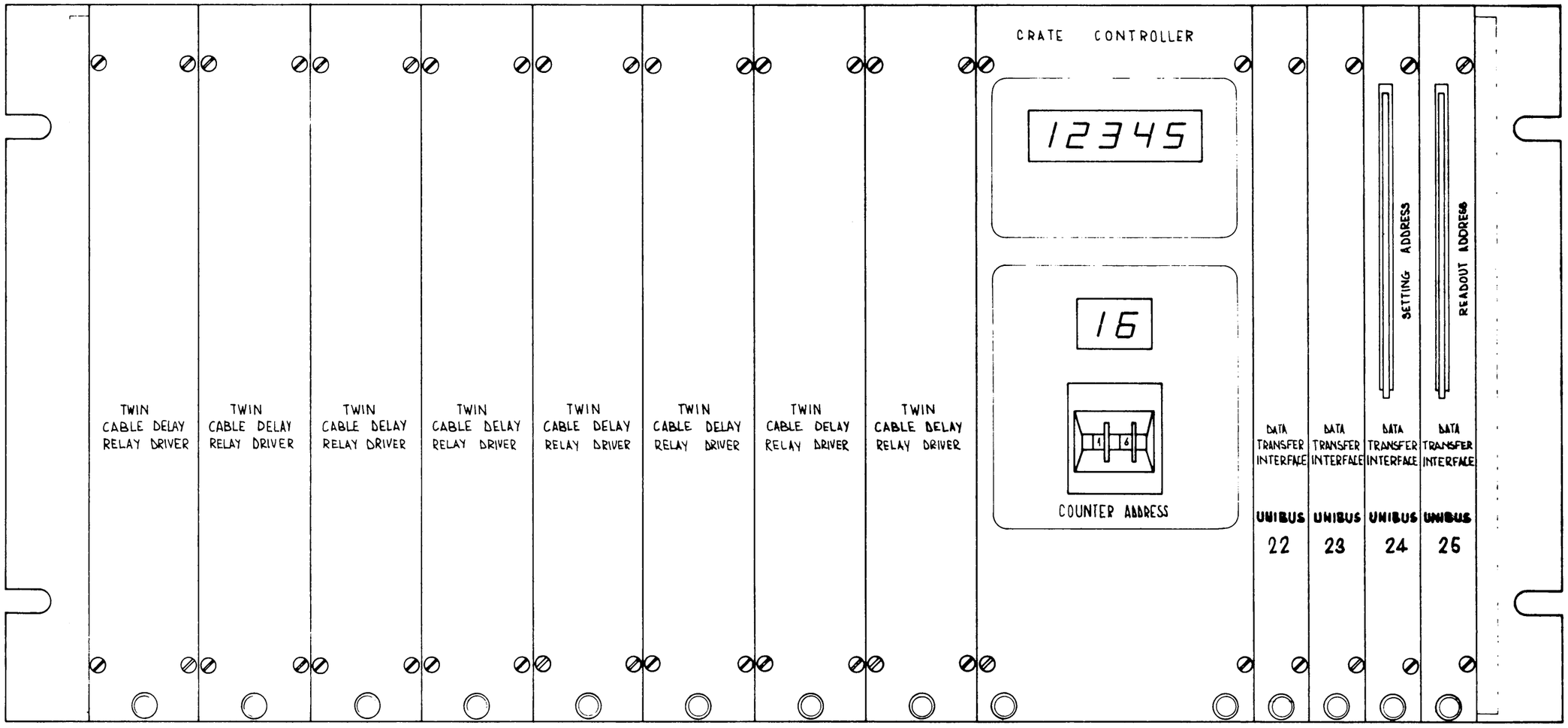
FIG 3



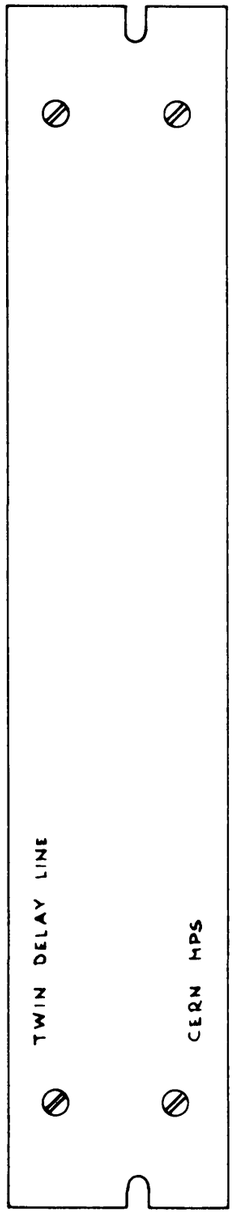
TIMING CRATE B

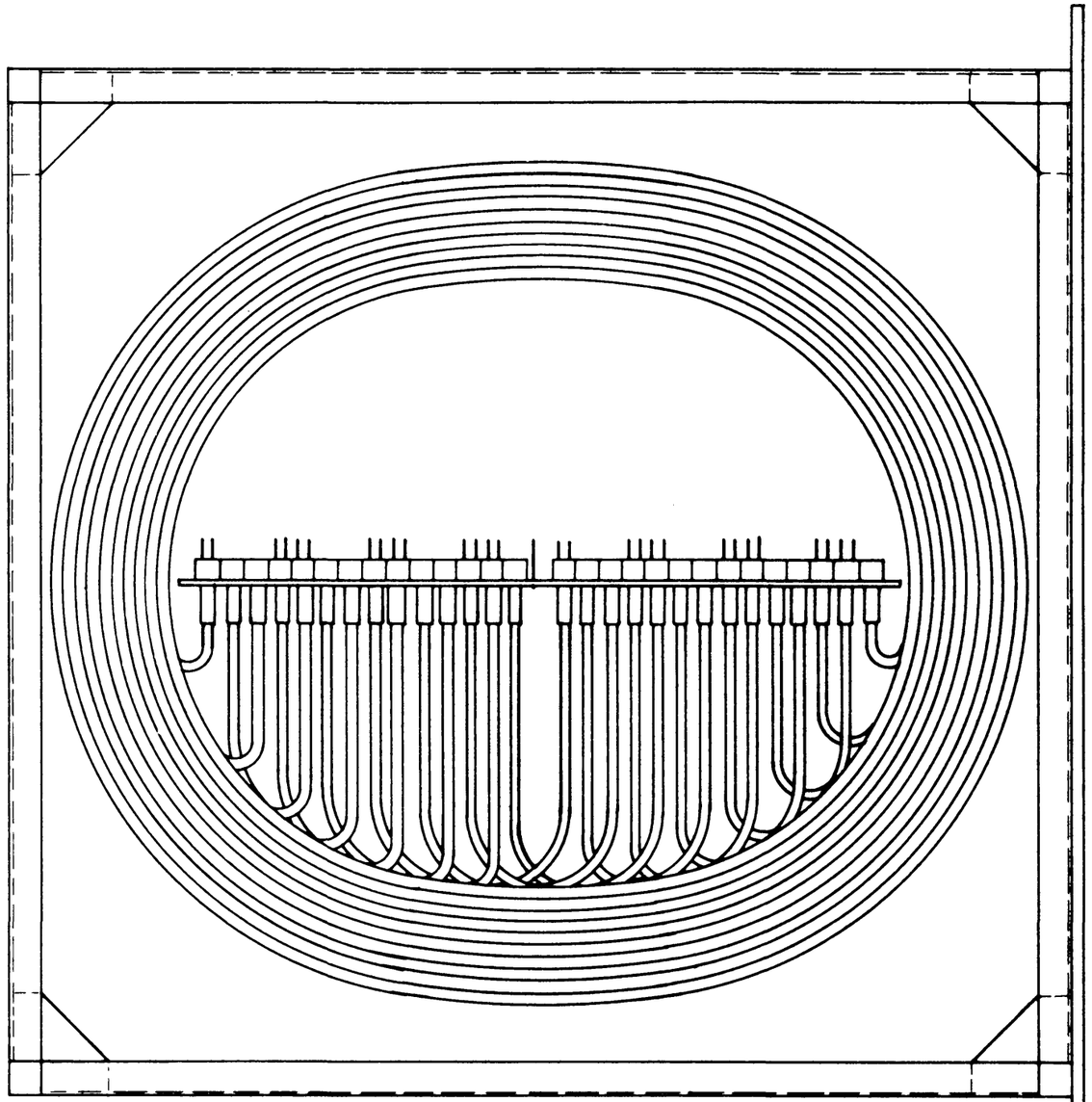
INTERFACED TO THE DTS SYSTEM

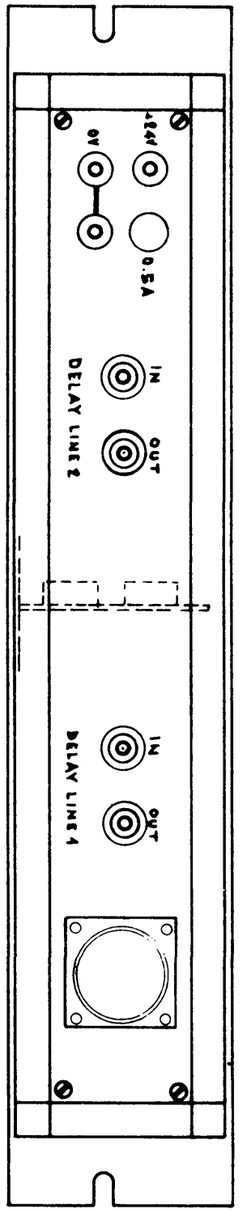
FIG. 4



TIMING CRATE B.
INTERFACED TO THE UNIBUS EXTENSION OF THE PDP 11/45 (EMAS COMPUTER) FIG 5

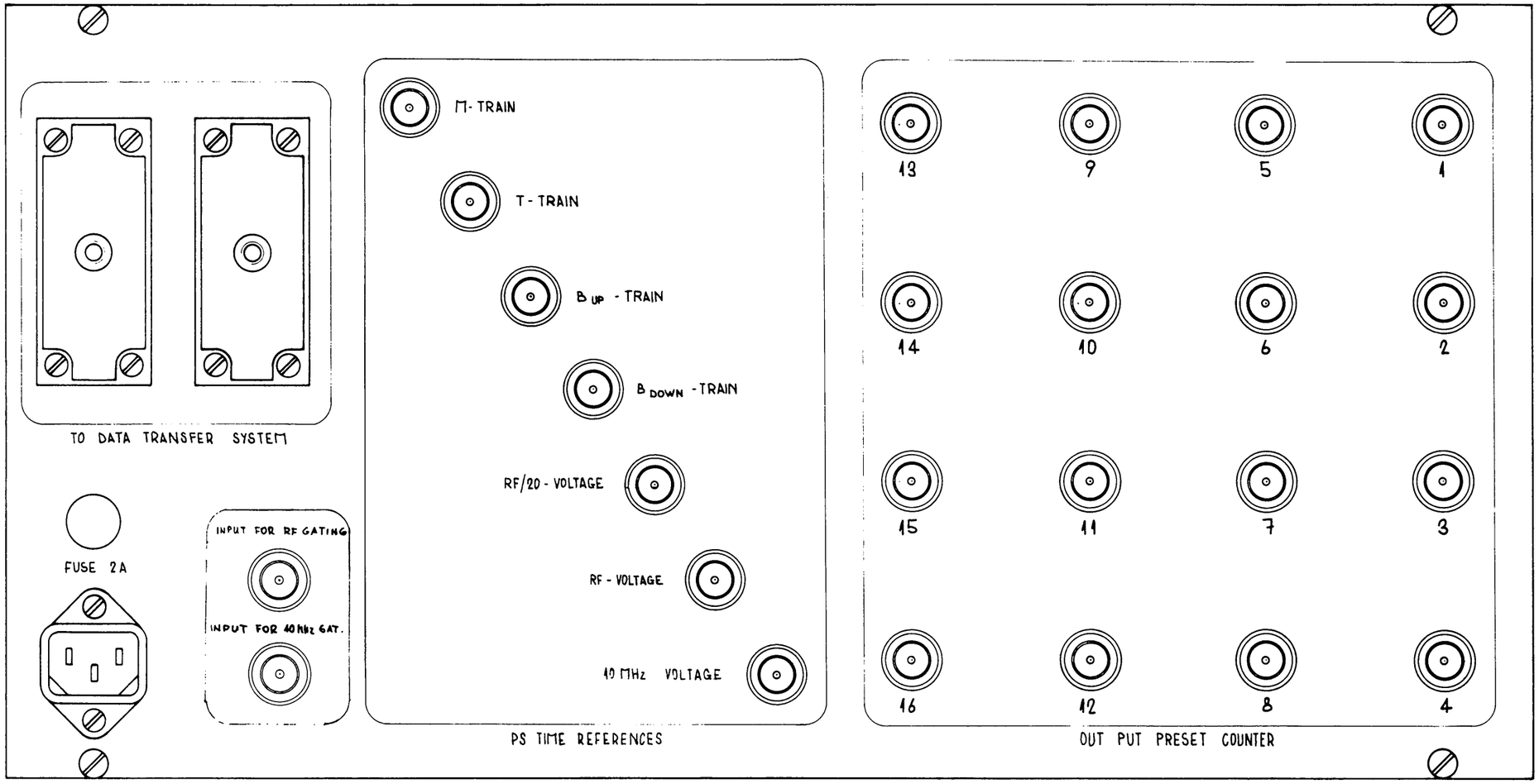






TWIN CABLE DELAY LINE

FIG 6



TIMING CRATE A REAR PANEL

FIG 7