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High-rate, high-resolution single photon X-ray imaging: Medipix4, a large 4-side buttable pixel readout chip with high granularity and spectroscopic capabilities

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Abstract: The Medipix4 chip is the latest member in the Medipix/Timepix family of hybrid pixel detector chips aimed at high-rate spectroscopic X-ray imaging using high-Z materials. It can be tiled on all 4 sides making it ideal for constructing large-area detectors with minimal dead area. The chip is designed to read out a sensor of 320×320 pixels with dimensions of $75\,\mu m \times 75\,\mu m$ or 160×160 pixels with dimensions of $150\,\mu m \times 150\,\mu m$. The readout architecture features energy binning of the single photons, which includes charge sharing correction for hits with energy spread over adjacent pixels. This paper presents the specifications, architecture, and circuit implementation of the chip, along with the first electrical measurements.

Keywords: Analogue electronic circuits; Digital electronic circuits; Front-end electronics for detector readout; Hybrid detectors

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Contents

1 Introduction

Over the past two decades, 4 successive Medipix collaborations has been established. These collaborations aim to exploit the knowledge acquired from advancements in high-energy physics to develop cutting-edge hybrid pixel detectors, enabling the precise detection of individual X-ray photons or particles on a per-event basis [1]. These technologies have diverse applications across scientific domains, including medical imaging, X-ray cameras at synchrotrons, X-ray-based material analysis, electron microscopy, among others.

First, the Medipix1 chip demonstrated the principle of a single photon counting architecture within a pixel pitch of 170 µm, and showcased the feasibility of X-ray imaging without noise hits by using a pulse processing front end while setting the detection threshold well above the level of background noise [2]. Medipix2 proved the feasibility of spectroscopic imaging with a compact pixel pitch of 55 µm by using dual thresholds per pixel [3]. However, the reduced pixel dimensions led to significant charge sharing between pixels due to diffusion during charge collection and fluorescence photons in high-Z materials [4, 5]. The readout electronics underwent a transition from single photon counting to a single photon processing architecture with the introduction of Medipix3RX. A novel scheme implementing an inter-pixel algorithm directly on the 55 µm pixel eliminated the energy spectral distortion produced by charge diffusion [6, 7]. Medipix3RX also introduced the option of connecting one pixel in 4 to a sensor with 110 µm pixel pitch.

Nonetheless, the Medipix3RX detectors can be abutted only on three sides, as one side of the chip is reserved for control logic and IO. This complicates the realization of a continuous large-area detector. The Medipix4 presented in this paper, follows the advancements of the Timepix4 chip and enables the application-specific integrated circuit (ASIC) to be tilled along all four sides with minimal dead-area [8]. Another constraint in medical X-ray computed tomography (CT) and X-ray imaging arises from pulse pile-up, which is attributed to the inherent dead time of counting systems [9]. Some recent photon counting detectors have begun developing on-pixel schemes to compensate for this effect and to increase the count-rate performance when employing monochromatic sources [10–12].

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In this latest Medipix iteration, a new pulse processing mechanism is integrated directly into the pixel to filter pile-up events that can occur with polychromatic radiation. Medipix4 focuses on improving the spectral fidelity using both charge sharing correction and pile-up filtering method.

Furthermore, the majority of current X-ray imaging systems are tailored for particular applications, such as employing small pixel pitches in synchrotron applications to achieve high count-rate capability while sacrificing spectral fidelity due to charge sharing and fluorescence effects. Conversely, larger pixel sizes are employed in most CT imaging systems to cope more with fluorescence in high-Z materials, while compromising spatial resolution (complete review on existing photon counting detectors for X-ray imaging and its limiting factors can be found in our paper [13]). The ASIC presented in this paper is highly programmable to accommodate a large range of applications. The Medipix4 chip has been designed to facilitate large-scale applications, enabling high-rate spectroscopic X-ray imaging at fine pitch using high-Z materials while maintaining spectral accuracy through the implementation of an inter-pixel architecture to correct the impact of charge sharing. The structure of this paper is as follows: section 2 starts by outlining the key specifications of the Medipix4 chip alongside its floorplan. In section 3, the architecture of the analog and digital pixel cells is described. Section 4 focuses on the initial results of electrical characterization. We conclude with a summary and an outline of future plans.

2 Medipix4 chip floorplan and specifications

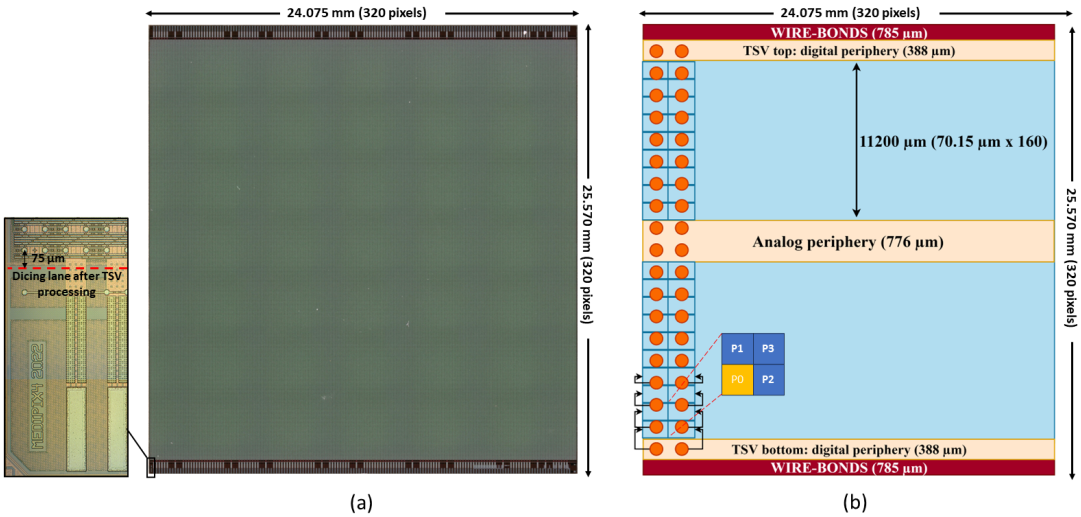

Figure 1. (a) The picture of the Medipix4 chip is presented, with a magnified inset located in the bottom corner. This inset shows the wire bond extenders that can be diced off after TSV processing. (b) The floorplan of the chip is shown schematically (not to scale). The readout pixels within the blue region measure 75 µm × 70.15 µm and are connected to an array of bump bonding pads with 75 µm pitch in both directions. This allows space to accommodate the peripheral circuits at the top, middle, and bottom of the chip.

The ASIC measures 24.075 mm × 25.570 mm and has been designed using an 8-metal layer commercial 130 nm technology process and has a power supply voltage of 1.2 V. The chip is designed to read out a sensor of 320 × 320 pixels with dimensions of 75 µm × 75 µm (*fine pitch mode*) or 160 × 160 pixels with dimensions of 150 µm × 150 µm (*spectroscopic mode*). The top surface of the Medipix4 ASIC is fully covered with a matrix of 320 × 320 bump bonding pads (with 20 µm

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octagonal opening) distributed on a 75 µm square pitch. The Medipix4 chip adopts the Timepix4 layout configuration, thereby attaining a complete sensitive area and enabling tiling along its four sides [8]. The readout pixels and peripheral circuits are positioned beneath the uniformly distributed bump bonding pads. This arrangement results in the readout pixels being smaller than the sensor pixels in one direction to incorporate the peripheral circuits. The readout electronics consist of two arrays, each containing 320×160 pixels with dimensions of 75 µm $\times$ 70.15 µm. A redistribution layer (RDL) is integrated using the top metal layers to establish connections between the pads and their corresponding readout electronics. As this approach involves a non-intimate connection between the readout and sensor pixels, it comes at the 'cost' of an additional 80 fF to the input capacitance of the front-end electronics. The primary challenge revolves around ensuring uniformity in input capacitance and providing adequate shielding to suppress any coupling with neighboring pixels and the chip's readout electronics [14]. The chip incorporates three peripheral regions, a space of 776 µm between the two matrices of readout pixels forming the analog periphery and 388 µm on each side for the digital peripheries. The analog periphery is composed of the blocks required for biasing the analog circuits within the pixels. The digital peripheries include control logic, data output SLVS (programmable between 1 to 8 per edge periphery), and the through-silicon via (TSV) structures. The chip offers connectivity to a printed circuit board through either standard wire bonding or via TSV technology. Wire-bond extenders are situated at the upper and lower edges of the ASIC, enabling wafer-level probing and single ASIC wire bonding without the necessity of TSV processing (at the expense of 93.5% of active area). The wire-bond extenders can be removed by dicing when input/output interconnections are established with TSV processing. The dicing is performed along the red dashed line depicted in the magnified inset on figure 1 and located 75 µm from the first bump-pad (and symmetrically from the last). In the TSV scenario, the die size is reduced to 24.075 mm $\times$ 24.075 mm, covering 99.37% of the active area without compromising chip functionality.

The Medipix4 chip is designed to operate in two primary acquisition modes: *single pixel mode* (SPM) and *charge summing mode* (CSM). In SPM, each pixel operates like conventional single-photon counting architecture, operating independently from its neighboring pixels. Conversely, in CSM, the inter-pixel architecture reconstructs the total charge within overlapping clusters of 2×2 pixels, guided by an arbitration circuit that allocates the hit to the pixel with the highest charge deposition. The complete reconstructed charge is then attributed to the winning pixel within a neighbourhood of 9 pixels. This charge processing architecture corrects the spectral distortion that arises from charge diffusion across the sensor material [7, 15, 16].

The Medipix4 architecture proposes pixel size programmability with a 75 µm pixel pitch in *fine pitch mode* (FPM) and 150 µm in *spectroscopic mode* (SM). FPM is particularly well-suited for applications that utilize Si or GaAs as sensor materials [17], while SM is better suited for high-Z materials like CdTe, CdZnTe, or perovskite [16]. Please note that using the fine pitch pixel with high-Z materials and with no charge sharing correction could lead to multiple hit counts for a single incoming photon due to the potential deposition of fluorescence photons far from the original impact point. For instance, CdTe has more than an 80% chance of generating fluorescence photons, and the mean free path of those photons is comparable to the fine pixel size: 58 µm for Te and 111 µm for Cd [18]. Similar to Medipix3RX, both SPM and CSM are available for both sensor pixel pitches, providing four different charge collection areas. Medipix3RX with a pixel pitch of 110 µm still exhibited some escape peaks from fluorescence in CdTe, even with charge-sharing correction (providing a charge collection area of 220 µm $\times$ 220 µm) [19]. For that purpose, a 75 µm pixel pitch was selected for the Medipix4 readout pixel, enabling a larger collection area of 300 µm $\times$ 300 µm in the SM-CSM configuration.

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3 Medipix4 pixel architecture and readout

3.1 Pixel schematic and analog processing modes

The block diagram of the Medipix4 pixel cell is illustrated in figure 2. In the analog circuitry, the initial stage contains a charge sensitive amplifier (CSA) with a programmable feedback capacitance. This feedback capacitance can be configured between 5 fF, achieving the highest gain in the *low noise mode* (LNM), and 10 fF in the *ultra-fast mode* (UFM). Unlike its predecessors, the Medipix4 front-end is only sensitive to negative charges originating from the sensor (electron collection). A test injection capacitance of 5 fF allows for electrical stimuli up to 25 ke^-. The chip provides access to two separate test pulses, enabling the injection of different charges into neighboring pixels. To manage the DC leakage current from the sensor, the first stage incorporates a compensation network with the ability to accommodate currents up to 50 nA per pixel. A pole-zero cancellation circuit follows the CSA. Subsequently, the signal is directed to a pulse-shaping amplifier that offers adjustable peaking and discharge times. The new shaper amplifier demonstrated in simulation reduced baseline drift at high flux when compared to the Krummenacher feedback topology employed in previous Medipix and Timepix iterations [20]. This enhancement is attributed to the filter circuitry within the DC compensation network, featuring back-to-back connected transistors that provide a significant equivalent resistance while using small silicon area [21, 22].

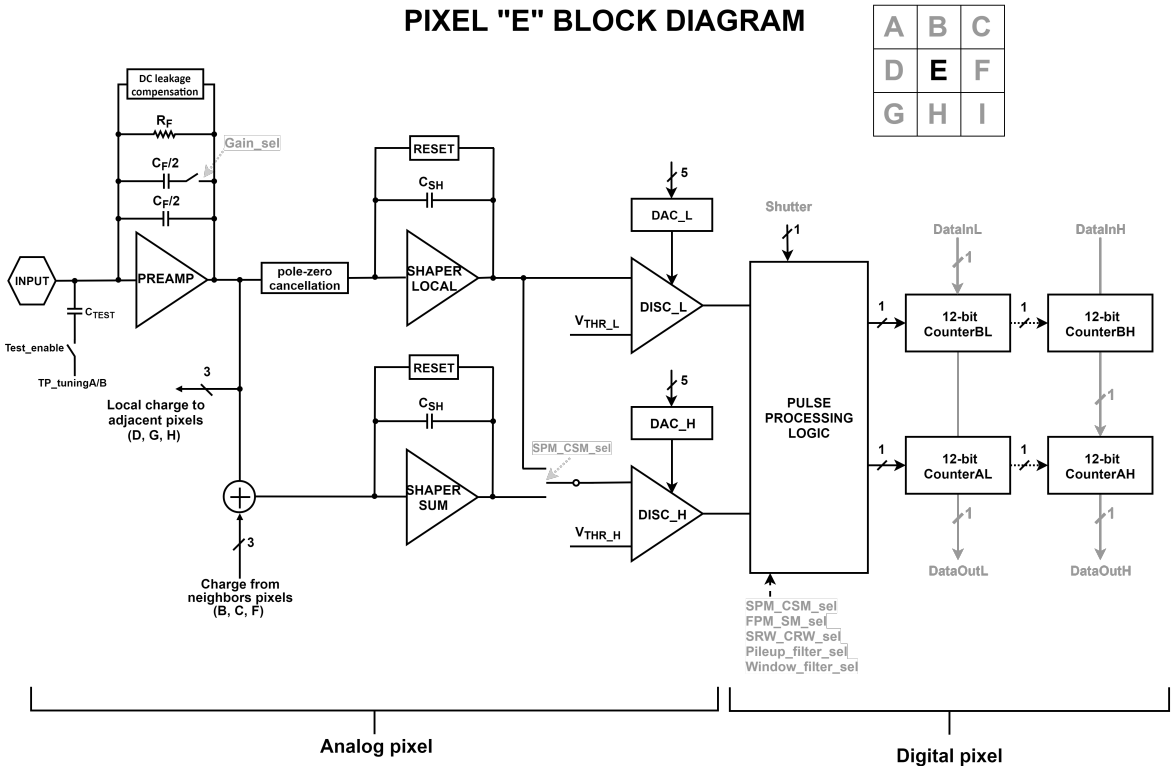

Figure 2. Simplified block diagram of the Medipix4 pixel cell. The communication of the pixel E with its adjacent pixels is shown in *fine pitch mode*.

In SPM, the shaper denoted as "LOCAL" is connected to two parallel comparators, each equipped with its own distinct energy threshold, which is independently adjustable. To address threshold

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disparities from one pixel to another, two 5-bit tuning digital-to-analog converters (DAC) are connected to the comparators, effectively compensating for any mismatches. This mode enables simultaneous imaging with dual thresholds.

The charge sharing correction is performed in CSM by enabling the summing shaper circuit called "SUM." This circuit reconstructs the charge within overlapping clusters of 2×2 pixels, thereby establishing an equivalent collection area of $150\,\mu m \times 150\,\mu m$. Each pixel sums its own contribution, as well as the contributions from pixels in its east, north, and north-east locations. In this summing mode, the noise from the four pixels is combined in quadrature, resulting in a twofold increase in the total noise. For instance, pixel E forwards its local charge to the summing nodes of pixels D, G, and H while receiving the charge contribution from pixels B, F, and C. Concurrently, a network of arbitration circuits within the digital pixel determines the pixel with the highest charge deposition among its neighbors, providing an overall 75 µm spatial resolution. This is possible using the time-over-threshold information. These steps guarantee the full reconstruction of the charge deposited in 2×2 pixels through an analog scheme, while the digital scheme allocates the reconstructed charge to a single pixel, preventing multiple counting for a single hit. This analog charge summing overcomes the limitation of sub-threshold charge loss that occurs when implementing digital charge reconstruction [23]. There is one discriminator (*DISC_L*) with an energy threshold placed above the noise floor for the arbitration of the largest charge in the local area, and a different threshold for the reconstructed charge (*DISC_H*) [24].

When programming the Medipix4 in *spectroscopic mode* (SM), the readout pixels are organized into a cluster of four pixels (labeled as P0, P1, P2, and P3 in figure 1). Among these, only the readout pixel P0, referred to as the "master" pixel, is bump bonded to the 150 µm pitch sensor pixel. The front-end circuits within the remaining three pixels ("slave" pixels) are deactivated, while their energy discriminators and counters are linked to the "master" pixel. In the scenario involving a 150 µm pixel in *single pixel mode*, a total of eight independent thresholds are accessible. However, when applying the charge-sharing algorithm with the 150 µm pixel, one energy threshold is allocated to the arbitration network denoted SPM_A, while seven thresholds are dedicated to the reconstructed charge. An overview of the different modes of operation and thresholds is provided in table 1.

Table 1. Summary of operation modes in Medipix4.

Operation modes	Spatial resolution	Charge collection area	Thresholds
FPM-SPM	75 µm	75 µm × 75 µm	2
FPM-CSM	75 µm	150 µm × 150 µm	1 SPM_A + 1 CSM
SM-SPM	150 µm	150 µm × 150 µm	8
SM-CSM	150 µm	300 µm × 300 µm	1 SPM_A + 7 CSM

The analog pixel is highly configurable to accommodate a large range of different applications. *Ultra-fast mode* (UFM), for instance, may be advantageous for applications such as computed tomography and synchrotron cameras, that require a very high count-rate capability. We simulated a deadtime not exceeding 130 ns (at 13.7 ke^- or 60 keV in CdTe). This will enable a count-rate capability up to 19×10^6 photons·mm^{-2}·s^{-1} at 10% hit loss, all while maintaining a 150 µm pixel pitch and remaining unaffected by charge sharing and fluorescence effects. This fast photon processing comes at the expense of a higher electronic noise. The latter can be improved in *low noise mode* (LNM) for a better energy resolution. Across all operational modes, the power consumption per unit area is

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intentionally maintained well below 0.5 W/cm^2. This design choice allows the chip to operate without the need for active cooling [13]. The power consumption is reduced in the 150 µm pixel configuration, wherein the front-end circuits of the slave pixel are deactivated.

3.2 Digital processing modes

Medipix4 facilitates spectral information extraction through analog pulse height analysis using two to eight energy thresholds. In general, window discrimination is used in order to optimize the counter depths, avoiding counter saturation in low energy bins seen in Medipix3RX.

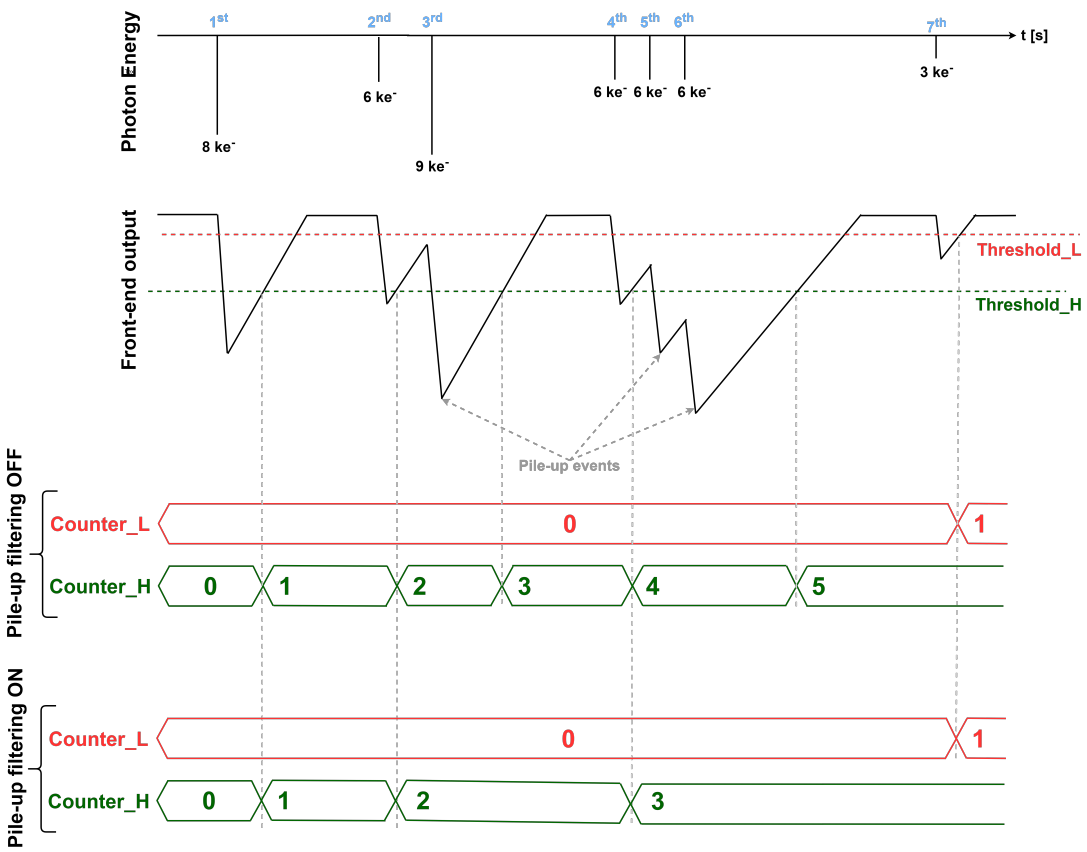

Figure 3. Working principle of the digital pixel when the chip is configured in *fine pitch mode* with *single pixel mode* and *pile-up filtering mode* enabled (and disabled for comparison) while keeping *window discrimination mode* on.

Medipix4 is designed to provide fast CT imaging capability while maintaining spectral fidelity. In addition to the charge correction algorithm, a new pile-up filtering mechanism is integrated into the digital pixel to mitigate the impact of pulse pile-up on the energy spectrum at the expense of some lost hits. Pulse pile-up occurs when the analog front-end does not return to the baseline between two consecutive events, leading to an incorrect assignment of subsequent events to their energy bins. Consequently, the system's reliability diminishes at high flux due to poor spectral fidelity in

measurements. The Medipix4 digital pixel can be configured in *pile-up filtering mode* to discard the events arriving during the discharge time of previous events. Figure 3 illustrates the pile-up filtering mechanism when the digital pixel is configured to operate in *fine pitch mode* and *single pixel mode* with *window discrimination* and *pile-up filtering*, using two thresholds (the lower energy threshold associated to *Counter_L*, placed close to the noise floor, and the higher threshold to *Counter_H*). Thanks to window discrimination, the first event is only allocated to the higher energy bin. The filtering mechanism discards events 3, 5, and 6 as the analog signal did not return to its baseline (which would have triggered the lowest energy threshold). This mechanism does not detect peak pile-up events where coincidences occur around the initial event's peaking time. Only events falling on its tail are detected by the digital pixel. Detailed measurements on the pile-up filtering mechanism and the count-rate capability of our ASIC when bonded to a sensor will be published when they become available.

3.3 Pixel matrix readout

Each pixel contains four 12-bit shift registers that function as counters during acquisition or as shift registers for reading out the collected data. The pixel readout can be programmed in *sequential read/write* (SRW) or *continuous read/write* (CRW) modes. In SRW mode, events are stored in counters that can be configured in a 1-bit, 2-bits, 12-bits, or 24-bits depth format. When the *shutter* signal is low, the counts of the energy bins are transmitted to the end of the chip column (top and/or bottom edge periphery) for subsequent readout. CRW mode enables readout dead-time-free operation for all energy thresholds in both *fine pitch mode* and *spectroscopic mode*. In this last scenario, pulses can be recorded in either a 1-bit or 12-bit depth format, while the readout is executed through the other 1-bit or 12-bit depth counter.

Table 2. Overview of readout modes in Medipix4 ASIC.

	Fine Pitch Mode (75 µm pixel)		**Spectroscopic Mode (150 µm pixel)**	
	SPM	CSM	SPM	CSM
On-pixel thresholds	2	1 SPM_A + 1 CSM	8	1 SPM_A + 7 CSM
Counter depth Sequential	$2 \times [1, 2, 12,$ or 24] bits		$8 \times [1, 2, 12,$ or 24] bits	
Counter depth Continuous	$2 \times [1$ or 12] bits		$8 \times [1$ or 12] bits	
On-pixel digital modes	Window discrimination threshold mode Pile-up filtering mode			
Readout direction modes	Split readout for independent readout from both sides Conveyor belt readout (towards top or bottom periphery)			
Output ports	1 to 16 SLVS (up to 640 Mbps per port)			

The Medipix4 pixel matrix offers two distinct readout modes: *conveyor readout mode* and *split readout mode*. *Conveyor mode* is specifically designed for scenarios necessitating a continuous scanning, like for imaging moving objects [25] or for X-ray laminography. In this configuration, the entire pixel matrix is read out via a single edge periphery utilizing 1, 2, 4, or 8 output serializers. Alternatively, in the *split readout mode*, both edge peripheries independently read out their respective 320×160 matrices through a maximum of 16 SLVS links. A full overview of the different readout modes is provided in table 2.

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The chip's maximal frame rate is contingent upon a number of parameters, including the counter bit depth (which must be chosen in accordance with the exposure time to prevent counter overflow), the pixel readout mode, the number of parallel output links (ranging from 1 to 16), and the frequency of the data acquisition clock (up to 320 MHz). For instance, the use of *split readout mode* results in a maximum frame rate that is twice as high as that achieved through the *conveyor readout mode*. Furthermore, higher frame rates can be attained by selectively reading a sub-area within the pixel matrix. This is done by specifying the number of rows in the matrix to be read out. For example, in a large multi-module detector, this feature may emulate a smaller-size detector with significantly elevated frame rates. Table 3 provides the frame rate capability of the chip in a few selected readout configurations. For instance, when configuring the chip to continuously read out a single row in 12-bit format, a frame rate of 1.176 MHz is achieved, compared to 8.32 kHz obtained by reading the full matrix. Alongside this readout feature, the number of frames and the inter-frame wait times can be programmed.

Table 3. Maximum frame-rate capability of Medipix4 for full matrix readout and partial readout.

Counter length	Readout mode	Full matrix readout	Links	Frame rate [fps]
1	Split readout & CRW	Yes	16	99 K
2	Split readout & SRW	Yes	16	49.5 K
12	Split readout & CRW	Yes	16	8.32 K
24	Split readout & SRW	Yes	16	4.16 K
1	Conveyor readout & CRW	Yes	8	49.7 K
2	Conveyor readout & SRW	Yes	8	24.87 K
12	Conveyor readout & CRW	Yes	8	4.16 K
24	Conveyor readout & SRW	Yes	8	2.08 K
1	Split readout & CRW	No, 1 row	8	6154 K
12	Split readout & CRW	No, 1 row	8	1176 K

4 Electrical measurements

A single Medipix4 chip without sensor was mounted on a printed circuit board using the wire bonding option. To enable initial electrical characterization, slight adaptations were made to the readout system SPIDR4, originally designed for Timepix4 [26], with valuable assistance from Nikhef. Access to the chip via slow control allowed for the first round of electrical tests. The test setup is shown on the left hand side in figure 4. Furthermore, dedicated efforts towards developing a specialized readout system for Medipix4 are underway. The outcomes presented in this paper concern the second iteration of Medipix4. In the first Medipix4 version, within the analog front-end pixel, the models exhibited an underestimation of the substrate leakage current in the thick oxide transistors employed as pseudo-resistors. Consequently, certain pixels within the matrix failed to lock onto the correct reference level, even after pixel threshold equalization. With the updated current version, the sensitivity to substrate leakage has been addressed. The right plot in figure 4 depicts the image of the Medipix4 collaboration logo obtained by sending test pulses to the pixel matrix and reading out the accumulated hits in the two counter bins. In this case, the chip was configured in *fine pitch mode* and *single pixel mode*. Only 21 pixels are masked, demonstrating a good yield after threshold equalization.

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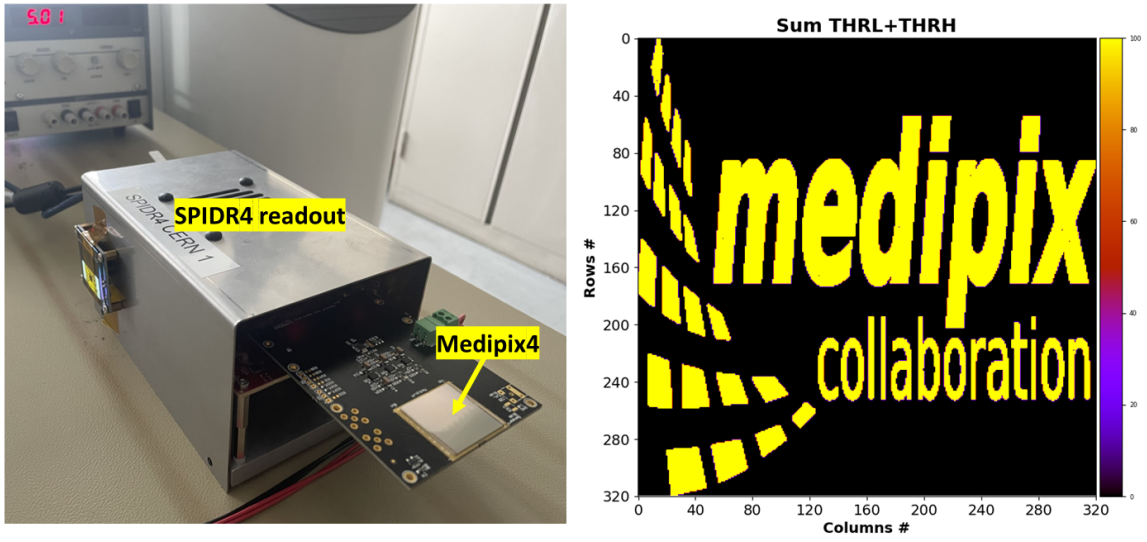
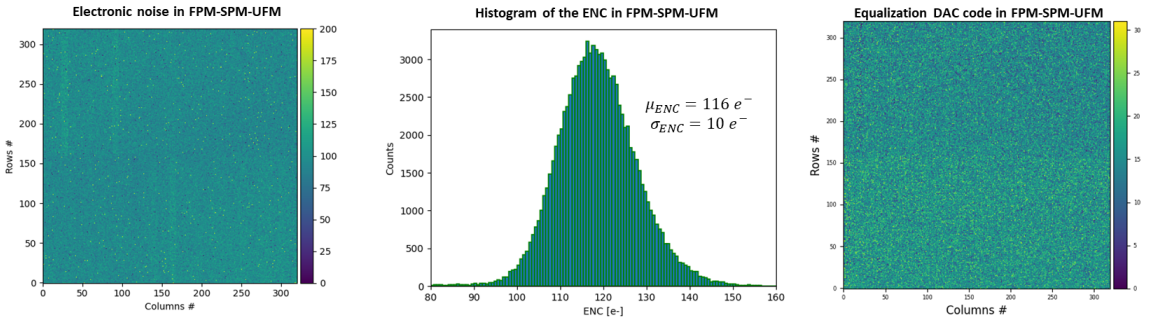


(a) (b)

Figure 4. (a) shows the Medipix4 chip mounted on a printed board circuit using the wire bond extenders option and read out using the SPIDR4 system. (b) The full chip imaging using test-pulses when the pixel is configured in FPM-SPM and with two thresholds. 21 pixels were masked during this measurement.



(a) (b) (c)

Figure 5. The measured electronic noise in r.m.s. electrons when the chip is programmed in FPM-SPM for which the analog front-end configured in *ultra-fast mode* (a) and the histogram (b). (c) The pixel DAC code for equalization exhibits a minor systematic offset between the top and bottom matrices, arising from a slight deviation in the pixel reference definition for the two matrices. It is important to highlight that, despite this marginal offset, the threshold dispersion following pixel equalization consistently maintains a magnitude smaller than the electronic noise, as illustrated in table 4.

Figure 5 presents the measured electronic noise when configuring the analog front-end in *ultra-fast mode*. The measured noise matches with the expected values, with a mean noise level of 116 e^- and a dispersion of 10 e^- r.m.s. Please note that these measurements are performed on a bare readout chip using the electrical test pulses. The precision of these measurements relies on knowledge of the test pulse capacitance, which carries a tolerance of approximately ±30%. For a more precise assessment of the front-end parameters, a subsequent measurement will be undertaken using radioactive sources following the flip chip bonding of the readout chip to a sensor.

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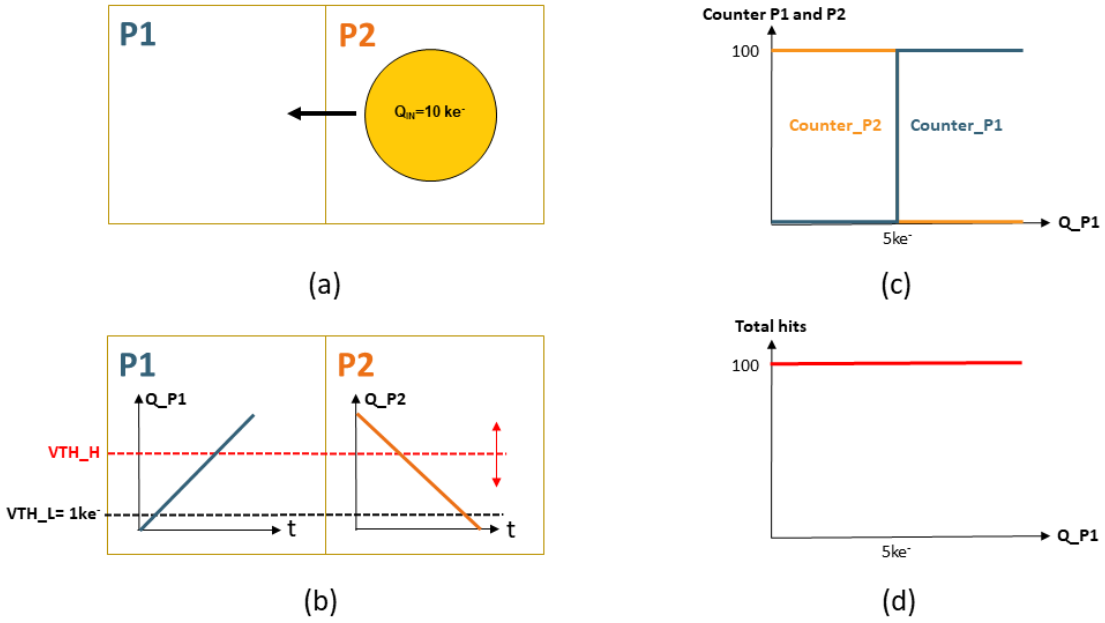

Figure 6. (a) depicts a scenario wherein a 10 ke$^-$ input charge is moved from the right sensor pixel P2 to the left sensor pixel P1. (b) displays the charge distribution at the front-end input for both pixels, resulting from charge sharing at the pixel edges. (c) illustrates the ideal pixel response, where the counter associated with the higher energy threshold (VTH_H) is capable of accurately reconstructing both the energy and spatial characteristics of incoming hits. It is important to note that this holds true when the higher energy threshold is set lower than the input energy. (d) shows the total hits registered by both pixels in an ideal case, highlighting the absence of hit loss or multiple counts.

A total input charge of 10 ke$^-$ was injected with test pulses to a cluster of two pixels as seen in figure 6. More specifically, 100 consecutive test pulses were distributed across various coordinates within the matrix. Similar to situations involving charge diffusion in thick sensors (in this example from right pixel P2 to the left pixel P1), we distribute the charge in such a way that a portion, denoted as Q_P1, was directed to pixel P1, while the remaining charge (10 ke$^-$ – Q_P1) was collected by its neighboring pixel, P2. The lower energy threshold VTH_L was set at 1 ke$^-$, while the higher threshold VTH_H could be configured to an energy lower than 10 ke$^-$. An ideal pixel detector should possess the capability to accurately reconstruct both the energy and spatial distribution of each incoming hit, without encountering issues of hit loss or multiple counts, under any setting of VTH_H lower than 10 ke$^-$. The ideal response of the counters associated with the higher energy threshold for both pixels is depicted in figure 6(c), and figure 6(d) illustrates the total hits registered by both pixels, showcasing the absence of hit loss or multiple counts.

Figure 7 shows the measured response of the pixels in *fine pitch mode* without charge sharing correction and after threshold equalization. The lower energy threshold was set at 1 ke$^-$, while the higher energy threshold is set at 2.5 ke$^-$ (a), 5 ke$^-$ (b), and 7.5 ke$^-$ (c). The upper plots depict the hits recorded by the higher energy bin for both pixels, P1 (blue) and P2 (orange), while the cumulative hits are presented in the bottom plots (red). These plots illustrate the consequences of charge sharing between pixels, which vary depending on the higher energy threshold level. Setting the higher energy threshold lower than half of the input energy (VTH_H = 2.5 ke$^-$) leads to the registration of hits

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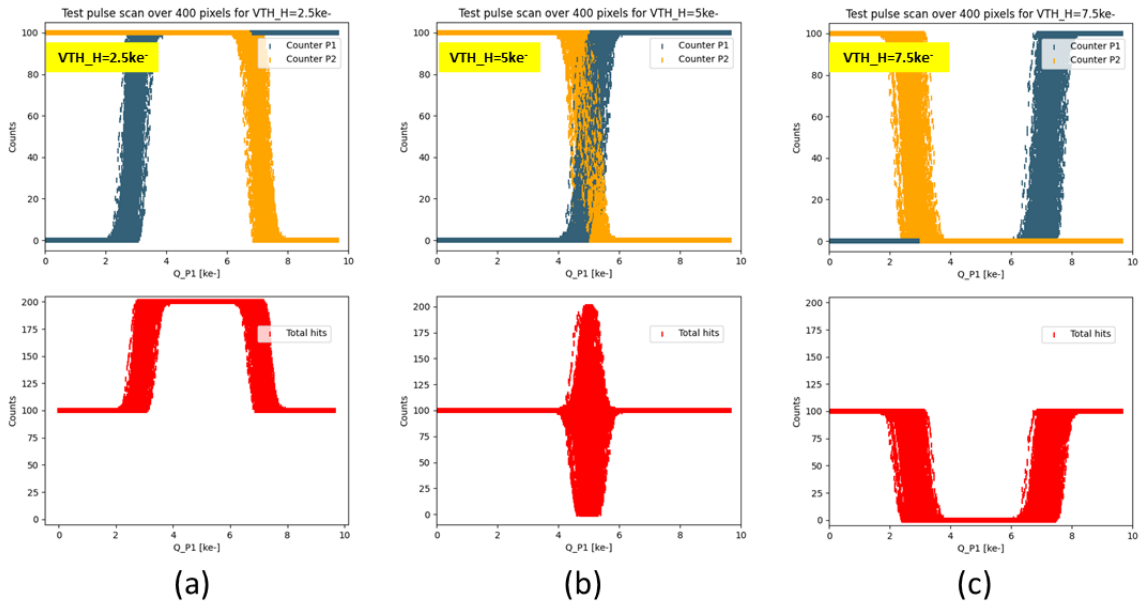

Figure 7. Charge sharing effects between pixels when the chip is configured in *fine pitch mode* and *single pixel mode* depending on the energy threshold level: 2.5 ke^- (a), 5 ke^- (b), and 7.5 ke^- (c). In (a), both pixels record counts in the 2.5 ke^-–7.5 ke^- range. The multiple registration of hits near the edges or corners between pixels results in poor imaging. In (c), neither of the pixels records counts in the 2.5 ke^-–7.5 ke^- range, indicating that hits occurring near the pixel edges or corners go undetected. (b) offers a favorable compromise for accurately reconstructing the energy and spatial position of incoming hits but may not be replicable in the case of a polychromatic input beam.

near the edges or corners between pixels multiple times. This results in blurred imaging due to charge sharing (and further with fluorescence photons not considered in this setup). Conversely, when employing the higher energy threshold close to the input peak energy (VTH_H = 7.5 ke^-), the hits sharing charge between pixels go undetected. In this scenario, pixels appear to be smaller than their actual size. To mitigate these effects, setting the higher energy threshold at half the input energy may provide a reasonable compromise. However, it's important to note that such effects cannot be controlled in the case of a polychromatic input beam, necessitating on-pixel charge sharing and fluorescence correction mechanisms. Figure 8 illustrates the behaviour of the pixels when configuring the chip with charge sharing correction. In this setup, regardless of the chosen higher energy threshold level, which is set lower than the input energy, each hit is accurately counted once and only once, with no instances of undetected hits. The implementation of this algorithm ensures precise energy and spatial reconstruction for every event, ultimately leading in excellent spectral fidelity.

A full summary of the electrical measurements in the eight different mode of configurations is provided in table 4. As a key figure, in *ultra-fast mode*, the linear dynamic range of the front-end extends to 42 ke^-, which is equivalent to 185 keV when employing a CdTe sensor. This signifies more than 50% improvement compared to Medipix3RX. In *low noise mode*, the readout noise remains comparable to that of its predecessor. Importantly, these crucial front-end achievements are realized while maintaining the full chip static power consumption below 0.5 W/cm^2.

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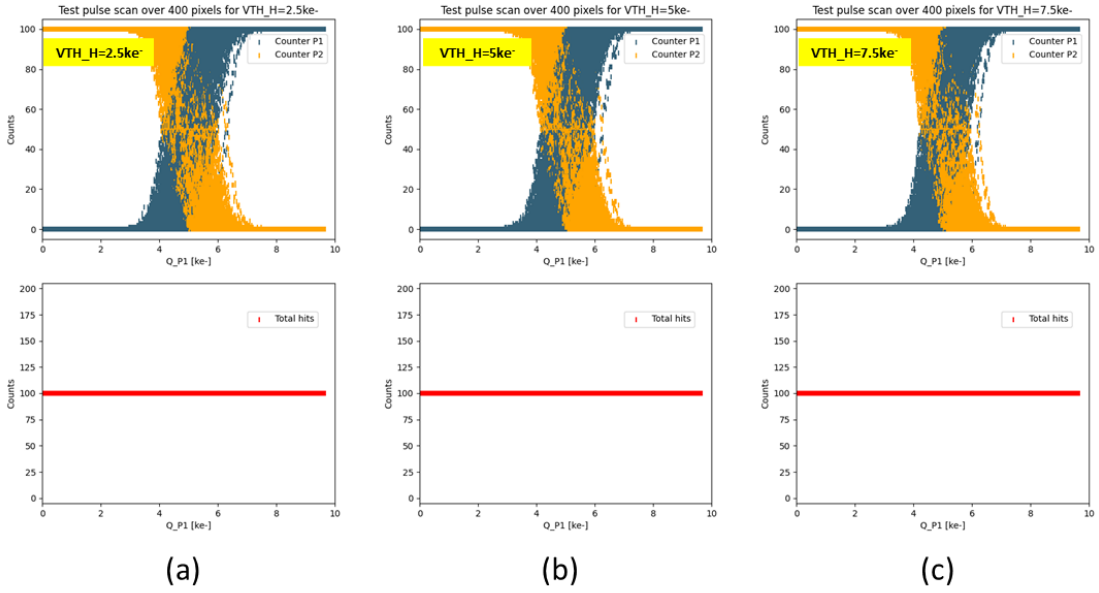

Figure 8. Charge sharing effects between pixels when the chip is configured in *fine pitch mode* and *charge summing mode* depending on the energy threshold level: 2.5 ke$^-$ (a), 5 ke$^-$ (b), and 7.5 ke$^-$ (c). Please note that, irrespective of the settings of the higher energy threshold, the s-curves are centered at 5 ke$^-$, showcasing the analog summing capability in *charge summing mode*. Furthermore, each hit is precisely counted once and only once, with no occurrences of undetected hits.

Table 4. Electrical measurements of Medipix4's front-end in the different mode of operations. The characterizations were conducted on a bare readout chip using electrical test pulses and assuming a 5 fF test pulse capacitance ($^*\pm30\%$ accurate and **limiting the input charge to 25 ke$^-$).

	Fine Pitch Mode (75 µm pixel)				**Spectroscopic Mode (150 µm pixel)**			
	SPM		CSM		SPM		CSM	
	UFM	*LNM*	*UFM*	*LNM*	*UFM*	*LNM*	*UFM*	*LNM*
Pixel gain (mV/ke$^-$)	10.3*	19.8*	10.6*	18*	10.4*	20.1*	9.4*	19.4*
Gain variation (%)	< 3	< 2	< 3	< 2	< 3	< 2	< 3	< 2
ENC (e$^-$) for bare chip	116*	77*	178*	117*	107*	68*	172*	105*
Dynamic range (ke$^-$)	> 25**	> 25**	42	28	> 25**	> 25**	42	28
Threshold dispersion before equalization (e$^-$)	953	524	1430	735	1185	570	1300	770
Threshold dispersion after equalization (e$^-$)	77	40	150	95	81	39	125	83
Minimum detectable charge (e$^-$)	830	520	1400	900	800	475	1275	800
Full chip static power consumption (W/cm^2)	0.46	0.46	0.47	0.47	0.31	0.31	0.36	0.36

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5 Summary and future plans

In this work, we have presented the Medipix4 hybrid pixel detector readout ASIC, describing its architecture and implementation along with the first electrical measurements. The charge sharing correction algorithm works as expected from the simulation. The front-end of the Medipix4 chip can be configured in two different analog modes: *low noise mode* (LNM) and *ultra-fast mode* (UFM). In LNM, the measured electronic noise is $72\,e^-$ r.m.s. using fine pitch configuration without charge sharing correction. In UFM, we expect a linear range up to $42\,ke^-$, showing 50% improvement compared with Medipix3RX. These performance enhancements compared to its predecessor are achieved at the expense of a slightly larger spatial resolution. The latter should not be a problem since studies have indicated that the optimal pixel pitch when using high-Z materials should be slightly larger than the Medipix3RX pixel in order to account for a larger fraction of fluorescence photons. Detailed measurements of this readout coupled with a sensor will be published when they become available.

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