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Particle physics experiments: From photography to integrated circuits

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ABSTRACT

Over the last decades the experiments in elementary particle physics at the new colliding beam accelerators with TeV energy, in particular the LHC at CERN, have seen profound changes. These present orders of magnitude increases in physical size, interaction rates, radiation intensity and data volume. Not only new instruments such as segmented and pixelated silicon detectors, but also calorimeters and surrounding muon detectors feature a much larger number of sensing elements. This provides improved precision in particle tracking and momentum measurement, avoiding a need for even larger overall detector dimensions. Associated silicon integrated circuits, specifically designed for these applications, improve the speed and reduce the electrical power for signal processing and information extraction. Now the detectors can cope with near-GHz interaction rates, more than 1000-fold the rate at the LEP collider ~1995, and produce distinctive reconstructions of interactions with μm-level precision, even with hundreds of simultaneous particles. All this in the inherently severe radiation environment up to tens of Mrad. The unconventional exploitation of silicon chip technology for radiation sensing and large-scale parallel signal processing has been the most important enabling factor. Some of the successive steps in the introduction of the silicon devices are described here in a narrative way, and with an unavoidable personal bias of the author. General characteristics of this electronics are outlined, including a brief description of IC manufacturing technologies. The focus is on the inner vertexing and tracker systems, which profited most of the miniaturization. References are made to further articles in the special issue, which treat in more detail the instruments and associated circuits for readout, precision timing and voluminous data transmission, by wire or optical fiber. In the margin, historical circumstances are indicated, which made the 'silicon revolution' possible and affordable for high energy physics.

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1. Introduction

Electronic instruments have become the standard tools for measuring anything, and with few exceptions have eclipsed purely mechanical or optical devices. Moreover, beyond the sensing front-part, instruments now also incorporate microelectronic integrated circuits, ICs, called 'chips', which manage the sequence of initialization, measurement, data recording, data transmission, storage, analysis and presentation of the relevant information. Also in elementary particle physics, this shift towards integrated electrical, digital processing has shaped the experiments over the last decades. This article aims to illustrate some of the steps in the evolution from mostly photographic methods to the fully digitized equipment of today's particle physics experiments. Other articles in this dedicated issue of the journal treat in more detail various aspects of specially developed ICs for elementary particle physics. Especially the work on complex circuits for data transmission and timing has become a large part of the effort, because of the increase in production rate and volume of data. However, in this introductory article the author, not a specialist in these subjects, will present only a few aspects on it, and readers should not expect a full historical overview. Some parts such as calorimetry and muon momentum measurements have been practically neglected. The emphasis here is on the progressive use of microelectronics as such, with illustrations of a learning curve in the adoption of this new approach.

Some fundamental concepts and functions in the readout electronics are described first. An overview of early electronics follows, with the narrative in large part based on the personal experience and involvement of the author. Chapter 5 offers a brief description of processes in silicon IC manufacturing, to support later discussions on radiation effects. In the main chapter 6, a number of milestones and developments are mentioned, mostly from the early years 1973–1995. The sensors themselves will not be treated much, although the electronics design always must be intimately matched to the sensor characteristics. Optimization needs co-design of sensor and IC. Silicon detectors will be mentioned when these happened to provide critical connections to specialists in silicon processing technology, the basis of ICs.

Obviously, also in the particle accelerators, advances in electronics have played a decisive role for progress towards ever higher kinetic energies and higher intensities. This will not be covered in this special issue. Still, the properties of the sensors and the electronics in the experiments are dictated to a large extent by the accelerator characteristics. This especially includes the severe radiation environment created by the intense beams, around their interaction-point in the center of the experiment set-ups.

Radiation-hardening will be briefly discussed in Section 6.12, and in more detail by Federico Faccio [1] and by Paulo Moreira and Szymon Kulis [2] in their contributions in this issue.

As mentioned already, an application area of microelectronics, which will hardly be touched upon, is the processing of the massive amounts of data, which takes place both 'on-line' and 'off-line'. Elementary particle physics has been an early adopter of electronic computers, at CERN in particular, starting in 1958 with a UK-produced Ferranti 'Mercury' computer, and installing in 1972 one of the first large CDC7600 main-frames from Control Data Corporation. Already in the 70's and 80's, at CERN original developments on data sharing networks got underway, and eventually ideas came up for use of the worldwide DARPA internet. The collaborations for the large LEP experiments looked for possibilities of distributed data analysis. Tim Berners-Lee, with Robert Cailliau working in this domain, developed the hypertext protocol and serendipitously[1] invented the World-Wide-Web WWW [3]. For the LHC era the secure LHC Computing Grid [4] was developed, see https://wlcg-public.web.cern.ch/ which originally was expected to become the largest world-spanning network. However, the efforts in physics quickly were dwarfed by the commercial and lucrative exploitation of the Web by giant companies such as Google and Facebook.

In this article, the author aims to provide a sketch of the evolving electronics landscape and relevant detector properties, with the steps that brought us to the present 'silicon age'. Some of the author's personal experience is reported, especially to illustrate how progress often comes about by random personal encounters all around the world. Finally, in chapters 8 and 9, arguments will be made, to further exploit the ever increasing capabilities of the recent electronic technologies, so that we can continue to improve our acces to physics at the infinitely small scale(see Fig. 1).

2. Photography or electronics

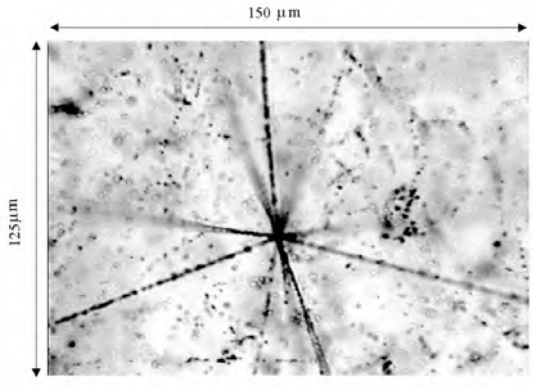
For a long time, from 1890 until ~1980, a majority of elementary particle discoveries was based on photography. Unknown particles or nuclear processes could be found via their interaction, either directly with the sensitive emulsions, or via pictures from cloud, spark or bubble chambers, exposed to natural cosmic rays or artificial, accelerated particle beams. The ionizing energy deposited by the swift, charged objects along their trajectories, resulted in clear, visible tracks with a large number of concatenated bubbles or silver grains, formed in the sensitive material, as shown in Figs. 1a–b. Although considered here as opposed to detection methods using electrical instruments, the photographic process itself is electrochemical, like other complex, natural processes, of which photosynthesis in plants is a prime example. The detailed photographic exposures to ionizing particles provided convincing visual information, and often a discovery could be based on a few images, or even a single one. At the relatively low energies studied in the 50's and 60's, interaction products were mostly contained within a stack of nuclear emulsions, or the volume of a bubble chamber. Photographs have large redundancy, if compared with today's instruments, where particle trajectories are often derived from only a few measured space coordinates. However, in the search for rare phenomena, the inspection of photographic material becomes a difficult task. The analysis of millions of bubble chamber photographs therefore, became from ~1965 progressively 'computerized' using scanning tables that could digitize and reconstruct the 3D coordinates of the projected tracks. A large number of scanning people first had to find the exposures with a 'good' interaction. Among many discoveries with the bubble chambers around the world, at CERN the most noteworthy would be that of the 'weak neutral current' in 1973, after scanning more than a million exposures from the Gargamelle (GGM) bubble chamber, in the CERN 25 GeV neutrino beam, which confirmed the prediction of a neutral Z boson [5]. In Section 6.2 the neutrino beam will be mentioned again, because silicon detectors were used for its monitoring.

[1] The 3 princes from 'Serendip' exploited chance encounters and observations of incidental objects along their journey, for solving problems they were facing. [https://en.wikipedia.org/wiki/The_Three_Princes_of_Serendip]

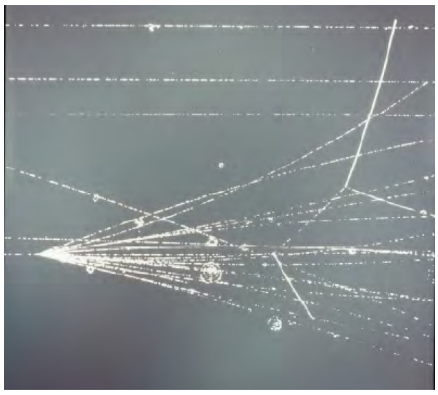
List of Abbreviations

ADC	Analog to Digital Conversion
AIEA	Agence Internationale d'Energie Atomique, English see IAEA
ALICE	A Large Ion Collider Experiment
ALEPH	Apparatus for LEP PHysics experiment at LEP
ALTRO	ALice Tpc ReadOut ASIC
ASIC	Application Specific Integrated Circuit
ATLAS	A Toroidal Large Acceptance Spectrometer
BEBC	Big European Bubble Chamber CERN special project, funded by France and Germany
BiCMOS	combined Bipolar Complementary Metal–Oxide–Semiconductor
CAD	Computer Aided Design
CAMAC	Computer-Aided Measurement And Control
CCD	Charge Coupled Device
CDC	Control Data Corporation supplier of main-frame computer systems
CDF	Collider Detector Fermilab
CEA	Commission de l'Energie Atomique France (Atomic Energy Commission)
CERN	Centre Européen pour la Recherche Nucléaire Elemetary particle physics laboratory, Genève
CHARM	neutrino experiment by the collaboration **Cern-Hamburg-Amsterdam-Rome-Moscow**
CIS	Center for Integrated Systems at the electrical engineering department Stanford
CMOS	Complementary Metal–Oxide–Semiconductor logic silicon circuit technology
CMP	Chemical Mechanical Polishing
CMP	Circuits Multi Projets Broker organisation to IC foundries in Grenoble
CMS	Compact Muon Spectrometer experiment at the LHC
CNRS	Centre National de la Recherche Scientifique France
CRNS	Centre de Recherches Nucléaires de Strasbourg
CSEM	Centre Suisse d'Electronique Miniaturisé
DARPA	Defense Advanced Research Project Agency in USA
DELPHI	DEtector with Lepton, Photon and Hadron Identification experiment at LEP
DESY	Deutsches Elektronen SYnchrotron Hamburg
DMILL	Durci Mixte sur Isolant Logico-Linéaire IC technology with Mixed Analog-Logic on Insulator
ECFA	European Committee for Future Accelerators
ECL	Emitter Coupled Logic high speed bipolar transistor integrated circuits
ENC	Equivalent Noise Charge r.m.s. in units of electrons of distribution of noise signals
EPFL	Ecole Polytechnique Fédérale de Lausanne
ESAT	Department 'Elektrotechniek' Catholic University Leuven Belgium
ESONE	European Standards On Nuclear Electronics
ETHZ	Eidgenossische Technische Hochschule Zürich
EUV	Extreme Ultra Violet 13.5 nm light used for silicon lithography
FILAS	name of p-MOS circuit made in 1973 by CEA-LETI
FPGA	Field Programmable Gate Array
FWHM	value of Full Width at Half Maximum of distribution of data
GGM	GarGaMelle heavy liquid bubble chamber at CERN 1970–1979
HARP	Hierarchical Analog Readout Processor
HEP	High Energy Physics 1950 ~1GeV; 1960 ~25GeV; 1970~75GeV; 1980~400GeV; 1990~1000GeV etc.
HERA	High Energy Research Accelerator electron–proton collider at DESY Hamburg 1992–2007
IBM	International Business Machines company
IC	Integrated Circuit
ICFA	Intenational Committee for Future Accelerators
IAEA	International Atomic Energy Agency agency of UN, headquarters in Wien, French name AIEA
IEEE	Institute of Electrical and Electronic Engineers internatiol professional organization
IMEC	Interuniversitair Micro Electronisch Centrum Universities Leuven-Gent-Brussel-Limburg
INVOMEC	Industriële VOrming in Middelbaar EleCtrisch onderwijs education body in Flanders, Belgium
IR	Infra Red light
ISR	Intersecting Storage Rings first proton–proton collider at CERN

ISSCC	International Solid State Circuit Conference organized yearly by IEEE
L3	Third experiment at LEP
LAA	Lepton Asymmetry Analyzer R&D program at CERN, funded by Italy
LAL	Laboratoire de l'Accélérateur Linéaire near Paris
LETI	Laboratoire d'électronique et de technologie de l'information based in Grenoble, part of CEA
LEP	Large Electron Positron particle collider at CERN
LBL	Lawrence Berkeley Laboratory now LBN (National) L
LHC	Large Hadron Collider at CERN
LHCb	Large Hadron Collider bottom physics experiment at the LHC
LOCOS	LOCal Oxidation of Silicon
MIT	Massachusetts Institute of Technology
MOS	Metal–Oxide–Semiconductor
MOSFET	Metal–Oxide–Semiconductor Field Effect Transistor
MOSIS	Metal–Oxide–Semiconductor Implementation Service 1981 https://themosisservice.com
MPW	Multi Project Wafer
MWPC	Multi Wire Proportional Chamber
NA	North experimental Area location prefix for experiments at CERN
NATO	North Atlantic Treaty Organization
NBS	National Bureau of Standards USA current name NIST
NFM	Neutrino Flux Measurement in CERN SPS neutrino beam
NIM	Nuclear Instrumentation Module
NRL	Naval Reseacrh Labortory Washington DC
NSREC	Nuclear and Space Radiation Effects Conference organized yearly by the IEEE
OTA	Operational Transconductance Amplifier
OPAL	Omni-Purpose Apparatus for Lep experiment at LEP
PASA	Pre Amplifier and Shaper Amplifier
PCM	Pulse Code Modulation electrical encoding method for communication, including digitization
PEP	Positron Electron Project collider ring at SLAC
PHASE	Physique et Applications de Sémiconducteurs Laboratory at CRNS near Strasbourg
RAL	Rutherford Appleton Laboratory near Oxford
r.m.s.	root mean square or sigma value of distribution of data
SACMOS	Self Aligned Contacts MOS
SEMICON	CONference organized by SEMIconductor equipment manufacturers organization
SLAC	Stanford Linear Accelerator Center
SOI	Silicon on Oxide Isolation
SPICE	Simulation Program with Integrated Circuit Emphasis
SPS	Super Proton Synchrotron accelerator at CERN
SSC	Superconducting Super Collider
STI	Shallow Trench Isolation in Si processing
TPC	Time Projection Chamber
TSC	Thermally Stimulated Current method to determine defect energy levels in semiconductor diodes
TSMC	Taiwan Semiconductor Manufacturing Company
UK	United Kingdom
UN	United Nations
USA	United States of America
USB	Universal Serial Bus standard for data transmission and connections
VELO	VErtex LOcator inner silicon tracking and vertex detector in LHCb
VLSI	Very Large Scale Integration
VME	Versa Module Eurocard computer bus standard ANSI/IEEE 1014-1987 - VME320 1997 320MHz
WA	West Area location prefix for experiments at CERN
WWW	World Wide Web initiated by Tim Berners-Lee with Robert Caillau at CERN



1a) neutrino interaction in emulsion, recorded in the CHARM experiment ~1995 (photo CERN)



1b) beam and interaction in the 2-m CERN bubble chamber ~1970 (photo CERN)

Fig. 1. Use of photographic emulsion or film for particle detection. The detailed view of the grains or bubbles generated by energy deposition along the trajectories convincingly shows the passage of the small, themselves invisible particles, basic quanta of energy and mass. Such photos even today are used to illustrate elementary particles in publications in the press.

In parallel, various teams conducted experiments which used purely electronic devices such as ionization chambers, scintillators with photomultipliers, or semiconductor particle detectors. Germanium and also silicon detectors became possible and popular from ~1955, mostly in nuclear physics studies, because these could measure in a small volume the characteristic energy values of emitted quanta such as alpha particles, electrons or gammas, eventually with a precision ~0.1 keV on the energy peak FWHM, corresponding to ~30 electrons r.m.s. These early electronic experiments were usually limited in the number of sensing elements because signal processors were still bulky, using vacuum electron tubes, such as the 1955 preamplifier in Fig. 2, from the company Laben in Milano. At that time, germanium and silicon diode nuclear detectors started to be commercialized by different companies, and these also offered matched electronic readout. Ed Fairstein of Tennelec Instruments, Oak Ridge, in 1961 still discussed which vacuum tubes would be best suited for charge sensitive pulse amplifier designs [6]. He explained also that noise for these capacitive sources would be better expressed as Equivalent Noise Charge ENC in e^- r.m.s. at the input, contrary to noise figures for resistive sources in electronics for communication. An earlier, and even more important milestone was the development of electronic signal digitization for the nuclear measurements, by Wilkinson in Cambridge [7] and Gatti in Milano [8]. Wilkinson writes that his instrument 'snugly fits in a 19-inch rack'. An electromechanical 'kick-sorter' with small metal balls, also used in Cambridge for showing energy spectra, quickly became obsolete. This Wilkinson ADC[2] apparently preceded equivalent instrument development in telecommunications. This has been documented by Anghinolfi and Heijne [9], and was unfortunately overlooked in the standard history of ADC by Kester [10,11]. Interdisciplinary research, and especially exchange of information and experience between different branches of science and technology, remains a matter of chance.

From ~1965 vacuum electron tubes filled only niche applications, such as in plasma physics. Nuclear instruments were then built using the more compact semiconductor devices, primarily Ge or Si bipolar junction transistors and various miniature passive components. International specialist conferences were organized by the Institute of Electrical and Electronic Engineers IEEE, and also by e.g. the Organisation for Economic Co-operation and Development OECD or the

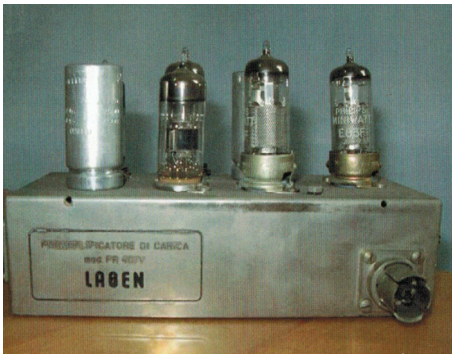


Fig. 2. Nuclear Detector Preamplifier, using vacuum tubes, ~1955. Commercialized by Laben, based on circuit designs by Emilio Gatti (photo Politecnico Milano).

International Atomic Energy Agency IAEA. These symposia on semiconductor detectors and electronics ('colloques' in French) attracted large participation in Paris, 1958 organized by the IAEA, or AIEA in french [12], in Versailles, 1963 organized by the OECD [13], in Liège, 1963 [14] and again in Versailles, 1968 [15]. In the 1964 IEEE Nuclear Science Symposium, Veljko Radeka presented the Junction Field Effect Transistor JFET for front-end signal amplification at cryogenic temperatures, which turned out to be the key to low noise performance with Ge detectors [16]. This led to the excellent nuclear energy spectra, mentioned before, and identification of elemental composition of materials in many applications. In the next chapter 4 will be discussed several coordinated efforts, which aimed at standardization of instruments for use in nuclear science.

15 years after Wilkinson, another 'home-made' digitizing instrument is illustrated in Fig. 3, now using transistors, but still it takes half a m^2 of area for one 13-bit and three 9-bit converters [17]. Sixty-four of these boards equipped the pioneering nuclear experiment 'BOL' in Amsterdam, Fig. 4, where a spherical array of segmented silicon detectors was used to analyze the angular characteristics of nuclear interactions by different particle beams from a cyclotron [18,19]. The 13% solid angle coverage around the target was still far from the near-hermeticity which nowadays is required in the LHC experiments. With only a few particles emerging from typical nuclear interactions, this partial coverage and also the single-port delay-line readout of each 'checker-board' sensor with 100 segments, was at the time fast enough for the low event rate. This 'trailblazing' multi-channel experiment (8192 elements) was later followed by similar instruments, such as

[2] Wilkinson and Gatti used really a 10-digit conversion, based on zero-to-nine telephone equipment, while today simple binary conversion is used. Therefore, one ought to have named this method: Analog-to-Binary-Conversion ABC, instead of ADC. The term ADC only became fashionable from ~1975. Telecom specialists earlier included digitization in the coding method, designated as Pulse-Code-Modulation PCM.

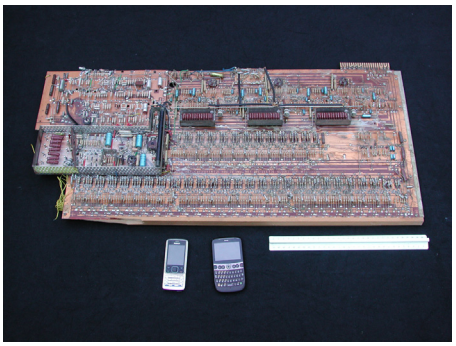


Fig. 3. Printed circuit board from 1964, with one 13-bit ADC and 3 ADC for 9-bit conversion. Used with the BOL experiment in Amsterdam. Smartphones shown as a comparison (photo by the author).

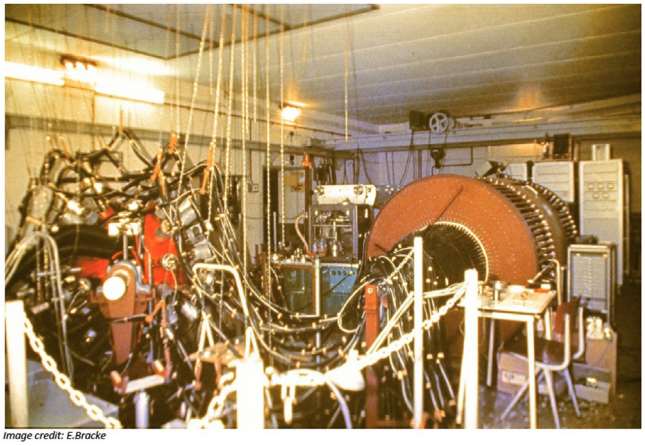


Fig. 4. Overview of the BOL experiment: the detector and on the side, the associated electronics (photo Erich Bracke).

the 'Crystal Ball' detector at SLAC [20], actually 98% hermetic, or the 'Cactus' detector at the cyclotron in Oslo [21]. The term 'channel' here indicates the sensing element, but often 'channel' comprises the full chain of sensor, signal processor, and up to final output data. Usually, in particle physics readout architectures, at some stage in the processing, the originally parallel signals are serialized, and then only a single port serves for the recording of all data, and the term 'channel' becomes very confusing. Early on, this serialization took place in the off-detector electronics, but since ASICs were introduced, often it is implemented already on the 'front-end' readout. In consumer cameras, for example, most imaging devices have only one serial output 'channel', but exploit millions of sensing pixels. In HEP it would make sense to standardize different terms instead of 'channel'.

3. Some fundamental aspects of electronics in the experiments

In order to reconstruct all details of an interaction, not a single ionizing particle should be missed, and neutral particles, as much as possible, should be made to convert into observable ionizing ones. The collision point is surrounded with sensing instruments, as much as possible, and angular coverage approaches 4π. Detection efficiency is the first requirement for a detection system in experimental particle physics. At the same time, the system should not produce fakes, resulting from excessive electronic noise. Ideally, if a signal is delivered, it always means that an ionizing quantum has entered the detector. Neither this article, nor others in this special issue on electronics, aim to review the many different approaches to particle detection, but it is essential to keep in mind that performance and constraints of a detecting instrument are determined by the electronics for the signal processing. Sensor and signal processing have to be optimized together. In other publications, often the sensors are discussed in extenso, while the electronics is left to imagination, as in a well-intended 1960 proposal for a particle tracking device[3], Fig. 5 [22], based on silicon diodes, which had then just been introduced.

The first operation behind the sensing element is the analog signal processing with a 'front-end' circuit, usually called preamplifier. Many details will be treated in this issue in the contribution by Jan Kaplon [23]. As mentioned in Section 2, its noise is best expressed as the r.m.s. value in electrons referred to the input, so that the signal-to-noise ratio can be conveniently determined if also the signal amplitude is measured as charge in electrons. Optimization of the noise performance is the important task of the analog circuit designer. Keep in mind that often it may be possible to improve the overall system performance by optimizing the sensor, e.g. by reducing noise with a smaller sensor capacitance, or by somehow increasing the intrinsic signal from the sensor. Examples are the charge multiplication in a high electric field around the signal wire in an ionization chamber, or electron multiplication in a microchannel plate.

Apart from the different sources which cause noise, shifts at the output in the absence of a signal, can also occur for other reasons. Techniques have been designed to correct for these, such as base line restoration, double-correlated sampling, etc. A basic difference appears between circuits which use an amplifier feedback loop with continuous sensitivity, and those which need a switching operation. In this context, it is essential to distinguish between experiments with asynchronous events, such as in a continuous beam on a fixed target, and experiments in which particles interact synchronously with a precisely predictable repetition rate. In the latter case, switching and sampling can be applied. Finally a signal is presented at the output of the signal processing chain, after current integration during a definite period, or using a sample/hold circuit that keeps the maximum value encountered.

Following the analog signal processing, usually more or less complex real-time logic operations are required. Comparators can be used to select only signals which exceed an (often programmable) threshold value, or which fall within a window. Comparators often are called discriminators, if they are set so as to accept only real signals which exceed the noise level. Already in early nuclear physics experiments, as a basic function, it was needed to correlate the signals from several, more or less simultaneous, products from an interaction. Electronics circuits can determine coincidences in time for two or more signal channels. In high-energy accelerator experiments, determining coincidences may be more complex, as the reactions produce a much larger number of particles, which pass through sensors at different distances from the original interaction point. In the past, such differences in time could be compensated by adding cables with precisely cut length, but today this can be achieved using much cheaper Si chips, with adjustable delay lines. Moreover, not all particles necessarily move at the same velocity. Some even can be identified by their lower speed in a 'time-of-flight' (ToF) measurement. In this case, on-sensor timestamping becomes necessary to compose the complete event later on. Note that for ToF the relative time between measurements is relevant, while in many other time measurements the 'absolute' time has to be determined, related to the global timescale of the experiment or the accelerator. Some of the work on timing for LHC experiments will be treated in Section 6.13.

In the evolution of nuclear and particle physics experiments and the corresponding electronics, there has been a continuous increase in the rate of interactions. Then the precision in the timing also needs to be improved. With photographic methods a few interactions per day or

[3] Staff from Philips USA participated in this 1960 Asheville Conference, where this silicon tracker was proposed by Bromley and Friedland. It may well be that their idea was at the basis of the 1965 BOL array in Amsterdam. Leo Koerts developed this initiative when ~1961 he was in New York for some time (private communication Koerts).

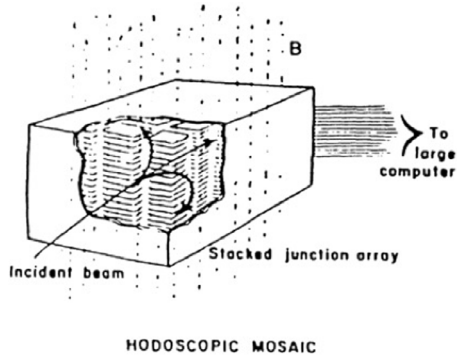


Fig. 5. Schematic proposal for Si tracker in 1960. Electronics was naively simplified (illustration 49 in Ref [22]).

per minute were recorded. Today, up to 40 million bunch crossings per second are recorded, in continuous operation, with each 'frame' containing already many tens of proton–proton interactions. And to be increased to ∼200 after the LHC high-intensity upgrades. This increase in rate is dictated by the much lower probability of occurrence of those interactions that one wishes to study. However, rates are limited by the instrumental capabilities of the sensor elements, the speed and recovery time of signal processing circuits, and the allowed volume of data transmission towards the off-line data storage. Related to rate and readout capacity is the insertion of buffer memory at one or several levels in the readout chain. The silicon IC technology offers various types of on-chip analog or binary storage.

Future upgrades in the LHC experiments aim mostly at higher event rates and have to deal with increased particle densities. This may be handled with faster electronics and by further segmentation of the detection area in smaller cells, operating in parallel. Note that serialized readout, e.g. with a lumped-element delay line, e.g. L-C, can only be used if the segmentation aims at improved position information, without any increased density or rate. Early position sensitive Si detectors for nuclear physics were usually designed this way [24]. Even now, reduction in 'channel count' is sometimes seen as an advantage, but with the typical capabilities of present Si CMOS technology, there is hardly a reason anymore to save on transistors or silicon in a large system. An example that will be mentioned in chapter 8, shows commercial imaging devices equipped with complete ADC for each pixel, and with many parallel digital outputs. To achieve increased rates and separate events within the 1.2 ns bunch crossing time, it would be desirable to attach subnanosecond timestamping to the measured data for all particles. A brief treatment of timing will follow in Section 6.13, but it is beyond this article to discuss details of these circuit developments for future experiments.

With imaging detectors that integrate over a certain exposure time and produce 'frames', there may arise problems with overlapping clusters created by successively incoming particles. Also this problem can be remedied with timestamping for each pixel in the cluster, when the particle comes in. Depending on the rates, this may again require (sub)nanosecond timestamps.

A triggering procedure is needed for the selection of the small proportion of useful events from between all those, which originally have been stored temporarily in local, relatively large on-chip memory, e.g. consisting of 128 consecutive words/timebins, at 40 MHz corresponding to a period of 3.2 μs. The depth of this local memory at least has to be compatible with the time needed for selection of potentially interesting interactions, the so-called L1, the first level of triggering. This decision making is still located in a distant electronics room, so that the 'trigger-latency-time' includes back-forth transmission over some tens of m. In recent experiments, the proportion of rare, 'interesting' events may even be as low as one in 10^9. It is beyond this text to enter in more detail, but it should be obvious that complex processing electronics is needed for obtaining useful triggers. In future, maybe some of the selection functions could be integrated with the circuits on the detectors themselves. An alternative approach has recently been implemented in the LHCb experiment, where the first level trigger architecture is altogether eliminated, and all measurement data are immediately transmitted to off-detector processors.

Most relevant in practice are the size and the power consumption of the ICs which incorporate mixed signal and digital processors, because they must be placed close to, or even directly on the sensing elements. The ongoing miniaturization of circuits has enabled ever smaller, ever more economic and therefore ever more numerous electronic processing units. Admittedly, nothing yet is coming close to the visualization of tracks offered by photographic emulsions, where the microscopic grains are independent sensing points, and not even needing in-situ power at all.

Finally, besides detection efficiency, noise, timing, rate capability, memory and logic, the power dissipation, the power supply modalities and the matched cooling are also key components in the overall system design. Cabling and cooling may represent a large fraction of the cost as well. Faster speed and more data need more power and more cooling, but an excess of hardware degrades the quality of the measurements. In consumer electronics, the drive for ever more advanced CMOS is justified by potential for increase in data volume and reduction in power dissipation. Unfortunately, in HEP the iteration time is decades rather than years. For the experiments, many trade-offs have to be made, which obviously include material cost and workload.

4. The age of standardized electronics modules

For several decades, the nuclear physics community provided a major effort in development of electronics for scientific instruments. Teams of physicists and engineers designed and built innovative instrumentation for the experiments at hand. The definitions for standard 'Nuclear Instrumentation Modules' NIM were issued in 1968 by the US Atomic Energy Commission (AEC-NIM), and were updated regularly by a committee with international participation, chaired by Louis Costrell at the USA National Bureau of Standards NBS (later NIST) [25]. At CERN already in the early years, a series of fast, NIM compatible linear and logic modules were developed and this project was presented by Henk Verweij at the 1968 'Colloque International' in Versailles [26]. A contemporary NIM crate with modules is illustrated in Fig. 6. Crates and modules were commercially produced by various European suppliers, such as SEN and in later years CAEN or Wiener, as well as by USA companies such as ORTEC, Canberra or Tennelec[4]. Progressively a wide range of signal processing and measuring instruments was introduced. However, the NIM instruments remained relatively bulky[5], they offered few or only a single processing channel and lacked an architecture for data transmission.

In elementary particle physics experiments, many more sensor elements were needed, compared to nuclear measurements, because of the much larger number of simultaneously produced secondaries. In order to deal with this aspect, the European Standards on Nuclear Electronics (ESONE) Committee defined in 1969–1971 the Computer-Aided Measurement And Control (CAMAC) standard [27], which enabled computer control of the functions via a bus architecture. The CAMAC standard was then also adopted by the IEEE and soon CAMAC crates and modules with their master computers filled the experiment control rooms, such as in Figs. 7a–b, with hundreds of cables running to the measuring instruments(see Fig. 1).

[4] Only a few companies are mentioned as examples, and no preferences are intended by omitting several others.

[5] As mentioned by Verweij [26], more compact modules were obtained when CERN with a Swiss company introduced the miniature 'Lemo©' connector, much smaller than the usual BNC. But look today at an iPhone© connector....

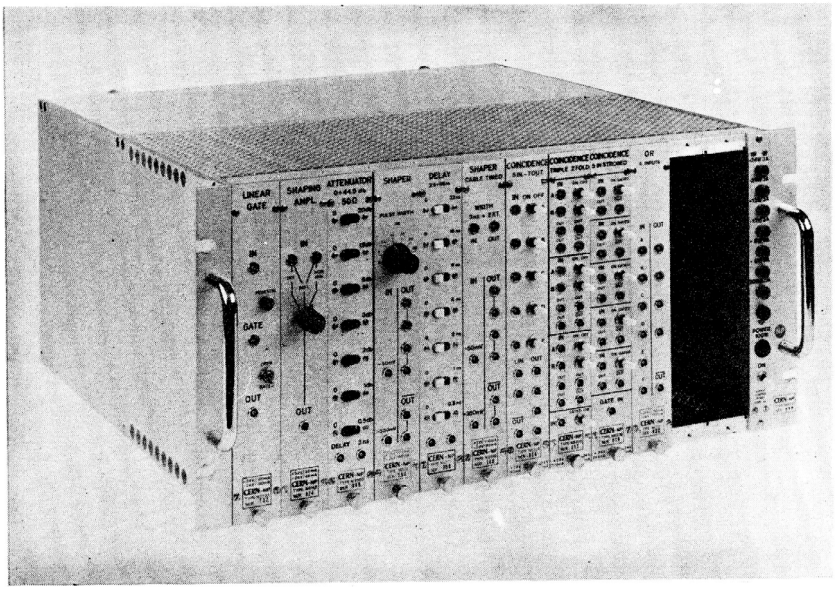
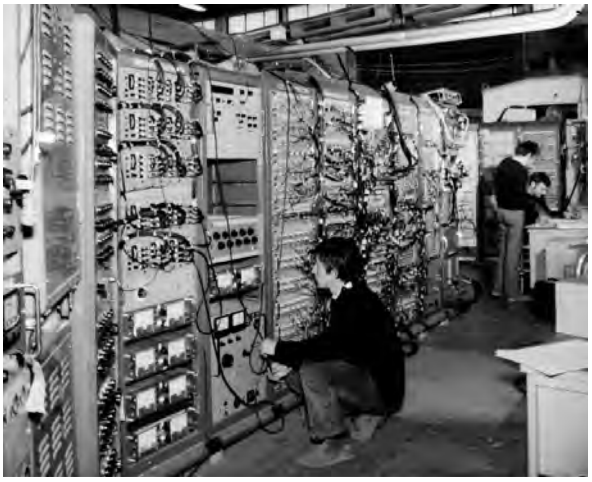
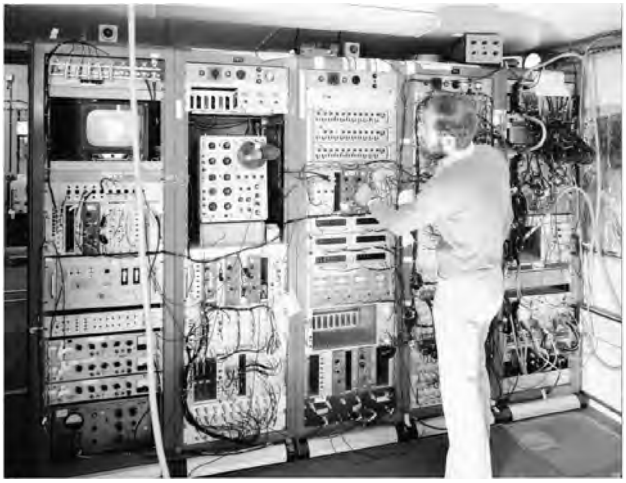


Fig. 6. NIM crate filled with modules, most of which were developed at CERN and then manufactured by European industrial partners (photo CERN, from ref [26]).



7a) Daniel Treille ~1970 in 5 GeV antiproton scattering experiment S91 (photo CERN)



7b) Wilfried Flegel 1975 in the g-2 experiment. (photo CERN 75-6-99)

Fig. 7. Views of typical experiment control rooms at CERN. Racks filled with modules.

Having worked for some time as electronics engineer at the cyclotron at Columbia University, Walter LeCroy became one of the main innovators in CAMAC modular electronics, with his instrument company based in New York (1964) and later also Geneva (1972). After ~1995 LeCroy abandoned production of these modules for physics, but other companies (CAEN, Wiener,..) continue to supply a wide variety until today.

The electronics signal processing module development in 1965–1980 went hand-in-hand with the then just invented multi-wire proportional chambers MWPC coming to the scene [28]. With a range of standard modules, the 'electronic' experiments could run a large number of parallel sense wires, so as to become a serious competition for the bubble chambers. The kHz rate of interactions that could be recorded electronically, was a prime argument in their favor, where the bubble chamber repetition rate usually was ~1 Hz. In an effort to improve this rate, a 'Rapid-Cycle' bubble chamber could reach ~30 Hz but this proved not sufficient for the relatively low probability of interesting events with charm or beauty signatures. Only nuclear emulsions survived for photographic particle recording in some special circumstances, because of their still unchallenged sub-micron precision. In order to pin-point quickly the interesting interactions, however, the emulsion stacks were surrounded by electronic detectors [29], which now are most often silicon microstrip or pixel detectors.

For the collider experiments in the 80's and 90's the NIM and CAMAC modules were hardly useful anymore, because of the strongly increased number of sensing elements, with much more data coming out. FASTBUS was developed as a new standard for processing of such large data volumes, in a collaboration between the NIM and ESONE committees and IEEE. The logic operations used 32-bit words and 'Emitter Coupled Logic' ECL integrated circuits, which had the highest speed at the time. The board size, as well as crate dimensions were chosen to be large as well, so that many circuits could be accommodated, as illustrated in Fig. 8. However, the high power dissipation and the difficulty of handling such large units, turned out to make the FASTBUS standard of little interest for users beyond HEP. Soon the industry adopted the VME standard, which originated from Motorola, using 32-bit and later also 64-bit data. Specific modules for HEP became available as well. In the period 1985–2000 FASTBUS, sometimes combined with VME,

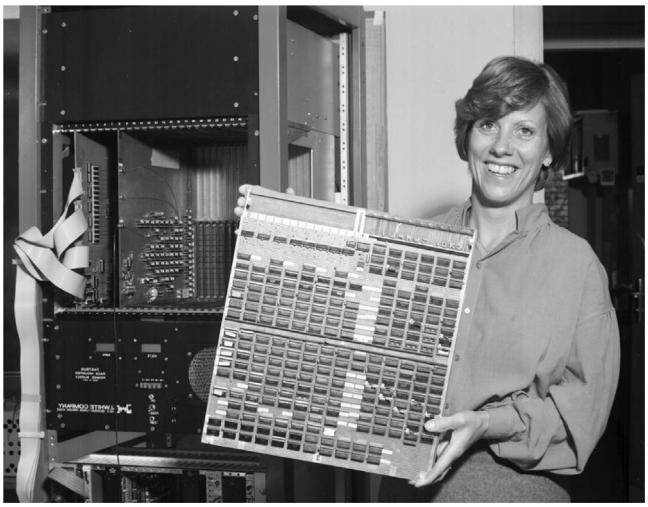


Fig. 8. Technician showing the FASTBUS module on which she did the 'wire-wrap' cabling (photo CERN 83-10-253).

was widely used in the experiments around the world. At CERN in the p-pbar experiments UA1 and UA2, then in the LEP experiments; at SLAC in SLD and PEP; at Fermilab in CDF and D0, and at DESY in the HERA electron–proton collider experiments ZEUS and H1. All these experiments installed large electronics systems for the readout and processing of their multiple detector sub-systems. Verweij sketched the status around 1990 [30] and used as a typical example the block-diagram in Fig. 9, which shows the components in the ALEPH data processing at LEP. Note the large number of FASTBUS crates for the Time Projection Chamber TPC. More about TPC in Section 6.4.

The use of standard modules in particle physics was reduced from ~1995 onward. On-detector electronics progressively became more sophisticated by the introduction of ASICs, and the off-detector processing used electronics with increasingly sophisticated Field-Programmable Gate Arrays (FPG(a). Much of this electronics was experiment-specific, and designed in the participating institutes, and some examples will be described in Section 6.9. Modular power supplies remained one of the important exceptions. The evolution of standards and the committees with scientific and commercial representatives, who played an important role, has been briefly documented in 2000 by Ray Larsen in a SLAC publication [31]. He also discussed the growing use of ASICs, where for the HEP applications no specific standardization has been introduced. However, in the next chapter it is explained that for the IC manufacturing community a wide range of standards is developed, in order that materials and equipment can be supplied by many different industries.

5. Manufacturing of ICs

Describing IC manufacturing in detail would fill several books. A few critical aspects will be mentioned here, in order to help in understanding the IC introduction and evolution in particle physics, and especially provide a basis for the later discussions of radiation effects in ICs. Complete treatments of physics and technology are found e.g. in handbooks by Andrew Grove at Intel [32] or Simon Sze at Bell Labs [33].

Silicon can be grown at a high temperature as a pure single crystal, nowadays with large dimensions, and in that form it is an excellent semiconductor. The long rod, most often with a diameter of 30 cm or sometimes still 20 cm, is sliced in <0.8 mm thin wafers, which are polished with flatness at μm level. In the crystal, the outer valence electrons, four from each atom, behave as a quantized collective in an energy band structure, with a gap of 1.12 eV between the valence

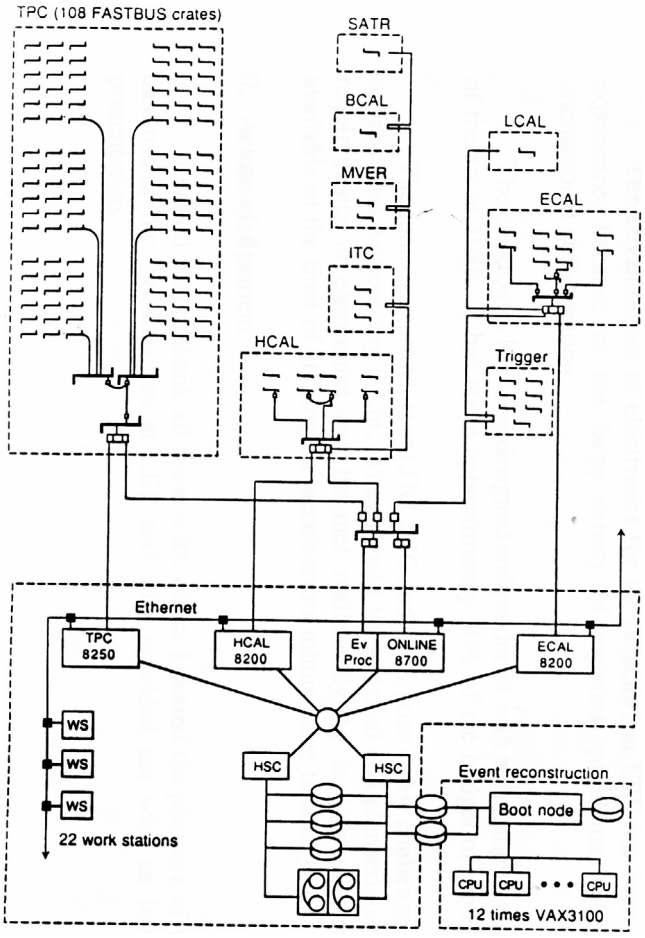


Fig. 9. Schematic view of the ALEPH signal processing electronics system (illustration Ref [30]).

band and the conduction band. The electrons occupy exclusive energy positions, and a fraction of them can be excited from the valence into the conduction band, and then move freely around. This depends on the available excitation energy, and first of all on the temperature. Energy can also be provided by illumination, if the photon energy exceeds that of the 1.12 eV bandgap, or by ionizing particles. Moreover, the conductivity can be adapted by introduction ('doping') of a small concentration of 'impurity' atoms. These are called 'donors', often phosphorous atoms, if they supply an extra free electron, leading to n-type Si, or 'acceptors' if they bind an electron and make a free-moving positive 'hole': p-type Si, usually with boron doping. Depending on concentration, the range goes from nearly isolating to highly conductive. Note that the ionization energy for a free Si atom is much higher at 8.15 eV, but still lower than that of a noble gas such as Ar with 15.76 eV.

Devices are created generally on one side of a Si wafer, by changing locally the electrical characteristics in p- or n-type. Oppositely charged volumes close to each other, a p–n junction, have a 'depletion' zone in between, with a high resistance, where nearly no free charges remain and which can act as a rectifying diode. Fully isolating material can be obtained by oxidizing the Si into SiO_2. Such a thin surface layer of amorphous quartz, called 'field oxide', is created all over a wafer as the first step in the manufacturing of ICs. The purity of this oxide is essential for reliable device operation. Then with lithography, patterns are projected on the oxide surface, holes are etched, and donor or acceptor atoms can be introduced at specific places in the Si crystal,

either by gaseous diffusion or by implantation of accelerated ions.[6] The implantation of energetic ions creates damage in the crystal, and a high temperature 'annealing' (often >1000 °C) is needed to restore the crystal structure and move the doping atoms into substitutional positions in the lattice, so as to create their proper electrical function.

Transistors are conducting or switching devices with a control mechanism to regulate the current, from 'off' state to high current conduction. They can be used for linear signal processing, including amplification, filtering and discrimination in a comparator, or to construct logic processors, etc. In the early years, 'bipolar' 3-terminal diffused transistors were used, with current 'emitter' and 'collector' embedded by diffusion in a 'base'. In the later Metal–Oxide–Semiconductor (MOS) technology, current-control was achieved by varying the voltage on an electrode of conducting material, called 'gate', positioned on a thin insulating oxide under which the current flows: the MOS Field Effect Transistor (MOSFET). Here emitter and collector have been named 'source' and 'drain'. The MOS structure is easier to manufacture, and easier to scale to smaller dimensions. Besides as a purely 3-terminal transistor, it also can be organized as a 4-terminal device with a separate substrate contact. However, in many ICs the substrate contacts are employed for special purposes, such as reducing cross-talk or improving radiation hardness.

The development of the silicon oxide technology took many years, because the thin SiO_2 sheet is very sensitive to impurities and 'pinhole' short-circuits. The MOS transistors and ICs need overall ultra-clean oxidation and processing, which requires clean-rooms and hyperpure materials, especially ultra-clean, de-ionized water. In HEP experiments, the Si devices can be disturbed by ionizing radiation which can introduce defects, that act similarly to impurities in the crystal or at the interfaces (Section 6.12).

Many transistors can be placed together on a single chip of Si, to work as a complete electrical circuit. However, separations between the transistors are essential to reliably operate the ICs. For many years partitioning was achieved with the LOCal Oxidation of Si (LOCOS) process, invented in 1966 by Else Kooi at Philips in Eindhoven [34]. Where LOCOS already allowed close placement of the devices, a further improvement in density was introduced ~1994 with Shallow Trench Isolation STI [35] for CMOS technologies at the 0.25 μm node and below. These isolations are very sensitive to irradiation and special precautions are discussed by Faccio in this issue, and briefly mentioned in Section 6.12.

Ever since the first monolithic circuits were invented, in 1958, the number of transistors in the circuit, on a single Si chip, kept increasing, thanks to decreasing dimensions of transistors, metal connection lines and isolation distance. Gordon Moore published in 1965 his visionary article "Cramming more components onto integrated circuits" [36], where he outlined this evolution towards ever smaller dimensions, and which would become the 'law' for industrial development, now during more than fifty years. Fig. 10 illustrates the continued reduction ('scaling') of the technology dimensions, over the last 15 years, with some examples of corresponding commercial circuits. With shorter length under the gate, MOS transistors also can switch faster, and the logic circuits can operate at higher frequency, even at lower power consumption. Although the velocity of electrons in a GaAs crystal is higher than in Si, circuit speed in GaAs logic nearly all the time was overtaken by that in Si, thanks to this scaling trend.

Scaling was possible also, because the wavelength of the light used for the most critical lithographic steps has evolved over the years, from the 0.436 μm blue mercury line, via 0.365 μm Ultra Violet light and various sources in deep-UV, with 0.193 μm as the latest, and now recently to Extreme UV EUV at 0.0135 μm. The light is projected through a mask, covering just the area of a single chip, which can be sub-mm to ~35 mm on a side. Then the wafer is moved to the position of the adjacent chip, and so on, until the whole matrix of identical chips on the wafer, now mostly with 300 mm diameter, has been illuminated. Using special mask-sets, it is also possible to 'stitch' patterns together and obtain very large Si-area circuits. Such 'wafer steppers' are an essential tool, besides furnaces for oxidation or annealing, ion implanters and cleaning equipment. This equipment has become very expensive, because of the need for nanometer precision over the full 300 mm wafer and ultimate cleanliness. The need for a clean environment also has strongly discouraged human interventions in the processing. Wafers are kept in air-tight boxes between all equipment loading stations. An EUV wafer stepper may cost in excess of 150 M€, and for a production line several of these are needed, apart from the additional steppers using longer wavelength, for the less critical layers on the chips.

Talking about layers: stacking of multiple layers for metal connection lines, or of layers with memory circuits in a USB stick, became possible after the invention of Chemical Mechanical Polishing CMP. The full wafer, with all its irregularities in height after etching and metallization, is covered with an oxide layer. Then a special polishing machine grinds the surface until again a perfectly flat surface is obtained, using a moving soft pad and hyperfine abrasive. Then a new layer with lithography and metallization can be applied with high precision. This CMP process has enabled the reliable connectivity by metal lines in many superimposed levels and the inter-layer connections ('vias'). All the newly invented equipment made continued miniaturization possible, with features now well below 10 nm, and wth reproducibility over the full wafer area.

Figs. 11a, b and c illustrate progress over 30 years, from a single MOS transistor with 2 μm gate length, to a stack of metal layers on top of the bottom layer with many transistors, in 65 nm CMOS, and a FinFET transistor in 10 nm technology. Transistors went through consecutive improvements, from node to node. The gate material, which at first was usually Al, was later replaced by heavily doped polycristalline Si. In recent technology nodes, again metals are employed, and the tendency now is to wrap the gate around the conducting channel, as much as possible. This has resulted in transistors with a triangular shape, called FinFET. Also tubular devices have already been developed, where the gate is all-around the channel. Physical simulation programs are used intensively, for understanding and optimizing the devices, as well as to evaluate the many details in the manufacturing process of these complex ICs. Simulation sofware for the device physics is complemented by simulation tools for the circuit design, see Section 6.7.

For two decades design, manufacturing and commercialization of ICs remained bundled together within industrial entities and some research facilities. Companies such as General Electric, IBM, Siemens or Philips even would make their own processing equipment and their own silicon monocrystals, until after 1970 standardization was introduced by the SEMI collaboration in the USA. A large variety of standards for materials and equipment then allowed independent commercial supply of Si crystals and wafers, which later could also be delivered with high-precision polished surfaces. While at first the imperial units 0.5", 1" and 2" were used, from wafer size 75 mm onwards the industry has adopted metric units exclusively. Most equipment now is designed for the currently predominant wafer size of 300 mm, while some mature technologies are still available on 200 mm. Moreover, manufacturing has become mostly automatized, with practically no manual human interventions anymore in the process. Processes consist of many hundreds of successive steps, with automatic wafer transfers in fully controlled, dust-free environments (see Fig. 11).

A technological and organizational breakthrough, sometimes dubbed 'revolution', took place in the early 1980's, which will be further described in the next chapter, Section 6.7, when the IC manufacturing became progressively de-coupled from the IC design. Independent design houses or teams in universities could develop innovative circuits,

[6] After electron acceleration in television, oscilloscopes and X-ray generators, the accelerators for ion implantation in semiconductors are probably the most important technical spin-off from nuclear and particle physics accelerator developments.

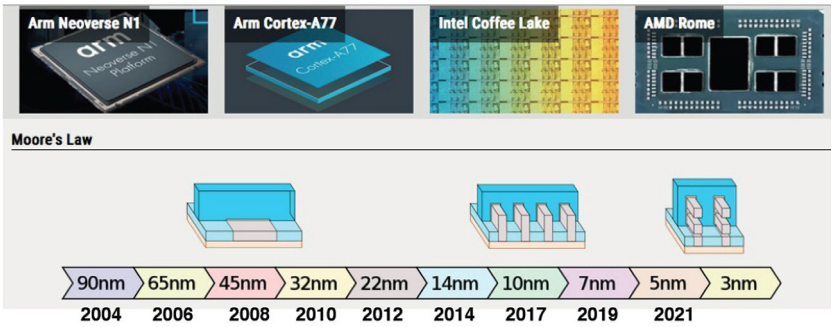
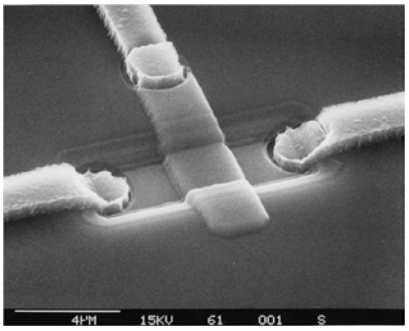
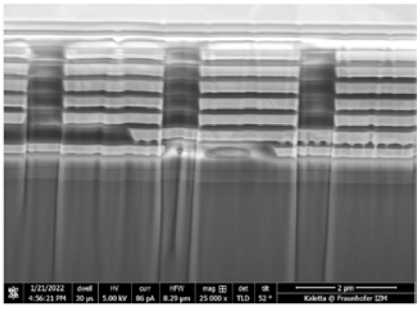


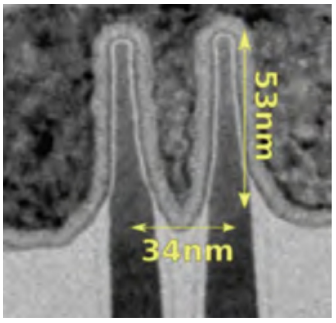
Fig. 10. Successive generations of CMOS technology, described as Moore's Law. Illustration https://en.wikichip.org/wiki/WikiChip accessed April 10, 2022.



11a) MOS transistor in a 2µm technology, ~1982. The gate is the metal strip across the channel, where current can flow from the source to the drain contacts.



11b) cross-section of part of the multi-layer structure of a chip made in 65nm CMOS technology ~2020
(photo Fraunhofer IZM)



11c) FinFET transistors in a 10nm technology. The 'width' of the gate is increased by stretching the channel upward along the fin. The current flows perpendicular to the plane, under the approximately triangular gate, but not along the bottom part.
(photo website Intel)

Fig. 11. Micro-photos of silicon devices.

and have these produced by dedicated foundries, who themselves would have limited or no design activities. Such foundries concentrate on development of perfect manufacturing, but in continuous interactions with both low- and high-volume customers.

6. Step-by-step towards ASICs: Planning or serendipity

Other contributions in this special issue will describe in more detail the design and applications of state-of-the-art integrated electronics for LHC particle physics experiments. In this chapter, a few of the early and historically interesting silicon chip developments for instrumentation will be mentioned. In some cases, as with the TPC in Section 6.4, an important part of the experiment was planned on the basis of a new electronics development. More often, the electronics was not predominant in the planning of the experiment, was more of an afterthought and had to satisfy functions and performance, already defined in prior decisions on the overall concept. Sometimes, a new detector system with integrated electronics was introduced later on as a retro-fit, following an unexpected technical development during, or even well after the construction, such as in UA2, L3 or in CDF (Section 6.8).

Over the years, integrated electronics in the experiments has evolved steadily towards more sophisticated processing, higher speed, lower noise and lower power per sensing element. Often by serendipitous discoveries and through personal encounters, rather than by planned innovation.

This overview begins around 1973, when already a wide range of commercial integrated circuits were on the market for some years. Such ICs were used in the CAMAC standard modules or home-designed equipment, already mentioned in chapter 4.

6.1. FILAS, first ASIC for detectors

Following the introduction of the Multi Wire Proportional Chamber MWPC [28], which usually features thousands of signal wires, a monolithic integrated circuit for the signal processing seemed to become interesting. In 1973 a French collaboration involving the CEA-Saclay Laboratory near Paris and the electronics development laboratory CEA-LETI in Grenoble used their pMOS technology to produce an 8-channel monolithic readout circuit, which they named FILAS. Characteristics were first published at the IEEE International Solid State Circuits Conference ISSCC in 1974 [37]. This was the earliest IC, specifically designed for a particle physics instrument. A number of wire chambers for CERN experiment WA5 were equipped with this circuit. Test results were reported in a letter to Nucl. Instr. Meth. by Bareyre et al. [38], and were also presented at the 1975 IEEE Nuclear Science Symposium [39]. However, the majority of wire chambers continued to be read out via small circuit boards or thick-film hybrids with discrete components. Few teams had access to IC technology, which at that time was concentrated within industrial facilities or governmental research laboratories. Also, pMOS technology is limited in speed and has high power consumption, compared to the later nMOS and CMOS.

6.2. Silicon steers neutrino beams

From ~1972 onward, in the CERN Track Chamber TC Division development work on silicon devices was initiated, in view of the Neutrino Flux Measurement NFM system, for steering and monitoring the new neutrino beams for the SPS West Area. There the BEBC and GGM bubble chambers would operate, in line with the WA1 electronic detector neutrino experiment, led by Jack Steinberger. It is relevant to mention this installation, because it created several contacts between CERN and the silicon world. And this, just at the time that silicon started to dominate electronics. Moreover, experience with this system generated ideas for microscopic particle detectors, with segmentation and fast signals, which could deal with extreme intensities.

Neutrinos in the GeV energy range are produced, each one together with a muon, in the decay of pions and kaons, which come out from a target, when hit with the pulsed, full-intensity, primary GeV proton beam from the accelerator. These pions are focussed with a special, pulsed magnet and allowed to decay, for which a long, evacuated tunnel is required so that no nuclear interactions can occur. Then the muons accompanying the neutrinos, have to be taken away in a 120 m long iron shield, because energetic muons, which do not have strong nuclear interactions, are difficult to stop. Neutrinos interact with even much lower probability, and at most one out of 10^{13} then would show up in the bubble chamber or in the massive electronic experiments downstream.

The NFM system consisted of arrays, each up to 49 silicon diode particle detectors, which were placed in 6 gaps, left open in the muon shielding. The primary proton beam then could be directed optimally onto the target, by looking at the circular symmetry of the muon flux in all gaps, so that the invisible neutrinos were correctly aimed at the center of the experiments, nearly 1 km downstream. Giorgio Cavallari [40], in the beam group of Pierre Lazeyras, supervised the system design and the data acquisition. Electronics engineer Pierre Jarron designed the signal processing, and the author, semiconductor physicist, took care of the silicon sensors, calibration and data analysis. The NFM has been in operation from December 1976 to September 1998, and besides steering the beam, it provided the measurements from which the energy spectrum of the neutrinos could be calculated.

The neutrino and muon flux would come every SPS cycle in a single 'fast-extraction' pulse of 21 μs, or as a 'resonant extraction' during 2 ms. The intensities to be measured varied radially and longitudinally in the shield, from 10^8 down to 100 per cm ^{2}, in these short pulses. This flux of up to 10^{11} $cm^{-2}s^{-1}$ then was measured by integrating the current generated in the Si diode during the pulse, while subtracting the dark current, measured in between pulses. Diodes had different dimensions, so as to allow the large dynamic range to result in output signals between 0.1 V and 10 V.

It was a fastidious amount of work to establish the actual muon flux for each of the >200 diodes from the measured voltage signals. Calibration was based on microscope counting of tracks in emulsions, which were exposed on top of the Si diodes for only one or two SPS pulses. It was found that ~20% of the signal was not from muons but from accompanying (delt(a) electrons. More details about the NFM and the calibration are described in [41]. It was clearly desirable to have an electronic counting device, with well-defined area and sensitivity, and which also could distinguish electrons from muons. With the muons so densely packed in time and space, no electronics could be fast enough for any existing detector, not even the smallest possible scintillators. The only approach might be to develop microscopically small semiconductor detectors, necessarily with a well-defined surface area, and no edge-effects. Back in 1978, fast particle counting, if possible with recognition of the particle type, became for the author a dream, nearly an obsession. The idea for segmentation in microscopic, linear, adjacent diodes was a first step. Two-dimensionality with a pixelated matrix followed in 1988. Each time it was the electronics development which was the key to progress. It took until the Timepix3 detector in 2013, to see a device coming into existence with the capabilities which were desired in 1978. This fulfillment finally came 15 years after the West Area neutrino beams at CERN had stopped operating.

6.3. The 70's: What else with silicon?

In the earlier silicon detector system for neutrino monitoring at the PS, similar to the NFM at the SPS, already in 1974 it was found that the diodes degraded quite quickly under the irradiation. This may have been the first observation in an elementary particle physics experiment of radiation damage in silicon. The increasing reverse diode current added to the signal current, and precise compensation would be needed. Various radiation damage studies were initiated. In collaboration with the institute PHASE at the Nuclear Research Center Strasbourg, Thermally Stimulated Current TSC measurements were made on separate Si samples, after exposure in the muon flux, in neutron radiation or in a cobalt gamma source. Double-vacancy and phosphor-vacancy crystal defects were found, but also a high proportion of neutron-induced, extended clusters [see Ref. [41], chapter 5, and further references therein]. Precautions were taken to mitigate radiation effects in the new NFM system at the SPS. Although radiation damage also occurred there, it was much less than expected. In the muon shield, behind the pion-decay tunnel, far from the primary proton target, the neutron flux was negligible, compared to what it had been in the PS neutrino layout, and it could be concluded that neutrons were primarily responsible for the damage in the Si volume .

Another specific problem occurred in diodes used earlier at the PS, because of the short, dense bunches. After the CERN booster came in operation ~1974, the beam intensity was increased to well beyond 10^{12} protons, distributed over maximum 20 bunches of 10 ns in the 2.3 μs beam pulse. Then, above a certain ionization density in the Si diode muon detectors, depending on their position, signals were not anymore proportional but increasing exponentially, by some unknown multiplication mechanism [42]. The then most famous scientist for studying charge multiplication in silicon was prof Roger Van Overstraeten [43]. He had returned from Silicon Valley, and was working at the ESAT laboratory of the Leuven University in Belgium. The author went to visit him in 1976. This was the first contact, which later developed into a fruitful collaboration of CERN and the particle physics community at large, with ESAT and IMEC. In fact, Van Overstraeten founded IMEC at the end of 1983, in the framework of a Flemish microelectronics industrialization project, supported by the first, newly established Flemish government under Gaston Geens and Marc Eyskens. This project included also the foundry MIETEC and the educational organization INVOMEC, which provided foundry access, CAD tools and support. Somewhat later, Eurochip and Europractice, to be mentioned in Section 6.7, were also supported by staff of INVOMEC in Leuven. Today, IMEC has grown to be the world's largest non-profit R&D center on semiconductors and applications, with ~4000 collaborators and budget >600 M€.

Among the other actions and contacts which helped the embryonic silicon activity at CERN, was attendance at the very first European SEMICON trade fair for silicon processing equipment, in 1975 in Zurich [44]. The introductory speech there was given by Gordon Moore [36], in which he mentioned that chips in the future might unrecognizably look like the grains of sand, from which the silicon itself had been produced. At the EPFL in Lausanne, Pierre Jarron and the author participated in the 'Journées Electroniques' on "Limits in Miniaturization 1980". There, some doubts were expressed, that technology could really go below 1 μm, because of the wavelength of the light needed for lithography. But generally there was optimism, and we had a first encounter with prof. Eric Vittoz from the EPFL. More contacts with the silicon world came from participation in the 1977 and the 1979 IEEE Nuclear Science Symposia, in San Francisco. The author consulted in 1979 several scientists in SLAC and Berkeley, about the prospects for silicon devices and integrated circuits. In particular, Fred Goulding, head of LBL electrical engineering, encouraged this work towards a silicon microstrip detector. Again by chance, also Paul Burger from Enertec-Schlumberger, who had supplied some of the muon detectors for the NFM system, was at this NSS, and plans were made for making

a prototype microstrip detector. Initially we would follow the 'surface barrier diode' process, already used for the Amsterdam checker board detector [18]. Equipment for oxidation and ion-implantation was not yet available, but would arrive soon afterwards. At the same time, we brainstormed about monolithic integrated circuits which would directly record and identify passing particles.

In the late seventies, precise energy deposition measurements in silicon were made, in order to better understand the particle detection and to compare these with the Bethe–Bloch and Landau theoretical descriptions. Si diodes of different thicknesses were exposed, also when embedded in absorbers, in pion and muon beams at CERN. Delta electron contamination in the absorbers could be determined [41, chapter 3]. Similar work, but with emphasis on particle channeling, was done at that time by the team of Erik Uggerhøj from Aarhus University, and collaborators [45].

6.4. CCD shift register as time encoder for TPC with 3D track reconstruction

In the USA, the application of a linear Charge Coupled Device CCD for signal recording and timestamping by David Nygren was an early, innovative use of a special integrated circuit in particle physics. In 1978 he invented the gas-filled 'Time Projection Chamber' TPC [46], to be used as the central tracker for the SLAC electron–positron collider experiment PEP4. The electronics design was published in 1981 by Jared et al. from Lawrence Berkeley Laboratory [47]. They used the Fairchild321 A commercial, 2-channel, 455 cell CCD. They could record at 10 MHz up to 20 successive pulses from each wire, during the 15μs maximum drift time of primary ionization electrons through the gas volume. The drift times as recorded by the clocking of the CCD, allowed the 3D reconstruction of the tracks which emerge from the primary interaction vertex.

Gas-filled TPC have become a widely exploited type of 3D particle tracker, which can be used if the intervals between primary interactions are not much shorter than the electron drift times through the gas volume. A typical example was the TPC in the ALEPH experiment at the CERN Large Electron-Positron (LEP) collider, described in the ALEPH overview [48], Section 4.2. They did not use CCD but the signals from each pad or wire were continuously sampled and digitized using a 11.4 MHz Flash ADC and 512 time buckets/bins. With the $\sim 10^5$ sensing elements, the readout system became also large, which can be seen from the number of FASTBUS crates, illustrated in the earlier Fig. 9. The load of data processing in the FASTBUS modules for the ALEPH 'event builder' was alleviated by the introduction of a set of hardware-programmed gate-array chips, one of the first logic ASIC design efforts in HEP. A little more about this in Section 6.9.

A decade later, in 2003, the first specific IC for application with TPC was developed: the ALTRO chip [49] in the ALICE heavy ion experiment at the LHC. This chip, preceded by the front-end signal processor 'PASA', contains ADC and sophisticated digital processing for 16 channels in parallel. The first version was designed by Luciano Musa at CERN, and produced in 0.25 μm CMOS by ST Microelectronics. The more recent prototype version SuperALTRO [50] was an early example of the combination in a single chip of the analog front ends with all their subsequent digital signal processing, including ADCs. This chip was for the LHC community also one of the first to apply a 0.13 μm CMOS technology, A final version named 'SAMPA' is now used for the upgrade of the ALICE TPC as well as for other types of gas-filled detectors.

While gas-filled TPC cannot easily be used as tracker in experiments with >MHz event rates, their strong point is the larger number of space points which determine the particle trajectories, in comparison with the now usual silicon vertex/tracker systems. In chapter 8 is described a recent development in ASIC readout for Si pixel detectors, which will enable the TPC approach to be used also in a 1 mm Si layer. In principle, this is compatible with the high rates in LHC.

Living close to the California Silicon Valley, Nygren was quite aware of various possibilities with new microelectronics devices, and he expressed this in a meeting of the International Committee for Future Accelerators ICFA in 1979. Fig. 12 illustrates a statement in this sense, which then strongly motivated following work at CERN.

6.5. 1980, Silicon microstrip detectors call for ICs

Several teams in Europe and the USA ~1979 considered projects to develop detectors which would improve particle tracking precision, such that the 'long-lifetime' beauty/bottom and charm particles could be studied. For the author, detectors with microscopic elements had been a longtime challenge, for reasons of dense flux measurement as explained in 6.2. Now the behavior of charmed particles added interest for such exploratory work. The existing relations with silicon manufacturers helped to speed up the realization of a few prototype microstrip detectors, in early 1980. Pierre Jarron already had been working on amplifier designs for single minimum ionizing particles since 2 years. A system with a 100-strip detector, at a 200 μm pitch and fifty 2-channel readout cards could be installed by May 1980 in CERN test beams. The first test was a collaboration with François Piuz in the CERN South Hall, and another beam test followed, with Bernard Hyams and Robert Klanner of experiment NA11, in their 120 GeV pion beam H6 in the North Area. These first measurements and event reconstructions were published before the end of the year [51]. That article also shows the references to most of the earlier publications, including those on the BOL experiment, for which double-sided Si devices had been made, but with fewer, larger strips. Besides the finer pitch of the diodes, the main innovation with the new microstrip system was the fully parallel signal processing, including off-detector ADC, for each of the 100 individual strips. The earlier BOL electronics determined the x and y position of the strips hit by the particle, using only two signal processors per wafer. These measured the time differences between the time of the interaction, known from the beam hodoscope, and the arrival times of the signals, which traveled along delay lines, both at the front and the rear sides of the sensor. As mentioned earlier, this approach would not be possible anymore with several simultaneous particle impacts per wafer.

The CERN microstrip team was convinced that soon lithography and MOS technology would be available, both for the sensor itself and for readout ICs. But designing such ICs would need a learning curve, which was estimated at a few years. To immediately show results with the new type of detector, a first step therefore was the design of a more compact, 4-channel, thin ceramic hybrid circuit, with discrete components: MSD2 [52]. Figs. 13 and 14 illustrate the basic units and their experimental environment, in the CERN Omega spectrometer. Already in 1981, several experiments at CERN and in the USA commercially acquired Si microstrip detectors and generally made themselves readout cards, similar as they used to do for wire chambers.

Vertex telescopes with several silicon planes needed much more and much smaller electronics. For the planned collider experiments, it appeared absolutely imperative to use silicon VLSI technology. In the years from 1981 several international meetings were dedicated to discussions about the new silicon detectors and their readout electronics: microstrip detectors and also CCD. After a small workshop at CERN and another at Cosener's House in Abingdon, a major meeting was organized in September 1981 by Tom Ferbel at Fermilab [53], complete with proceedings (Fig. 15). He invited several silicon technology specialists as well as scientists from around the world. Ferbel had the foresight to include a discussion on radiation hardness for sensors and electronics. Joseph Killiany was there, and he invited the author to come a few weeks later to his group at the Naval Research Laboratory NRL in Washington. There he introduced Nelson Saks and his work on radiation effects in their CCD imagers [54]. Later on, this contact contributed to a new approach for radiation tolerant ICs in the LHC experiments (see 6.12 and article by Faccio, this issue).

The next meeting with a great impact on the introduction of silicon in particle physics, was the 3rd European Symposium on Semiconductor detectors, November 1983 in Munich [55]. Why the Third and not

ICFA meeting October 1979
(editor U. Amaldi) (convenor D. Nygren)

3.2.3 Semiconductors

The use of solid-state techniques in high energy physics appears to be remarkably under-developed, but the situation could change with

Fig. 12. Copy of lines from 1979 ICFA report.

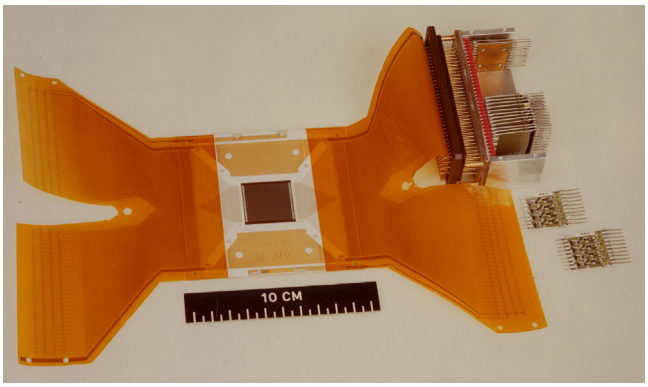
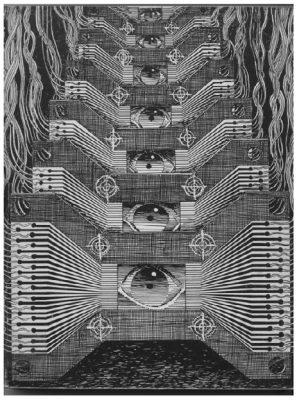


Fig. 13. Microstrip detector and the MSD2 4-channel hybrid readout circuits, providing high density signal processing in a relatively small volume (CERN photo-8310560).



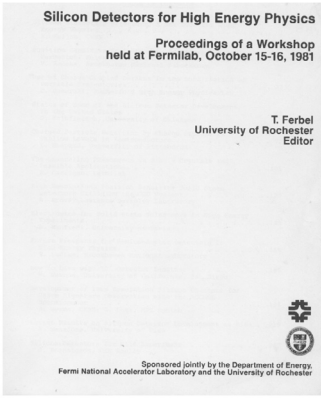


Fig. 15. Proceedings of Fermilab Conference, on microstrip detectors, September 1981. From [53].

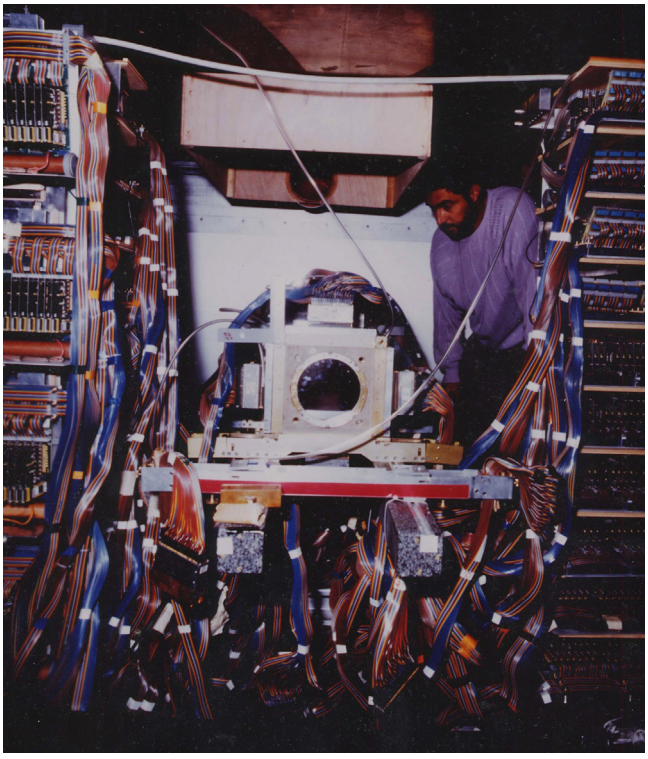


Fig. 14. Leonardo Rossi in the CERN Omega spectrometer, installing the silicon microstrip telescope equipped with the MSD2 readout circuits. The expenses forin the cables alone, equalled those for sensors and electronics. (photo CERN).

First? During earlier visits at the PHASE laboratory in Strasbourg, the author had noticed a copy of stencilled proceedings of the first Symposium on Nuclear Detectors at the Technische Universität München TUM, May 1970, and also of the second, in September 1971, published as Nucl. Instr.Meth. 101 (1972) vol 1. Rather than having another new series of meetings at CERN, it was preferred to resume these nearly forgotten Munich Symposia. A motivation for this choice was the trailblazing work in the NA11 group at the Max Planck Institute, together with Josef Kemmer at the TUM. At this Symposium, Chris Damerell, also working in NA11, presented an overview, with emphasis on their first results obtained with CCDs, directly as particle detectors [56]. Several teams described possible approaches for readout electronics. Most of them emphasized the integration of the front-end signal processing circuit directly on the silicon sensor chip. In hindsight, the more visionary contribution was the proposal for a 128-channel nMOS ASIC by Sherwood Parker, Steve Shapiro and J. Terry Walker from Stanford and SLAC, with Bernard Hyams from CERN [57]. But for years to come, it was not obvious which would be the best way to go.

6.6. *Which way to go? Again CCD, or different directions*

The group of physicists in the CERN NA11 experiment had been considering already in 1979 the use of a CCD matrix of capacitors as a particle tracking detector. CCDs combine in a monolithic device the segmented sensor function, originally for visible light, together with serial readout via a fairly simple output circuit. In 1985 Chris Damerell and his Oxford team had installed two such devices as part of the microstrip telescope [58] and in the same article they proposed a system for the SLAC collider experiment. The long serial readout time could handle only low interaction rates, but it was found that the true 2-dimensional coordinate measurements provided so much more precision and selection capability, that the experiment collected better results, even with much lower beam intensity and fewer interactions. The use of CCDs continued in several experiments over the following decades. This became a niche for tracking and vertex measurements, in parallel with Si microstrip detectors [59]. The excellent results in 2-D particle tracking obtained with the CCDs, triggered later the development of hybrid pixel detectors, so that 2-D also became possible at very

high interaction rates, thanks to their fully parallel signal processing for all sensor elements.

For some time, the CCD also appeared to be attractive as readout circuit for microstrip detectors, and several presentations were given during this 3rd Munich Symposium [55]. With a high clocking frequency and numerous small pixels, a CCD might store the successive analog signals of particle hits, similar to the TPC application mentioned in 6.4, but now working as a parallel–serial converter with event selection capability. The frequency of 66 or 70 MHz announced in early LHC proposals was well in reach for the CCD. This timestamping with associated analog amplitude signal storage, was inspiration for Jarron and the author to propose a project for such a CCD, in collaboration with the Philips group in Nijmegen [60], who had already made a 50MHz device for their 'time-expansion' oscilloscope. In parallel, in 1984 an opportunity arose for the author, to stay for a year-long visit in the CCD group at the electronics laboratory ESAT of the Catholic University Leuven, Belgium. At the time this was one of the famous places for development of CCD. By chance, just then, the Flanders 'Interuniversity Micro Electronics Centre' IMEC had been founded, as mentioned in Section 6.3, so that close contacts between CERN and IMEC were in place from the outset. These contacts soon led to the conviction that CMOS technology would be better suited than CCD, for IC development in particle physics applications.

Still, in the 1983 Munich Symposium different alternatives for silicon detector readout had been proposed, so as to integrate the electronics, or at least the front-end amplifiers, directly onto the high resistivity Si microstrip substrate. Teams with direct or indirect access to silicon processing facilities went in this direction. And this approach has continued to be developed for years. Today, some sensors have integrated transistors, such as the CCD on high resistivity [61,62] or Si drift detectors [63,64]. The integrated front-end transistor circuit helps in achieving a very low noise, recently only a few electrons r.m.s. However, it turns out that high resistivity Si is not quite compatible with CMOS processing in the large, commercial foundries. One of the reasons is that this material is brittle, because it is grown in a 'floating-zone' process, which results in lower oxygen content than in Si crystals grown by the more common Czochralski process. The small concentration of oxygen atoms apparently results in better cohesion and some flexibility of the Si crystal.

It is useful to designate different approaches for producing the silicon sensors and/or their readouts as ASICs. Until ~1975 many nuclear research institutes had adequate equipment, such as a furnace and an evaporator, to make their own Si or Ge detectors, and for readout they also produced their own printed circuit boards, or they bought standard NIM modules, as mentioned in chapter 4. This may be called 'home-made' approach (a). This applied to the FILAS ASIC, for example, where scientists from CEA were the users, and colleagues in CEA the designers and manufacturers. Approach (b) would be different, when the user entity is not itself designing nor manufacturing, but places an order with an electronics company to take care of this, according to user requirements and specifications. In a third approach (c), the user learns 'himself' how to design circuits according to the manufacturer's design rules, and then transfers the design to the industrial manufacturer, usually called 'silicon foundry.' which also has provided the technical parameters for their process. This approach (c) practically represents a 'revolution' because until ~1980 design and manufacturing of ICs were the exclusive domain of commercial suppliers and some well-equipped research institutes. And until then, most ICs were circuits for general use, while ASICs aiming at specific applications, were hardly known of. This 'revolutionary' model is discussed in the following section.

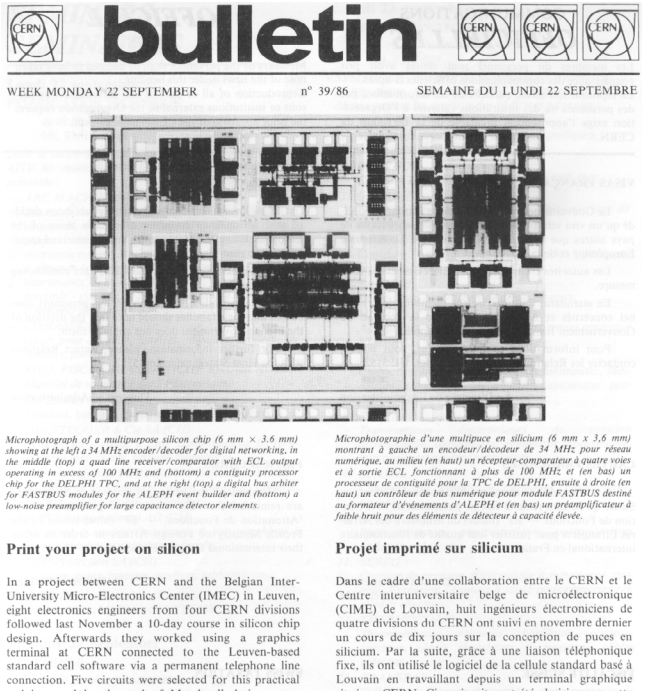
6.7. A revolution answers the call, with multi-project wafers, brokers and a user group in hep

By chance, around the time when the silicon microstrip detector was introduced in particle physics, the landscape in silicon IC design and processing turned around, and a 'silicon revolution' took place. This sometimes is called the 'Mead-Conway revolution'. The most visible turning point was the Design Course by Lynn Conway in 1978 at MIT, on Very Large Scale Integration VLSI. This was followed immediately afterwards by the publication of the textbook by Carver Mead and Lynn Conway [65]. Many universities then started courses and training, and commercial 'design houses' were founded. Several industrial companies responded by opening up their manufacturing facilities to designs submitted by these outsiders, while others still remained closed to the outside, as before.

These changes were to a large extent based on advances in the silicon processing technology, which moved towards the use of metal or polysilicon gates over a very thin oxide, for steering the current: the Metal–Oxide–Semiconductor MOS technology, already described in chapter 5. This MOS technology lends itself to easier design rules than those needed for circuits in bipolar technology. At the same time, the ever smaller-dimension lithography, larger furnaces, chemistry and clean room environment began to imply million-dollar bills, which only the industries with large production volumes could economically afford. By 1980 such a factory would cost in excess of 50 million US$, increasing by tens of millions for each new generation, and today a cutting-edge manufacturing facility may require even 2×10^{10} $. Such a facility has to have a yearly turnover in the 10^{10} $ range, which implies manufacturing of millions of wafers, with billions of chips. The requirement of high overall production volume, eventually made possible an easier access for a large variety of users, also including education and scientific applications. A wider base of customers could be created. Especially the company Taiwan Semiconductor Manufacturing Company TSMC, founded in 1987 by Morris Chang, who came from Texas Instruments, elevated the outside-design principle to a high level. At the start TSMC received for a while significant technical help of Dutch and Swiss specialists of the Philips company.

The access to the open 'silicon foundries' became organized through 'broker-organizations', which facilitated distribution of the foundry-specific design rules. They assembled many designs together in economic 'multi-chip' blocks, to be manufactured as Multi-Project Wafers MPWs. This new modality of chip design was supported for academic and R&D users, e.g. by MOSIS [66] in the USA. In Europe, NORCHIP was one of the first brokers, in 1983 followed by INVOMEC, the educational department of IMEC in Leuven, which soon served customers beyond Flanders. In France Circuits Multi-Projets CMP was started in the French 'silicon valley', near Grenoble. Several other national organizations were active, until the European Commission in 1989 launched the VLSI Design Training Initiative and the associated service organisation "Eurochip" was formed, consisting of five of the major regional players (CMP France, DTU Denmark, GMD Fraunhofer Germany, IMEC Belgium and RAL United Kingdom). This scheme delivered common pan-European brokerage and ASIC design tool services across Europe. Subsequently. the organization was renamed, and continues to operate in the EU R&D Framework Programs as 'Europractice' [67]. Besides the MPW hardware, these brokers provide educational material, access to CAD tools, foundry-specific process parameters, and help-desk facilities, so as to avoid trivial technical questions to be adressed directly to foundries themselves. A number of people made this European initiative into a great success, working at RAL, IMEC, Fraunhofer in Erlangen, Grenoble and Lyngby in Denmark. Without discriminating others, it seems fair to credit John McLean at RAL, who was supervising the activities on the CAD tools, Dr Carl Das with his colleagues at IMEC and Fraunhofer, who organized the MPW, and Prof Bernard Courtois in Grenoble.

These increasingly wide-spread ASIC design activities became quite professional through the availability of device and circuit simulation packages, either developed at universities or commercially. The SPICE program ('Simulation Program with Integrated Circuit Emphasis') [68] was introduced in 1973 by Laurence Nagel and Donald Pederson at Berkeley University, and newer versions are still widely used. In the



bulletin

WEEK MONDAY 22 SEPTEMBER n° 39/86 SEMAINE DU LUNDI 22 SEPTEMBRE

Microphotograph of a multipurpose silicon chip (6 mm × 3.6 mm) showing at the left a 34 MHz encoder/decoder for digital networking, in the middle (top) a quad line receiver/comparator with ECL output operating in excess of 100 MHz and (bottom) a contiguity processor chip for the DELPHI TPC, and at the right (top) a digital bus arbiter for FASTBUS modules for the ALEPH event builder and (bottom) a low-noise preamplifier for large capacitance detector elements.

Microphotographie d'une multipuce en silicium (6 mm x 3,6 mm) montrant à gauche un encodeur/décodeur de 34 MHz pour réseau numérique, au milieu (en haut) un récepteur-comparateur à quatre voies et à sortie ECL fonctionnant à plus de 100 MHz et (en bas) un processeur de contiguité pour la TPC de DELPHI, ensuite à droite (en haut) un contrôleur de bus numérique pour module FASTBUS destiné au formateur d'événements d'ALEPH et (en bas) un préamplificateur à faible bruit pour des éléments de détecteur à capacité élevée.

Print your project on silicon

In a project between CERN and the Belgian Inter-University Micro-Electronics Center (IMEC) in Leuven, eight electronics engineers from four CERN divisions followed last November a 10-day course in silicon chip design. Afterwards they worked using a graphics terminal at CERN connected to the Leuven-based standard cell software via a permanent telephone line connection. Five circuits were selected for this practical

Projet imprimé sur silicium

Dans le cadre d'une collaboration entre le CERN et le Centre interuniversitaire belge de microélectronique (CIME) de Louvain, huit ingénieurs électroniciens de quatre divisions du CERN ont suivi en novembre dernier un cours de dix jours sur la conception de puces en silicium. Par la suite, grâce à une liaison téléphonique fixe, ils ont utilisé le logiciel de la cellule standard basé à Louvain en travaillant depuis un terminal graphique

Fig. 16. Front page of the CERN Weekly Bulletin in September 1986, number 39/86 [70].

Universities in California, a locally developed layout tool 'Magic' [69] has been popular for many years. Through the connection of CERN with IMEC, the Silvar-Lisco programs supported early design work. This was since 1979 one of the first commercial CAD software suppliers, also based in Leuven. It was soon surpassed by Mentor Graphics (founded 1981, since 2017 Siemens-ED(a) and then by Cadence, established in 1988, and which is today market leader, who offers an extensive toolkit for nearly all aspects of the IC design and production sequence, and covering most of the technology nodes in industry. Acces to these tools for academia is organized through Europractice.

After only a few years, this 'Mead-Conway silicon revolution' also led to the widespread introduction of ASICs in particle physics experiments. The first chip design for CERN contained 6 test projects, illustrated in Fig. 16, and was manufactured at MIETEC in Oudenaarde, Belgium, via INVOMEC. Already in 1990, ASICs for CERN in the SACMOS technology of the Swiss Philips branch Faselec, would arrive from TSMC instead from Zurich. For a number of years the ASICs for particle physics were made with several different silicon foundries, or university-related facilities. A few of these will be illustrated later. The Italian-funded LAA detector R&D program [71] supported the early microelectronics work at CERN, until the much wider ranging CERN Detector R&D program was started in 1991. Progressively, until 2000 nearly 50 projects were recommended by the Detector R&D Committee DRDC, in order to develop critical equpment for the planned LHC experiments. The formal approvals allowed support by national agencies and by CERN. Many projects aimed to design combinations of detector and microelectronics, for the various parts of the future detectors, including tracking, calorimetry, signal transmission and processing, etc. Several teams began work on ASIC design, including some in the USA who for a while had been idle by the cancellation of the Supercollider SSC in Texas.

A coordinating role was assumed by the LHC Electronics (Research) Board, LERB, which also initiated Microelectronics User Group meetings, held at CERN several times each year, between 1991 and ~2000. Outside specialists were invited to give seminars on technical aspects of design, manufacturing and radiation effects. Moreover, the LERB also started a series of yearly Workshops on Electronics for LHC Experiments, with the first in Lisbon in September 1995 [72]. Afterwards these were held in Balatonfüred (Hungary), London, Rome, Snowmass Colorado, Kraków, Stockholm, Colmar (France), Amsterdam, Boston, Heidelberg and València (Spain). From 2007 the Workshop was named Topical Workshop on Electronics for Particle Physics TWEPP, starting with TWEPP-07 in Prague [73]. The series is continuing, with the Proceedings published each year soon after the meeting, and available on the CERN website. These form together a rich trove of information, in which hundreds of particular IC designs have been described, often before manufacturing and later with the results.

By the end of 90s the CERN microelectronics team took up a sort of 'pre-broker' function [74], and collected for many HEP users their designs to be submitted, before these would go to a real broker with the foundry contacts, often Europractice and/or IMEC. Thanks to the close contacts which Alessandro Marchioro could create with the IBM company, a majority of designs from particle physics from ~1998 onwards, could be processed in a 0.25 μm CMOS technology in IBM foundries, in France or in the USA. Technical advantages coming from this relationship will be mentioned later, and these are also commented on in the article by Faccio, in this issue [1].

6.8. The first ASICs for MARKII, UA2, CDF and LEP experiments

The ASIC project in Stanford, already mentioned at the end of 6.5, using their 5 μm nMOS technology, advanced between 1983 and the fourth Munich Symposium in 1986 [75], where the team reported first particle measurements [76]. A photograph is shown in Fig. 17, with their chip connected to the 128 diodes of a microstrip detector. In the next year, several teams followed up on the basic design ideas from this Microplex, especially the switched capacitor feedback and the storage capacitors. Such readout chips would become essential in the inner region of the beam collider experiments, such as Delphi in LEP at CERN, and MARKII in SLAC.

In 1987 Stuart Kleinfelder at LBL with colleagues from Fermilab, published [77] a thorough re-design, including sparse readout, which they called SVX. This ASIC was produced via MOSIS in a 3 μm CMOS technology. A chip photograph is shown in Fig. 18. A later iteration SVX2 was evaluated in 1990, and effectively used in the CDF silicon vertex detector [78]. This was an upgrade of the inner tracker, and consisted of a 4-layer silicon microstrip tube, inserted within the existing gas-filled TPC in CDF, the proton–antiproton collider experiment at Fermilab. This upgrade became operational after 1992. The CERN LEP experiment L3, using the SVX-H3, developed another upgrade/retrofit project, with a 2-layer, double-sided silicon microstrip vertex detector [79]. This precision tracking instrument was inserted within their gas-filled Time-Expansion-Chamber, after the diameter of the beam pipe could be reduced. This operated from 1993 until the LEP shutdown in 2000.

J. Stanton at the Rutherford Appleton Lab RAL near Oxford, in the team animated by Paul Seller, elaborated another version of the Microplex [80], intended for the Delphi silicon vertex detector. Also in this case, several iterations were made [81], and by 1990 they showed version MX5 [82]. These ASICs were manufactured by the Belgian foundry MIETEC, supposedly in a 1.5 μm CMOS technology. Then a further MX3/MX6 version was designed in a collaboration with the LAL near Paris [83], by Ardelean, Seller and colleagues. The main reason was to look for better noise performance. They achieved nearly a factor 3 improvement, depending on parameters such as shaping time, detector leakage current and power supply, and they mention a 3 μm CMOS, again at MIETEC. Successive versions were used for the vertex detector and its double-sided upgrade in Delphi [84,85]. Previous circuits for Si microstrip readout often operated with equivalent noise charge ENC in the range 1000–2000 electrons r.m.s. but now they achieved an ENC as low as 800e^-, at ~10 μs shaping time.

The Microplex MX5 was also adopted for the upgrade of the LEP experiment OPAL [86]. They reported a noise performance in-situ of

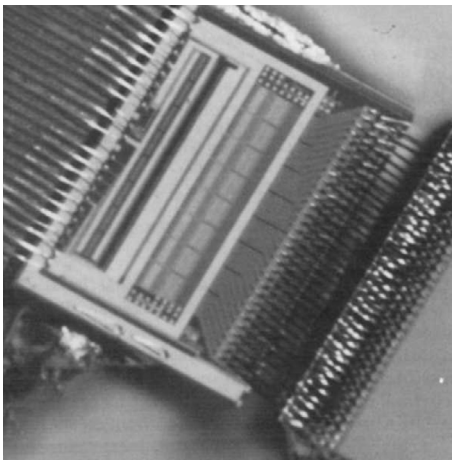


Fig. 17. Photograph of the first mounted Microplex circuit in a test beam, 1986, with wirebonds from the Si microstrip detector on the bottom right, and output top left [76].

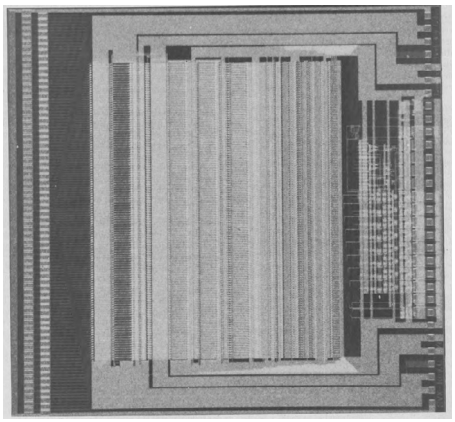


Fig. 18. Microphoto of SVX2 chip, 1987 [77].

1000e⁻ r.m.s. Also here, for the further upgrade with double-sided microstrip detectors the MX ASIC was employed [87].

A German group participating in the ALEPH experiment at LEP, from the Max Planck Institute in Munich, together with the Fraunhofer Institute for Microelectronics, with processing facilities in Duisburg, also took up the design of Si microstrip readout. At first they intended to integrate the front-end in the sensor itself. By 1986 they changed into using their in-house CMOS technology for making a separate ASIC [88]. At the first London Detector Conference in 1987, they published a 128 channel prototype [89], much along the same lines as the Microplex and MX. Franco Manfredi from Pavia University and scientists from the Politecnico Milano joined this group, and helped improve the design by incorporating JFET, which also became available in the Duisburg-Fraunhofer technology. This helped in achieving a noise figure ~600 e⁻ r.m.s. for 10 pF input capacitance of each Si strip. A schematic diagram of part of their design is shown in Fig. 19, where also the 4-fold correlated sampling can be noted [88]. This ASIC with 64 channels, called CAMEX64, or later with the JFETs JAMEX64 [89], was used for the ALEPH vertex detector, which employed 2 layers of double-sided microstrip detectors [90].

In contrast to the switched-capacitor pre-amplifier circuits in the preceding Microplex, MX and CAMEX, Pierre Jarron at CERN implemented a continuous feedback loop in the design of the fourth ASIC, called AMPLEX [91], with an Operational Transconductance Amplifier OTA, as illustrated in Fig. 20. In this way, the classical approach for a charge-sensitive amplifier was used, as in most nuclear physics instruments. The resistive feedback element was a long transistor, which also functioned as a compensating element, adapting the baseline after variations in the leakage current of the detector element at the input. The 16-channel AMPLEX design effort was preceded by an intensive training in 3 μm CMOS IC design, at the INVOMEC training center at IMEC in Leuven, in May 1986. This training included practical design exercises, which resulted in the test chip, already illustrated in Fig. 16 [70], which contained a prototype of the amplifier, used in AMPLEX. The AMPLEX characteristics were then optimized for the 16-element Si pad detectors for UA2, with relatively large capacitance. The noise figure should be low enough to enable the identification of primary single electrons from the interactions. These had to be distinguished from copious secondary electrons, generated at a distance from the origin. The ENC was measured to be 400 e⁻ + 33 e⁻ r.m.s. per pC, and with 20pF detector capacitance [70], well suited to detect the electron signals of ~20 000 e⁻. A chip photo is shown in Fig. 21. These chips were mounted in special, thin ceramic packages, a precaution which was abandoned in all later experiments. They were lodged on top of a very thin, flexible multi-layer ladder. This was bent in U-shape,

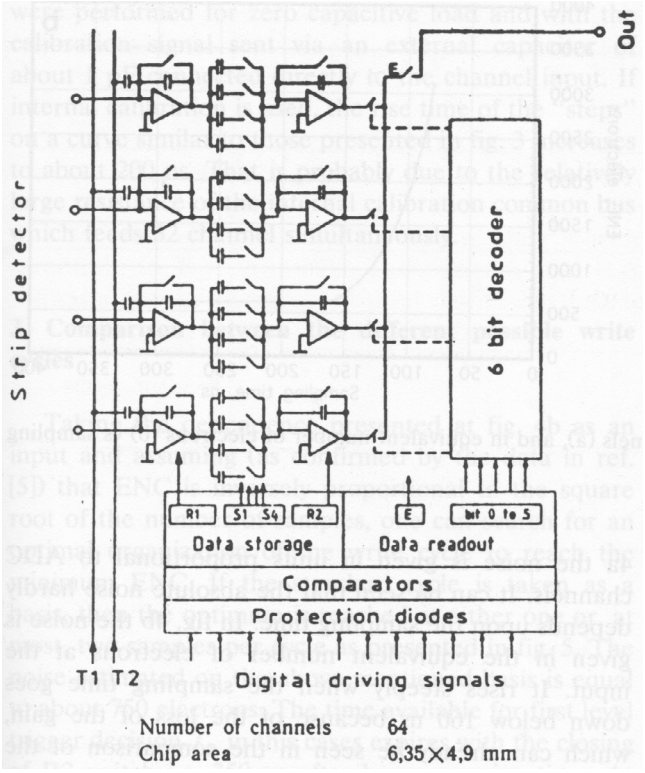


Fig. 19. Schematic diagram of 4 channels in the CAMEX64 ASIC. From [88].

with clamps so as to make the contacts with the 16-pad Si sensors inside, not using wirebonding. This arrangement, by chance, later enabled 400 °C annealing of the sensors, after radiation damage had occurred. Twelve ladders composed the inner cylinder, only 4.8 mm thick, with outer diameter 66 mm, and this was placed as a late upgrade inside the proton–antiproton experiment UA2 at CERN. The non-trivial insertion of this inner tracking system is captured in Fig. 22. It was somewhat ironic that the AMPLEX was designed a few years after the preceding ASICs, described above, but was immediately used in the UA2 collider experiment, during two years, well before any of the others entered operation in their vertexing and tracking systems in LEP, SLAC or the Tevatron.

It may be worth mentioning that only for MARKII, Delphi and ALEPH the silicon microstrip detectors had been foreseen in advance for use as the inner tracker, and for which the design work on readout ICs was planned beforehand. Silicon trackers and their specific ASICs

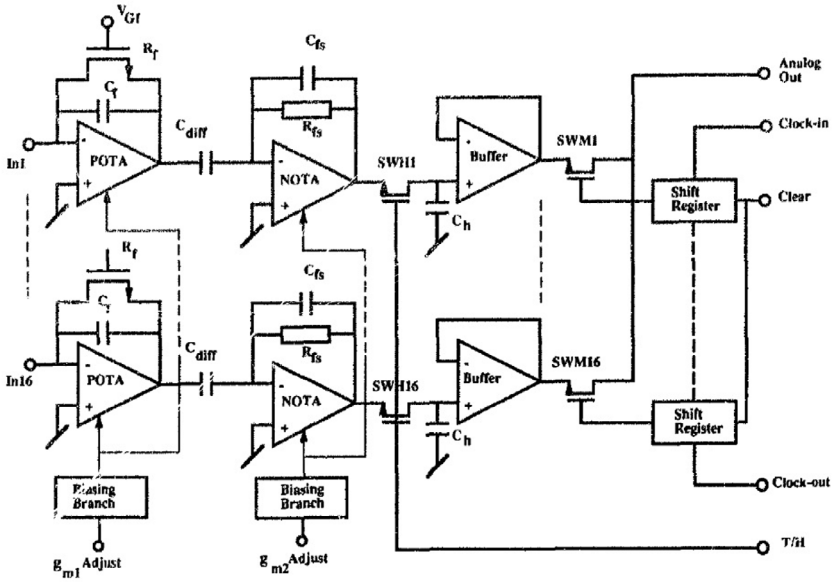


Fig. 20. Schematic diagram of 2 channels in the AMPLEX ASIC (source CERN and from [91]).

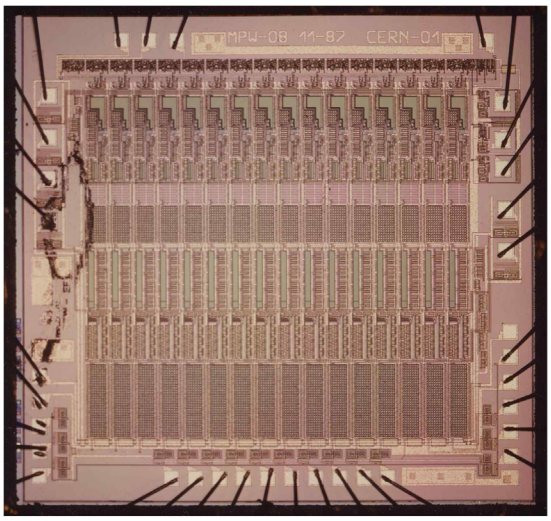


Fig. 21. Die photo of the 16-channel AMPLEX ASIC, size 4.1 × 4 mm^2. 10 inputs are at the lower edge, and 3+3 around the corners. (photo CERN).

Fig. 22. UA2 inner silicon array during insertion. The little white squares are the AMPLEX ASICs in their ceramic packages. (photo Claus Gößling).

in CDF, OPAL, L3 and UA2 were retro-fits. The same was also the case for the experiments D0, ZEUS and H1, which are not discussed here at all. Significant innovation in microelectronics was also undertaken by teams in DESY and in other accelerator centers, mostly for upgrading while their collider experiments were fully operating. This activity is unfortunately not covered further in this article. In all experiments, usually a few collaborators recognized the potential of the new silicon technology, and promoted the work and expense for the addition of this instrument. And often it had to find a place within an already designed or existing gas-filled tracking detector.

6.9. Channeling the floods of data

In the collider experiments at SLAC, DESY/HERA and LEP the event rates and data volumes increased by a large factor, in comparison with the previous fixed target experiments. One reason was the hermetic coverage with concentric layers of detectors all around the interaction point. A second one was the higher accelerator energies which dictated larger radii to stop reaction products and to measure their momentum and energy. More basically, the real reason was the low probability for the occurrence of the processes to be investigated, which made a high interaction rate essential. As already mentioned in chapter 4, the FASTBUS standard was developed to enhance the capability of the data processing electronics in view of the much larger quantities of data at LEP and other colliders. Phil Ponting and Henk Verweij [92] presented the evolution of electronics systems for those large experiments.

In practice, even the large FASTBUS cards had difficulty to accommodate the complexity which was needed, and commercially available ICs using ECL were not always optimal for the application. The high power dissipation by the numerous ICs on a board was an issue. Becoming aware of the potential of ASICs, a first project to improve the data handling in a FASTBUS card, was implemented by Alessandro Marchioro, together with colleagues from the Ecole Polytechnique in Paris, and RAL, all involved in construction of the ALEPH Event Builder. They designed a Direct Memory Access DMA controller ASIC chip set [93], using two gate array chips in the technology of the company European Silicon Structures ES2, in the south of France. A photograph is shown in Fig. 23 of the FASTBUS board on which 5 of these ASICs are included. Note that in 1986 only hardwired gate arrays were accessible, with metal layers on top of a basic array of cells. The Field

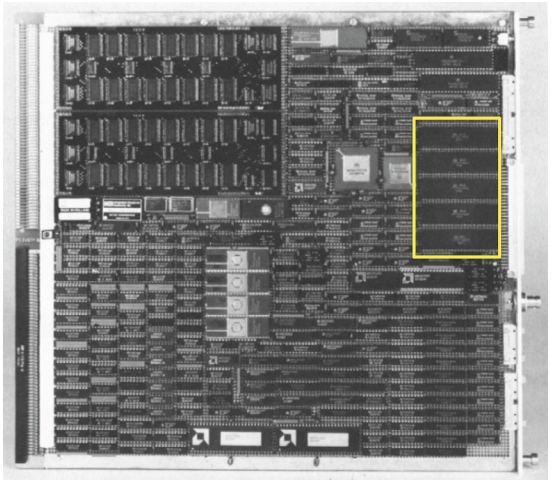


Fig. 23. FASTBUS CPU board of the ALEPH event builder, on which 5 gate array ASICs in the rectangle, middle-right (photo CERN and [93]).

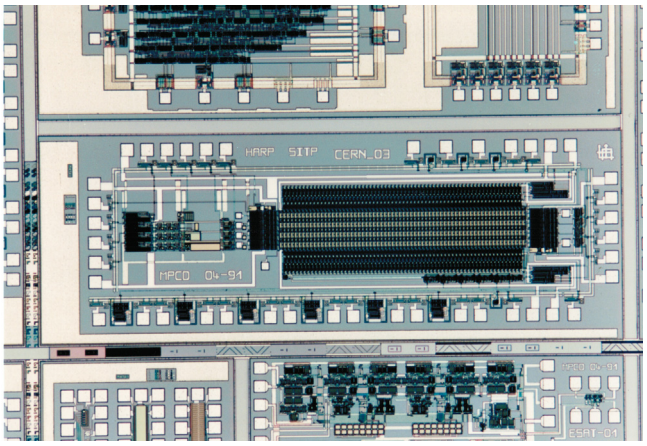


Fig. 24. Photograph of prototype of the long ASIC 'HARP' [96] with linear array of analog memory cells. Some other chips are placed around on this MPW. (photo CERN).

Programmable Gate Arrays FPGA which are widely used nowadays, just made a timid appearance at that time. The current, very complex FPGA need an increased number of connectivity layers on top of the chip, and these can now be made on the flattened surface, obtained each time after depositing a new metallization layer, thanks to the introduction of CMP, already mentioned in chapter 5.

Following up on the positive experience with this first logic ASIC, the ALEPH team continued ~1989 with more efforts to improve FASTBUS data processing. A 'slave' interface chip 'FASIC' was designed in a 1.0 μm CMOS technology with 3 levels of metal, on a sea-of-gates common substrate [94]. Quite a number of other logic ASIC projects followed, of which some are discussed in the contribution to this issue by Moreira and Kulis [2].

Because the data flood submerged equally the other collider experiments, there was a lot of IC design going on also elsewhere, apart from LEP at CERN. As only one example, the same team that had worked on the microstrip readout chips for ALEPH, implemented for the ZEUS experiment at DESY a number of circuits, such as the 10 MHz analog pipeline described by Buttler and colleagues in [95].

All the factors mentioned in the beginning, would play *a fortiori* at the LHC, and blow up the data volume into the Exabytes. The need for adequate processing ICs then motivated several teams to launch custom designs, using the methods and approaches which made the computer industry successful. An important function to be implemented in ASICs for different detector systems, was the temporary local storage of raw data, at the high interaction rate of the collider. A 1991 prototype chip with 32 parallel analog memory rows [96] is shown in Fig. 24. Capacitors were switched at 66 MHz, at that time the announced LHC collision frequency, and were charged one after the other by the amplifier output. Each linear array could store data during the trigger decision time of 4 μs. This IC was designed by Francis Anghinolfi, Pierre Jarron and colleagues, who dubbed it 'HARP' for Hierarchical Analog Readout Processor.

Another area of activity concerned the design of converters, which are used to digitize the original analog data coming from the sensors. Both signal amplitudes and times have to be digitized. The new approaches for data transmission under the new conditions, with close to a million sensing elements, have given rise to lively discussions about the most appropriate architectures. Many factors influenced the outcome, and in the proceedings of the LHC Electronics Workshops, mentioned before, the evolution can be nicely followed. In most cases, the digitization would take place in the ASICs on the detector. A notable exception was implemented in CMS for the inner tracker data, which were sent via optical analog links to the counting room. A more detailed treatment of ADC and TDC on- and off-detector can be found in the contribution [97] in this issue.

In this context, the major effort for the LHC experiments has to be mentioned, which was made for the transmission of the data from the detector, situated in the high radiation zone, to the processing and recording electronics, in the counting rooms further away. Further down the chain, a massive amount of electronics for on-line analysis, temporary storage and transmission is placed still underground, maybe 60 to 200 m from the detector systems themselves. Most of the data connections now use optical fibers, but some of the control signals, as well as power is supplied via room temperature copper or aluminum cabling. Extensive development work has been done for the optical fiber connections. Drivers and receivers have in part to be radiation resistant, and therefore were not available on the market. This optoelectronics is described by Jan Troska, François Vasey and Tony Weidberg, in this special issue [98].

6.10. Silicon pixels, the ultimate tracking detector asic, until now

When by the end of the 80's some expertise had been gained with the microstrip detectors in LEP, the CCD tracker at SLAC and with ASIC design in general, it became realistic, at least for the author, to dream of a true 2-D detector with high precision and high rate capability [99]. The need for fast 2D detectors under high occupancy, was obvious for tracking and vertexing in the planned Superconducting Super Collider in Texas, as well as for the, not yet finalized plans of an alternative proton collider at CERN. A collaboration between SLAC, the Space Sciences Lab of the University of California and Stephen Gaalema of Hughes Aircraft Company studied from ~1986 both CCD and hybrid assemblies with a separate sensor matrix and CCD or CMOS matrix as readout chip [100]. This work on hybrids was based on existing infrared imaging (IR) devices for space applications. These readout circuits used capacitive charge integration with correlated double sampling, and a fixed frequency clock for resetting, as usual for imaging devices. It was not clear at all, if a monolithic Si device could be adapted for fast recording, or if a hybrid approach with bump-bonded chips would be more suitable. The IR-imagers used CCD or slow CMOS chips with an addressable matrix, and were not useable at MHz frame rates.

Development of pixel detectors for particle physics started in earnest at the International Workshop at IMEC in Leuven, 31 May to 2 June 1988 [101]. Several specialists from industry and academia participated, such as prof. Eric Vittoz from CSEM/EPFL, who outlined a possible signal processor which would fit in a small pixel area [102]. Much of the history of the beginning of pixel detectors has been

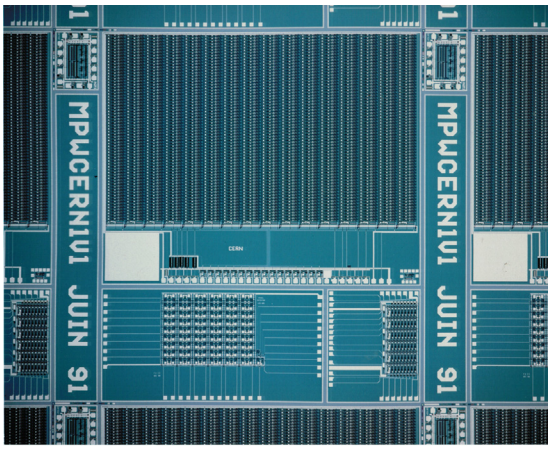


Fig. 25. Microphoto of pixel ASIC Omega2 on wafer, with some other chips for RD19. [CERN-Photo-].

documented in [103], and need not be repeated here. In this special issue, more recent developments in hybrid pixel electronics are covered by Maurice Garcia-Sciveres [104] and the monolithic implementations and perspectives are treated by Walter Snoeys [105].

Here it is interesting to recall the early, widespread scepticism. Main arguments were, firstly, that electronics would not survive for a reasonable time, such as 2–3 years, under the intense radiation in the middle of the collider, and secondly, that the high expense could not be afforded for a detector technology, which had not shown any viability at that moment.

For the designers of a first pixel readout ASIC, however, the main issues were how to accommodate in ∼0.01 mm^2 the signal processing functionality, that only 15 years before, would have occupied half a NIM crate, and how to deal with the power consumption in the restricted, enclosed central part of the experiment. It was essential to show solutions to these problems, working in a real experiment. The CERN team, in collaboration with the EPFL, and supported by the Swiss research fund and the LAA project, implemented a pixel readout design for hybridization [106]. A second version, shown in Fig. 25, was then actually produced as a complete detector and a setup with 3 planes was tested, autumn 1991 in the ^{32}S heavy-ion experiment WA94 in the Omega spectrometer at CERN. This experiment indeed had a very high density of simultaneous particles coming from each interaction, so that the performance of the new instrument could be convincingly demonstrated. Results were published at the IEEE Nuclear Science Symposium immediately afterwards, as a late paper [107].

During the 1988 Leuven Workshop, Sherwood Parker presented a project for a monolithic pixel detector, in a double-sided process, which would be implemented at the silicon facility CIS in Stanford University [108]. At the end of 1991, a telescope of monolithic pixel chips was then operated in a Fermilab beam by Sherwood Parker, Walter Snoeys and colleagues [109].

An important characteristic in the detection of minimum ionizing particles with small pixels, and which sometimes is not taken into account, is that the signal only depends on the thickness of the sensor element, and not on its sensitive area, such as it is the case for visible light imagers. The generated free charge carriers, remain mostly limited to a column of ∼1 μm diameter around the particle trajectory, which is always much smaller than the pixel dimensions. And if the pixel can be made small, the electronic noise, a function of the capacitance, can be much reduced, to a value <100 e$^-$r.m.s. Therefore, given similar signal amplitudes, the signal/noise is improved to the point that a pixel detector practically has no spurious noise hits anymore [110], even for a giga-pixel system, in comparison with a system with microstrip detectors, which have typical noise >400 e$^-$r.m.s.

This quick progress, over less than 3 years, was convincing indeed. Because these instruments would be placed in the center of the collider experiments, it remained to be proven that adequate radiation hardness of the sensors and the ASICs could be achieved. This will be discussed further in Section 6.12, and is treated also in the contributions on pixel detectors in this issue by Snoeys [105] and Garcia-Sciveres [104]. Eventually, the required radiation hardness of the pixel assemblies was obtained, although this still has to be ascertained for increased radiation exposure in the future.

After 3 decades of experience, it became obvious that experiments need the precision and rate capability, offered by pixelated detector systems. Resolving and tagging of secondary decays allows the selection of rare interactions, which can point to new physics phenomena. Could higher rates and still better precision, in position and timing, help in this search? This will be discussed briefly in chapter 8.

An interesting and not unexpected result of the pixel detector development is their use in a large variety of practical applications based on ionizing radiation, in non-destructive materials analysis, industrial processes, microscopy, in medicine, in space and environmental dosimetry. The instruments measure the incoming particles or converting X-rays one by one, so that their position and angle of incidence can be determined with μm precision, as well as the time in fractions of ns (see Section 6.13), and also the energy deposited by each particle. Signal processing proceeds fully parallel, at unprecedented rates. Most properties can be obtained as digital information. Moreover, if the pixels are small and the sensor is sufficiently thick, different particles can be recognized instantly from the shape of the cluster of hit pixels. This is a unique feature for dosimetry in space, where the identification of ions is not straightforward, while they have a large biological dose enhancement effect. Depending on the application, a small 2 cm^2 instrument, or a larger, stitched area can be used, with a matrix of edgeless units. This article is not the place for further discussion of such applications of the pixel detectors.

6.11. ASIC design solves a basic problem in collider experiments

In the early 1980s, the general opinion was that future high intensity colliders could be built, but that experiments would not be able to follow the rates of interactions and the flow of data. With the introduction of ASICs in the trackers at LEP, DESY and PEP at SLAC, progressively the potential of microelectronics was recognized. This led to the necessary innovation, which would allow the operation of experiments at much higher intensities. Once these first ASICs had been designed and installed, the teams became aware that many other applications could be envisioned. Studies were made for the planned SSC experiments, and then for possible scenarios at CERN. The Italian LAA detector R&D project at CERN bridged the financial gap at CERN between the LEP construction and the approval of the LHC. Thanks to LAA funding, the microelectronics team in the CERN EF Division could operate already in 1988. After the AMPLEX, projects were started on pixel detector development and radiation hardness. Design tools and software, the already mentioned Silvar-Lisco package, as well as equipment for transistor and noise characterization, became available. Access was organized to CMOS technologies at MIETEC-Belgium, at Faselec-Zurich, ES2 and other foundries. Design rules and parameter files were obtained, with CAD tools and support, as already discussed in Section 6.7.

Similar actions were undertaken in other laboratories and institutes around the world, too many to be described here in extenso. Quite a number of physicists and engineers became quickly adept in mastering these tools, measuring instruments and radiation testing. A solid basis was created, on which now for many years the particle physics community managed to exploit the potential of ASICs. This was described in 2014 by Snoeys in an overview of the impact of ICs in particle physics experiments [111].

Probably the most important function, which now could be implemented in ASICs for different detector systems, was the immediate,

local storage of all data, produced at the high interaction rate of the colliders, as described in Section 6.9. The data could be stored on capacitors as analog quantities, or in a digital memory, if the signal amplitudes were converted to binary numbers. Conversion had to be executed at the interaction rate, 40MHz at the LHC experiments ATLAS and CMS, and ∼1000 times slower in the ALICE experiment. After solving the data rate problem, still remains the issue of the strong radiation environment, which often destroys ICs, as was painfully discovered during the early space exploration.

6.12. Radiation and silicon devices

The Si diode detectors used in the muon shielding for the neutrino beams at CERN, Section 6.2, already suffered from radiation damage, especially showing increase of their dark/leakage current. The nature of the defects which generate this current, could be investigated using the Thermally Stimulated Current TSC method, referred to in 6.3. This showed that the muons mostly produced di-vacancies in the high-resistivity (>kΩ) material [41], increasing the diode reverse current and leading to lower resistivity of the original n-type bulk Si. Also gamma and neutron irradiations were undertaken, where the former had minor effects and the neutrons apparently caused complex cluster defects, with large increase of the current. Effects on electronics devices and circuits by ionizing radiation are discussed, for example by Andrew Holmes-Siedle and Len Adams in 'Handbook of radiation effects' [112] or by T.P. Ma and Paul V. Dressendorfer in 'Ionizing radiation effects in MOS devices and circuits' [113]. A large body of information is available in the Proceedings over many years of the series 'Nuclear and Space Radiation Effects Conference' NSREC, organized by the IEEE, and published in their Transactions of Nuclear Science.

The particle colliders, which were discussed around 1980, the Eloisatron in Italy and the proton collider at BNL, would feature an intense radiation field in the central region, where silicon instrumentation nevertheless would be desirable. This was a reason for detailed studies of radiation effects, and after the 1981 Fermilab Workshop [53] contacts were made at the NRL in Washington, mentioned in 6.5. Understanding was also gained by repeated attendance at the series of conferences on "Defects and Radiation Effects in Semiconductors", e.g. 1978 in Nice, France [114], and several NSREC conferences, which were until 2001 always held in the USA. A brief description follows.

Radiation can disturb the crystal structure, which leads to 'displacement damage', i.e defects which act as centers for the thermal generation of excess free moving charge carriers, leading to dark current. Radiation also creates ionization, resulting in free or trapped charge. The additional charge carriers can change the characteristics of electronic devices such as transistors, in different ways. Bipolar transistors which use current through the base-volume are especially sensitive, and for a while it was supposed that MOS devices would be less sensitive to irradiation, with electrons moving close along the surface, under a steering metal or poly-Si gate. However, ionizing radiation was found to create a remanent positive charge in the oxide layers, which separate the gate from the conducting channel. This charging then shifts the threshold value for turn-on/off of the MOS field effect transistor. Later it was found, in fact by Nelson Saks et al. at NRL [115], that for a very thin oxide layer, <3 nm, the positive charging can be compensated by tunneling of electrons, and threshold shift becomes negligible. This is also described in more detail in the article by Faccio [1].

Other types of damage caused by irradiation of electronics devices and circuits can occur. Very exceptional should be the 'transient' ionizing flash, which is a high intensity burst of mostly energetic gamma rays and neutrons, resulting from a nuclear detonation. The gamma flux then during a short time can become as high as 10^{12} $cm^{-2}s^{-1}$ [113], swamping all the parts of an IC with free electrons and holes, rendering circuit operation quite impossible. Such conditions do not occur in the collider experiments. On the contrary, very localized high ionization density can be caused by energetic ions or nuclear interactions, and this causes the so-called Single Event Effects SEE. These can take several forms: Single Event Latchup SEL, which is the short-circuit between the electrodes of the power supplies for the whole IC, leading to a continuous large current. After an SEL, normal operation typically can only be restored by interruption of the external power to the chip. If a very large current flow damages the gate isolation oxide of a transistor, this is called Single Event Gate Rupture SEGR, which cannot be repaired anymore in situ. Single Event Upset happens quite often in the experiments, and consists in a corrupt value of a node or memory cell. If this node is part of a control mechanism, it may cause loss of a significant fraction of data, or may cause the interruption of control, including timing functions, or go even as far as to stop the running of the whole collider. Special design with triplication and majority voting is needed, and also layout of the IC can strongly reduce the impact of SEU. In particular, inserting guard-rings and many well-placed contacts to the common bulk potential can mitigate the risks for SEE. To implement such precautions in the IC, it is necessary that the designers have full control over the circuit design and layout process, and also have appropriate simulation tools. Again, these aspects are discussed in the contributions by Faccio and Moreira-Kulis [1,2].

Starting from the mid 1980s, relations were built up with various suppliers of radiation tolerant ICs for space and military applications, both in Europe and in the USA. These were invited to present their products in the User Meetings, and at workshops. For example, Nick Van Vonno of the company Harris Semiconductor in Florida presented a hardened bipolar process in Lisbon [116] and they had also the AVLSI-RA CMOS technology available. SOI radhard technology was proposed by Honeywell in the USA, and by ABB-HAFO in Sweden. For several years, an intensive collaboration was pursued in the RD9 project, between CERN and the Thomson CSF group in Grenoble, to study application of their technology HSOI-3HD. The embedded oxide layer in SOI reduces SEE, but it becomes progressively charged and transistor threshold shifts of hundreds of mV appear. A total ionizing dose up to ∼20 Mrad could be more or less accommodated, but the noise of amplifiers increased quite a lot [117].

These radhard technologies generally used special, and usually secret, processing steps which would reduce the effects of the radiation on the oxides and silicon structures. However, by studying in detail the physics of the radiation interactions, it became clear that in more advanced, deep submicron CMOS processing, inherent properties of those technologies could be exploited to deliver rad-tolerant ICs without need for special process steps. This is described by Faccio [1]. Snoeys, Faccio, et al. [118] already showed at the Munich/Elmau Symposium in 1998 a radiation hardness of up to ∼1 Mrad for a pixel readout ASIC, using these special layout rules in a 0.5 μm CMOS technology. In 2000 for the final design of a similar pixel readout ASIC in a 0.25 μm CMOS technology, a total dose >10 Mrad could be ascertained, with overall acceptable noise performance. This chip in fact then was employed in the pixel system of the ALICE experiment at LHC, and has been used until the 2018 long shutdown. A general description was presented [119] of the possibilities for radiation tolerant ASICs, now becoming accessible for the LHC experiments. At that time, a radiation-tolerant cell library was developed for this 0.25 μm CMOS technology, and made available by the CERN team [120].

In parallel, further development of radhard SOI technology was undertaken by CEA-Saclay and LETI, resulting in a BiCMOS process called DMILL [121]. This was properly qualified and transferred to industrial manufacturing. The technology was supported by several institutes, collaborating in the RD29 project, with spokesperson M. Dentan. Also here a design kit for Cadence, a digital library, and a broker service were provided. Armani [122] reported a limited threshold shift for MOSFET after a 100 Mrad (Si) gamma irradiation. Several systems in the LHC experiments then were equipped with ASICs in the DMILL technology, and these also have been functioning satisfactorily for the first decade of LHC operation.

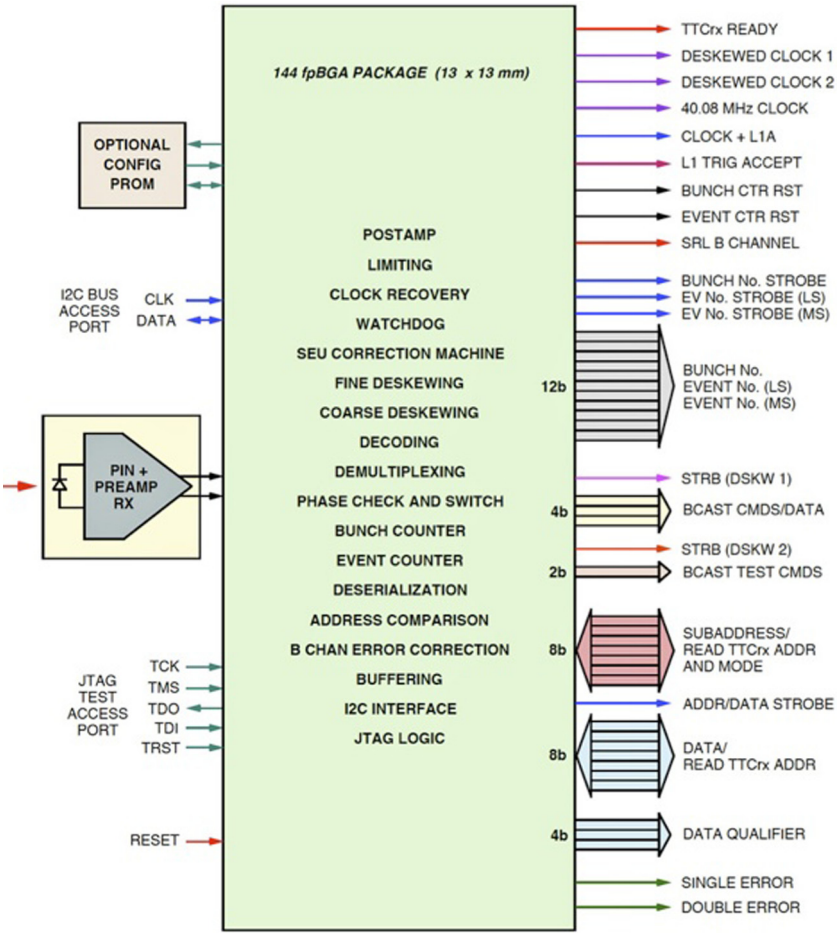


Fig. 26. Block representation of functions of the TTCrx ASIC (diagram CERN).

In conclusion, besides exploiting intentionally developed radhard technologies, also the use of a standard commercial 'deep-submicron' CMOS technology allowed to obtain radiation-hard ASICs, and this at lower cost. By very good luck, and thanks to the contacts of Alessandro Marchioro, it was possible to establish a durable commercial relationship with IBM, which allowed access to their 0.25 μm CMOS. At the same time, via the EU Europractice organization, the use of Cadence CAD tools came within reach, for practically all institutes participating in the CERN research program, under university-educational conditions. In this way, it was possible, to design a large number of different ASICs, for different applications in the experiments. Over nearly 15 years, prototypes and small production quantities of ASIC wafers have been delivered reliably.

6.13. *Timing is everything*

Further to the discussion in 6.9 of data transfer in large volume, it is interesting to introduce also some of the efforts to provide the distribution of timing around the collider. It is a complex task to bring together all data related to a given particle interaction at the collision point, and having these continuously occurring at 40 MHz. These sets of data are composed of signals from distances that can be far apart in the detector, so that in the meantime already 2 or 3 of the next beam crossings have occurred, each again with their produced outgoing particles. Moreover, an added complexity arises because information often is not analyzed on the detector itself, but signals may have to travel far outside the detector volume, to a counting room at large distance, and via cables of different lengths. All detector subsystems have to be equipped with precise, adjustable timing instruments, and ASICs play here a critical role. Fortunately, with the well-controlled underground temperature, hardly any component inside the large detector system is moving, once installed and adjusted. But the design and production of the timing systems has been a long and arduous effort, which started already in the framework of the project RD-12, in 1991 with the first spokesman Sergio Cittolin [123]. RD-12 formally continued until 2010, with evolving participations by many teams around the world. It was called "Timing, Trigger and Control Systems for LHC Detectors". In the end, the final version of a TTCrx ASIC was installed in most LHC detectors.

One of the early versions of the TTC ASIC, a typical example, was designed by Jørgen Christiansen et al. and published in the 2nd LERB Workshop in Balatonfüred, Hungary, in September 1996 [124]. This circuit would receive over a fiber-optic network the original LHC clock signals, and recover and distribute timing to the detector elements with precision well below 0.1 ns. The team published this with more details, at the 1995 IEEE Nuclear Science Symposium [125]. A Phase-Locked-Loop PLL circuit was produced in the same team, by Marchioro and colleagues, and published a year later [126]. The delays for the different detector elements could be digitally adjusted in steps of 1.04 ns, with a precision <0.15 ns r.m.s. An overview of the complete control system for the CMS tracker was then presented, and this illustrated the many points that had to be taken into account [127]. The complexity of the TTCrx ASIC is also illustrated in the diagram in Fig. 26 [128], where the numerous functions of the circuit are indicated. As this circuit had often to be placed in the highest radiation areas, several iterations were made, before it was acceptable, especially in view of SEE. For the control and timing system, upsets cannot really be tolerated. This is treated in some detail by Faccio [1].

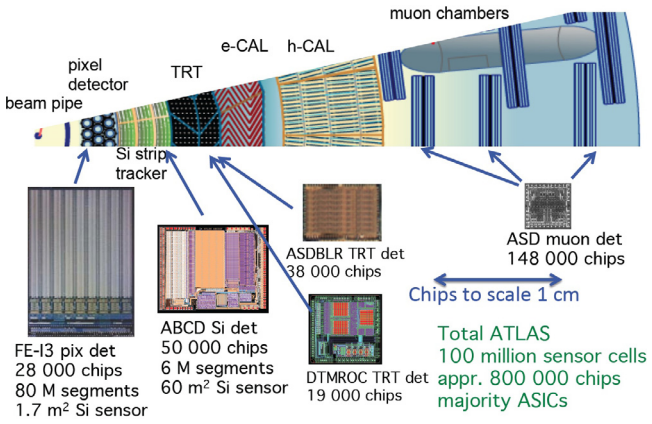


Fig. 27. Illustration of the radial positions of different systems in the ATLAS detector, each with one of their main ASIC front-end readout chips. The numbers refer only to the chips shown. In addition, many more ASICs are present in ATLAS.

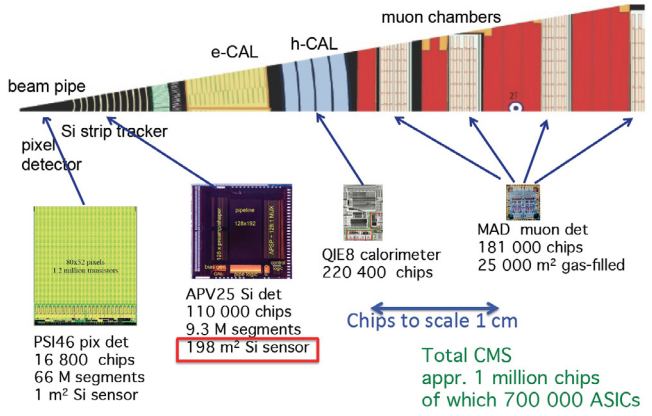


Fig. 28. Illustration of the radial positions of different systems in the CMS detector, each with one of their main ASIC front-end readout chips. The numbers refer only to the chips shown. In addition, many more ASICs are present in CMS.

It could be interesting to remember that time measurement ~GHz already in the 1950s could be made with <ns precision, with photomultiplier tubes and circuits using the electron vacuum tubes of the time. Over many years, contrary to most aspects of electronic circuits, the speed has only crept up slowly, and even today the smallest transistors, using materials different from standard Si, cannot go easily into THz frequencies. Now timing has entered the ps domain, with experiments such as NA62 at CERN, which uses a very high density pion beam, and therefore needs a beam hodoscope with particle tagging capability better than 100 ps [129]. An overview of operation in the ps region was given by Christiansen [130]. However, especially in density and power, enormous progress has been made in circuit performance. As an example, consider the recent Timepix4 imaging readout chip, 28.2 × 24.6 mm^2 [131], which incorporates both signal amplitude measurement and timing measurement with 0.1 ns precision in each pixel of the 512 × 448 matrix of 229 376 pixels. A long way from Wilkinson's 1948 single ADC which occupied a full rack. This imager can be used for advanced time-of-flight measurements, e.g. with neutrons, nuclear decay analysis, and many other applications.

7. Integrated circuits in the collider experiments

The size, the need for segmentation and complexity, and the reduction of power dissipation of the experiments at the CERN collider LHC have been the most compelling reasons for the widespread introduction of specialized CMOS ASICs in particle physics. Without ICs, it would not have been possible to deal with the high interaction rates and event multiplicities, inherent to this particle accelerator. All experiments adopted strategies to develop and produce adequate instruments with ASICs for the study of the physics phenomena in this new range of energy and particle mass. The two large experiments ATLAS [132] and CMS [133] each installed far more than a million ASICs to process the signals and control the operational conditions of the various detector components. Fig. 27 illustrates in a simplified way for the ATLAS experiment the positions of different systems, and a few chip photographs of (in most cases) their front-end readout ASIC. A similar schematic for the CMS detector components is shown in Fig. 28. The approximate numbers shown in these Figs. 27–28 refer to only these pictured ASICs. They do not take into account the many ASICs for timing, control and other functions, so that the total number of ASICs in each experiment may even come close to 2 million. In addition, the electronics in the counting rooms for data processing is not taken into account either. There mostly commercially available, packaged circuits have been used, such as FPGA. Much of this electronics is placed 'close' to the detectors in rooms underground, and some in the surface buildings. Moreover, all around the world, massive facilities are used with electronics, computing and data storage for the off-line information extraction from the original measurement data.

If also the components are added for the other experiments ALICE and LHCb, the number of ASICs for the original LHC experiments may add up to quite some millions of units. A significant fraction of these have been manufactured between 2000 and 2007, in a 0.25 μm CMOS technology, under a direct contract with the IBM foundry service, and a smaller proportion in the DMILL technology. The foundry cost has been quite acceptable, considering the overall budgets for the experiments. Precise numbers are not available, but the expenditure for CMOS manufacturing is estimated at less than 20 M€, including prototypes. The cost for the readout chips made in the specially radiation-hardened BiCMOS technology DMILL [121] has to be added, which may have been about half of the previous number. Besides the chip manufacturing itself, also the cost for design and engineering, as well as the cost of testing and board assembly should be taken into account. The cost for cables was considerable as well. The microelectronics work involved probably ~150 scientists and engineers over a 6-year period. Much has been executed by relatively inexpensive Ph.D. students and Postdoc's, so that a cost estimate of ~60 M$ may not be far off, about twice the cost of the chips themselves. Estimating the overall cost of the detector hardware and support structures is beyond the capabilities of the author, a daunting task.

However, in hindsight, one thing can be concluded: the budgetary prospects for signal processing in the LHC experimental radiation environment would have been pretty hopeless, if circuit design and production would have been undertaken in a way, similar to what is usual for comparable radiation environments in space or for military scenarios. Circuits for these applications often are commercially produced at a cost in excess of 1000 US$ per unit. The main reasons for this high cost lie in the small number of units needed and the exhaustive test and trace procedures imposed by space qualification protocols. The numbers needed for particle physics also are modest, in comparison to most commercial applications. But the approach of self-reliance chosen in particle physics, both for the design and the acceptance testing, has allowed to achieve well-functioning devices at relatively affordable expense. Overall cost of the microelectronics probably was between 5%–8% of the total experiment cost. Cabling, cooling, etc. are not included here, and cost of working hours is very approximate.

In the following chapter, the possibilities of ever more powerful microelectronics instruments will be discussed. Already during the first decade of the LHC collider operation, improvements have been prepared, which have now been installed during the first long shutdown. Later on, quite a few types of the chips mentioned in Figs 27–28 are planned to be replaced during the following accelerator shutdown, LS3 starting 2026. These aim to enhance performance during the running of

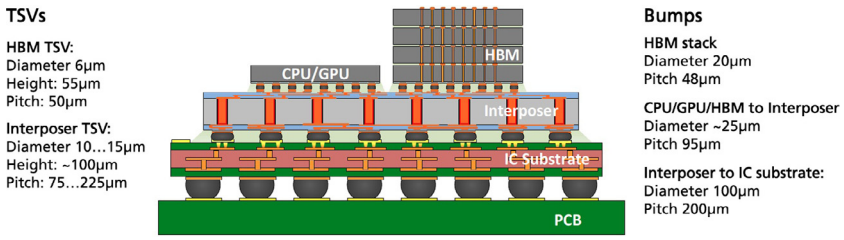


Fig. 29. Sketch of a 3D assembly using TSV, interposer and chiplets on top.

the High Luminosity HL-LHC after 2029, especially to allow increased rates of the interactions. There is the issue, touched upon in the next chapter, of the long lead times which prevent the use of really innovative electronics possibilities in these demanding systems.

8. The point of 1 nm technology, from planar to 3D space

Would there be good reasons for future particle physics experiments to exploit the newest silicon IC technologies, such as 32/28 nm, or even technologies with FinFETs at 14/10 nm or below? In 2022, the future generations named 3, 2 and 1 nm are reported to be under development in the laboratories, and are planned to come in production later this decade. Because the silicon crystal lattice parameter is 0.54 nm, it looks quite impossible to make a classical field-effect transistor with a length of only 2 atoms, or to manufacture metallic connections with this small width. Also, at such small dimensions the device characteristics would become quite unpredictable, due to lack of uniformity in the distribution of doping atoms, inherent to the usual random implantation methods. Instead, a technology parameter of 1 nm is not anymore a physical dimension, but essentially indicates a better performance in functionality and power density, in comparison with earlier technology nodes such as 32 nm.

Until ~2010, when 28/32 nm came in operation, the successive chip technology generations were indicated with their real minimal dimensions in µm or nm, as already shown in Fig. 10. This length did correspond indeed to minimum transistor gate length and distance between metal lines at the transistor level. But from then on, the numbers became 'symbolic' and also do not have the same meaning anymore for different manufacturers. For example, the Intel 10 nm is in many ways similar to the TSMC 7 nm node.

The improvements in successive nodes now are achieved by packing the components closer together in the layer, and even more by stacking several such layers on the same surface area. This stacking can be in selected places only, or over the whole chip. A sketch of a stacked assembly with several active layers is shown in Fig. 29. The smaller chips on the top are called 'chiplets'. Approximate dimensions for various parts are given as well. The resulting assemblies may dissipate so much heat, that built-in, active cooling is needed. As the cooling mechanism the liquid-to-gas phase transition of CO_2 is more and more exploited. The liquid can be pulled through channels etched in the Si, by capillary action and evaporation at the outlets. This has been already used in several systems in CERN experiments, such as in the NA62 Gigatracker. Also for the LHC experiments, this cooling was installed in 2021 in the LHCb VELO inner pixel detector. An overview was written by Alessandro Mapelli [134]

An example of a stacked assembly already in production, is illustrated in Fig. 30. This is an integrated CMOS image sensor from the company Sony [135], made in 90 nm technology, connected by metal contacts on each pixel (6.9 µm × 6.9 µm) to a signal processor chip in 65 nm CMOS technology. Each of the 1 462 272 pixels is connected to a 14-bit ADC in the logic chip. One reason for this innovation is to address the issue of image lag with fast moving objects, by implementing a global shutter action. In fact, also in physics experiments, a global timing for simultaneous exposure is used.

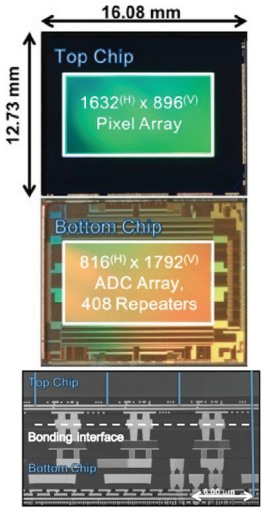


Fig. 30. Back-illuminated image sensor matrix with global shutter for visible light on top, made by Sony [135], using 14-bit ADC in parallel on each 6.9 µm square pixel in the CMOS chip below. A cross-section shows the copper interconnects between the 2 chips, and the scale with arrow of 6 µm.

For the use of new ASIC technologies in physics experiments, it is essential to be informed about the advanced functionalities becoming available. Engineers specialized in chip design unfortunately may have only an approximate knowledge of the requirements in the evolving physics landscape. Vice-versa, the experimental physicists do not quite know what recent technologies are capable of. In commercial exploitation of new and expensive technologies, the main drivers are increased processing capability for large data volumes, wireless transmission, higher speed and lower power consumption. Consumers now can play complete movies on their smartphone, and apparently, this allows a chain of companies to earn enough money to justify the difficulties and cost of nanometer silicon technology.

What potential then is there for physics experiments? If the hints towards new elementary particle physics are hidden in small deviations from the parameters in the standard model, amidst a massive number of conventional results, it will be worthwhile to drive event rates and data processing towards hitherto unknown quantities. At the existing LHC collider, this would involve increasing collision rates still further, even beyond 1000 interactions per bunch crossing. Slicing the crossing duration of ~1.2 ns in 10–20 sub-periods, could make event reconstruction manageable under such conditions, but a lot more data must be stored locally, and ps timestamps have to be added, probably for all detector components. The recent pixelated ASIC Timepix4 [131] can already record timestamps with precision <100 ps in all the pixels. Various approaches are underway to further improve timing precision, as discussed briefly in Section 6.13. In addition, precision timing opens up other possibilities as described below.

An innovation which would be alternative or complementary to a 'simple' increase of statistics, could be the improvement of the precision of the measurements of the particle energies and momenta. This

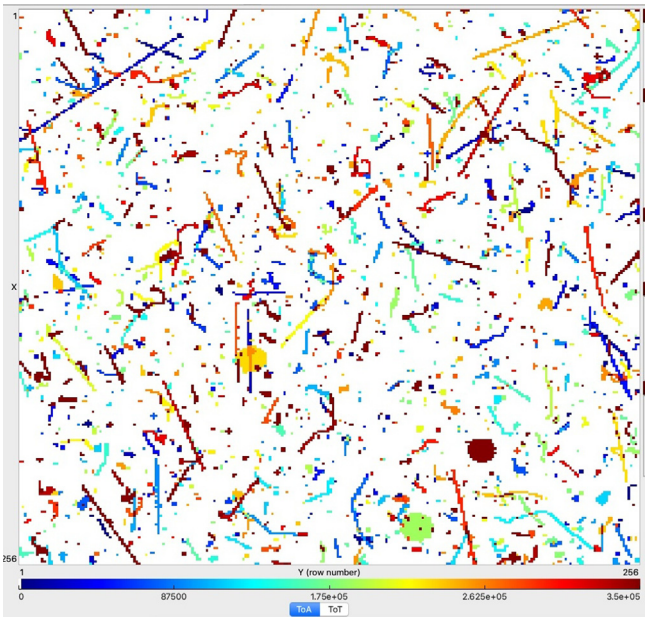


Fig. 31a. Exposure of a Timepix3 detector at sea level during 5600 s. The arrival timestamps are divided over a range 0 to 350 000, so that each bin here is 16 ms. Many muon tracks have been recorded, as well as 3 alpha particles (light green, yellow and dark brown spots) and numerous electron clusters, of which many in fact are converted X-ray photons.

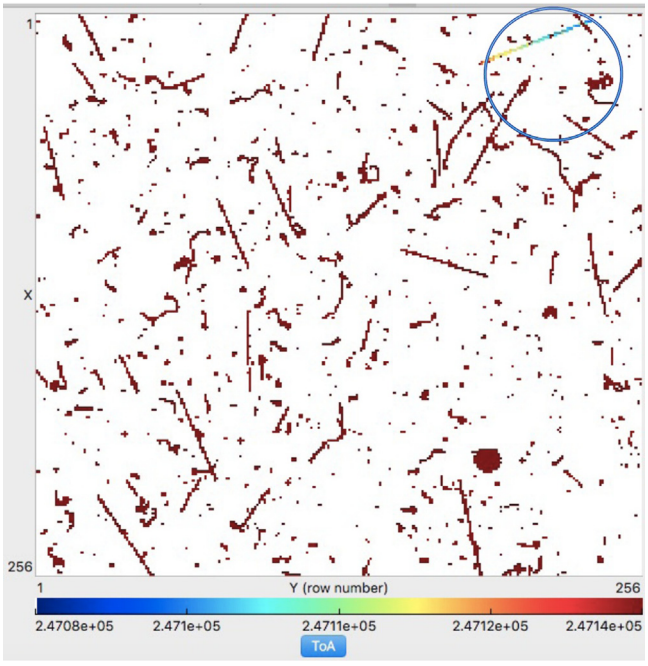


Fig. 31b. The same exposure, but now the range has been narrowed to 247 080–247 140, and all clusters generated before the lower limit are suppressed. Those afterwards, dark brown, are shown as in overflow. The selected muon track of interest, encircled in the top right corner, is filling here 50 of the 60 bins. The timestamps in each pixel are a measure for the depth in the 500 μm silicon thickness where the energy deposition occurred, thus creating voxels with dimensions better than $50 \times 50 \times 50$ μm^3.

might contribute to verify small deviations on particle mass, energy or spin. Such deviations, if real, could provide the needed hints towards new physics, long before higher energies for particle acceleration will be available. In this context of improved precision, it can be mentioned that ps timing in Si pixel detectors also opens the possibility

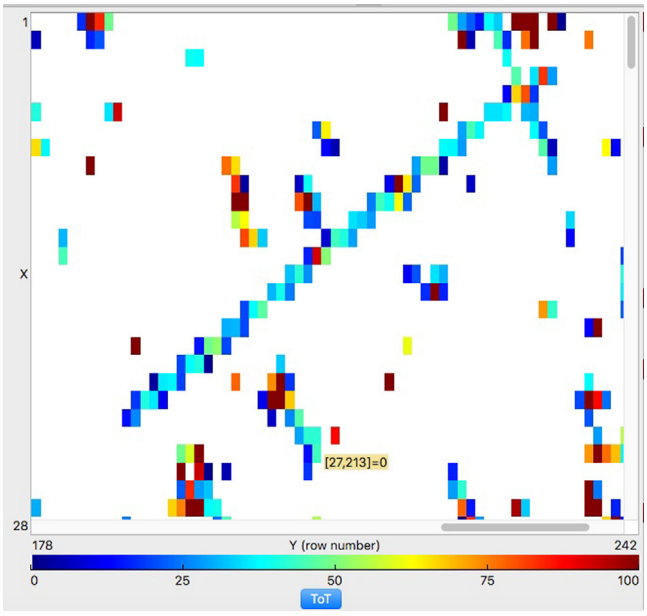


Fig. 32a. Enlargement of the selected muon track, showing the energy in keV deposited in each pixel. The color scale runs to maximum 100 keV. Deposits vary from 14 to 49 keV. For overlapping clusters from different incident quanta, such as for the selected muon in the top right, their energy deposits are added up, resulting in a 'corrupted' value in between valid ones.

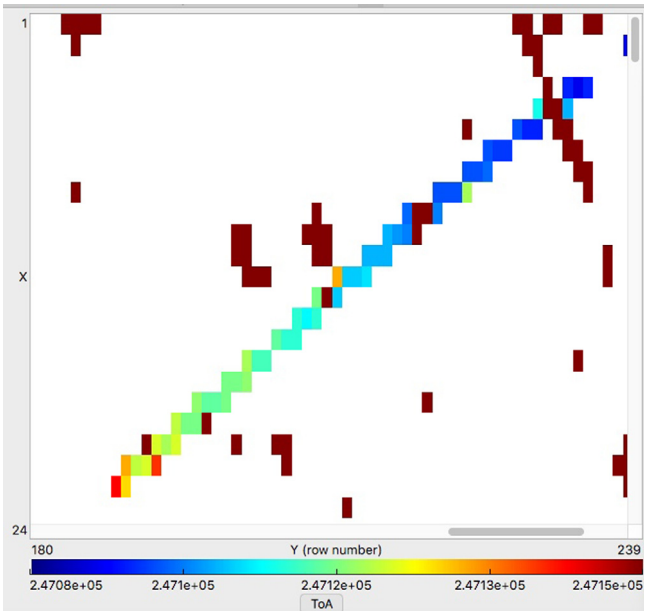


Fig. 32b. Enlargement of the selected muon track, showing the timebins of signal arrival at the pixel contact. Range as in Fig. 31b. The maximum hole transit time for the pixels at the far end, at an applied field of 200 V on 500 μm Si, can be estimated at 50 ns, with hole velocity $\sim 10^8$ ms^{-1}.

of precision tracking within a thin layer. An increased number of voxels (basic volume elements), maybe even 10–15, could be used to determine the particle trajectory, instead of the single point from a surface-defined pixel. This was already pointed out by Filipenko et al. for use in doube-beta decay studies [136]. More recently, Bergmann et al. [137] showed such 3-dimensional track reconstruction based on voxels, volume elements in the Si with dimensions <50 μm on all sides. They used a 500 μm thick Si pixel detector, exploiting the 1.5 ns timestamp information from the Timepix3 ASIC. It is now possible in

a thin semiconductor crystal, to measure stubs of tracks, as in a Time Projection Chamber, similar to the one described in Section 6.4, but also at MHz rates. In an LHC experiment, this could be done in a few layers, at different distances to the primary vertex of the interaction. An example of the measurement for a selected muon track from a long exposure with the Timepix3 detector, is shown in Figs. 30a–30b and Figs. 31a–31b. The Timepix3 measures amplitude and signal arrival time simultaneously in each pixel. Incidence can be recorded with ns precision, even over long exposures, by keeping track of the 'roll-overs' in the FPGA used in combination with the pixel readout ASIC. The simultaneously recorded signal amplitudes, shown in Fig. 31a, can be used to correct for the timewalk of the 'late' timing signals in Fig. 31b. The same team [138] also made full 3D reconstructions of nuclear interactions in a 1 mm thick CdTe crystal. While known particles produce characteristic clusters of pixels, a search for unusual phenomena and exotic sorts of ionizing quanta could become 'easier', especially once artificial intelligence algorithms have been developed.

For practical use at high rates in LHC experiments, such instruments will need sophisticated on-chip processing, for which new nm technology can be used, possibly implemented in chiplets on top of the more conventional "mother-chip". This pixel readout chip could still use e.g. 28 nm CMOS.

In this way, novel 3-dimensional silicon structures, with inter-layer connectivity would lead to tracking and vertexing with more measuring points than the 5–15 which are currently available. A first-order vector could be associated with the space point that is measured until now, even using a relatively thin single Si layer. Moreover, such instruments will be sensitive to all sorts of ionizing quanta, that may be created near the LHC interaction points, There is no need for any trigger, as long as data can be processed locally or transmitted effectively, maybe even wireless. Such new instrumentation could be possible even without very much increasing the material thickness, as a larger number of data points can be recorded in a single layer. The reduction of power in the digital part, using low-nm CMOS, may help quite a bit, as in your smartphone. Detailed studies are needed to make sure that all this can work in real life, and that cost remains affordable, balanced against potential physics results.

Such new approaches will require significant work in microelectronics, and a lot of retro-fitting. Still, it is likely, that a significant investment in nanoelectronics, certainly in the short run, can help to find new physics earlier than it will be possible with the much larger, long-term investment in the very high energy accelerators. One may hope that solid indications for new physics from the former, then can secure the large funding needed for the latter Fig. 32a.

9. Conclusions

Conclusions relate on the one hand to the changes which have been implemented over the years in the particle physics experiments, and on the other hand to different circumstances which allowed this to happen. Starting with the latter, it still may be interesting to recall the prevailing opinion ~1985, that a new accelerator would be possible, but not the experiments, with the available technologies. A multi-TeV, high intensity accelerator/collider could technically be built, if economically expensive, and could produce interactions with sufficient energy to produce the expected, new types of particles, with a 'Higgs' boson as a near-certain example. Plans for the SSC, LHC and HERA were close to decisions. However, experiments along traditional lines could not be imagined to deal with the rates and radiation intensities, produced in these colliders. Especially at the slightly lower energy, foreseen for LHC, in comparison with the SSC, and therefore the compensating higher intensity in the experiments. A design was even proposed, in which the collisions would take place within a steel enclosure, with only the muons coming out, from which then new particles would have to be reconstructed. The LEP experiments, running at 50 kHz, recorded one interaction per 20 μs. For the new collider this would have to be increased by a factor 1000, with intensity $\times 10^4$ or even higher. During an SSC workshop in 1989, it was claimed by radiation experts, that no electronics whatsoever could survive inside an LHC tracking environment Fig. 32b.

Against this background, initiatives for detector R&D were contemplated, but budgets at CERN already were stressed by the simultaneous building and operation of the UA and LEP at CERN. Fortunately, for CERN an external source of detector R&D funding came up in 1988, with the Italian-supported LAA program. A few years later, in 1991, this could be supplemented by the dedicated CERN Detector R&D program, with wider participation, even if it had a relatively lower budget. Several technical committees were created in this context. The LHC Electronics Board LEB organized regular user meetings. Subjects in microelectronics and radiation hardness were discussed in quarterly Microelectronics User Group MUG meetings, where also world-renowned specialists were invited. The tolerant and 'bottom-up' attitude towards innovative approaches helped numerous initiatives. It is here also the place, to stress the need for continuous and close contacts with scientists in technical areas and industry, outside the particle physics world. Travel to trade fairs, conferences and industrial laboratories is not a luxury, but a necessary investment, to create a basis for innovative action in our own field. It also is essential that staff can rely on contacts with outside specialists over periods of many years, when old problems finally may find solutions in new technology. In this article, the author tried to present several examples of 'serendipity' where chance encounters or old acquaintances triggered important steps forward.

Coming then to the results of these various R&D efforts, it is rewarding to see that very satisfactory electronic instruments after all have allowed the LHC experiments to operate successfully over their first decade. They all could amass data at the unprecedented rates, and now even contemplate rate increases for the future. This has been possible within their fairly tight budgets. The work by many inventive scientists paid off, against the early, dark expectations.

It is no exaggeration, to conclude that the use of self-custom-designed microelectronics ASICs has been one of the main enablers, making the originally impossible looking experiments a successful reality.

Declaration of competing interest

The author declares that he has no known competing financial interests that could have appeared to influence the work reported in this paper. The text is largely based on the many personal relationships developed over 50 years.

Acknowledgments

Hundreds of physicists, engineers and technicians have worked for years on the innovation of electronics for the particle physics experiments. A number of projects and their actors have been mentioned in this article, but many others remained unnamed. Personal viewpoints of the author unavoidably skewed this presentation of historical developments. Many statements in the text are not justified with literature references, which otherwise would run in the hundreds. The author would welcome criticisms and comments. These could be helpful if ever a book would describe in more detail the endeavour in microelectronics, which rejuvenated this field of physics. Anyway, the author is indebted to many colleagues, who have worked hard over more than five decades, to create ever better adapted detectors and electronics for current and future experiments at CERN, and around the world. Ideas, support and hardware have been forthcoming from the academic side as well as from the industrial side.

Nameless reviewers have scrupulously looked at this article and are gratefully acknowledged for their useful suggestions for improvements. Thanks also are due to the staff of the CERN library, who provided

access to literature resources, which in their form of electronic archival, turned out to be unusable or non-existent.

After all the years of working together, the author likes to thank the closest colleagues, among many others at CERN, in temporal order: Giorgio Cavallari, Pierre Jarron, Alessandro Marchioro, Michael Campbell, Walter Snoeys, Rafael Ballabriga, Xavi Llopart and Jerome Alozy. Also he likes to mention Pierre Lazeyras, Adolf Minten, Horst Wenninger and Antonino Zichichi, because they encouraged and supported these electronics developments at CERN, which otherwise might not have been possible.

At the industrial and professional side, between the support from many companies, it is justified to single out the willingness of IBM, to open up their processing facilities in 0.25 μm CMOS, for the needs of particle physics and the LHC, a customer with only a tiny volume of chips. Especially the encouragement by Robert Dennard has to be mentioned. The IEEE and the institutes IMEC in Leuven and EPFL in Lausanne continuously have been sources from which originated a lot of expertise and inspiration. And since 30 years the Medipix collaborations (http://medipix.web.cern.ch/MEDIPIX/) [139] have been an excellent framework for the innovation in ASICs, which then resulted in new instruments for the particle physics experiments.

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