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CRaTeBo: a high-speed, radiation-tolerant and versatile testing platform for FPGA radiation qualification for high-energy particle accelerator applications

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Abstract: The CHARM Radiation Tolerant FPGA Tester Board (CRaTeBo) is a FPGA testing platform for the CERN High-energy Accelerator (CHARM) irradiation facility. It is meant to ease the radiation testing of FPGA-based systems by providing users with a radiation-tolerant carrier card featuring an FPGA interface, a high-speed communication interface, a flexible power supply, and an HPC-FMC connector for additional front-end electronics. It is foreseen to be a permanent installation in the CHARM facility at CERN, giving users the possibility to carry out radiation tests of their system with minimum effort on the test setup development.

Keywords: Modular electronics; Radiation damage to electronic components; Radiation-hard electronics; Accelerator Applications

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1 Introduction

Field-Programmable Gate Arrays (FPGAs) are widely used in electronic systems because of their performance, flexibility, and cost-effectiveness. However, their lifetime and performance are influenced by Single Event Effects (SEE) and Total Ionising Dose (TID) effects. At CERN, many systems involving FPGAs are used in the Large Hadron Collider (LHC) radiation environment, thus their qualification is crucial to ensure the reliable operation of the experiments. However, radiation testing involves multiple challenges, concerning both the design under test and the irradiation test setup. The most common procedure for qualifying an FPGA consists of testing each of its elements individually, even though this procedure does not allow the failure rate estimation of the actual application nor the comparison with other FPGA families. In recent works [1–3], the authors discuss how to overcome such limitations by using benchmark circuits, improving the qualification process by enabling comparisons of SEE and TID performance between different FPGA technologies. Nonetheless, retrieving the failure rate of an actual application remains a challenging task, particularly for systems involving additional front-end electronics, such as detectors applications. Therefore, testing actual systems in operational conditions remains a critical aspect. Moreover, the radiation environment of the LHC is made of different particles over a large spectrum of energies, whose distribution changes depending on the location. Thus, it is crucial to assess the behaviour of the system in a representative radiation environment. This can be achieved at the CERN High-energy Accelerator (CHARM) irradiation facility, where the mixed radiation field comprises a multitude of particles at different energies, which can be adjusted

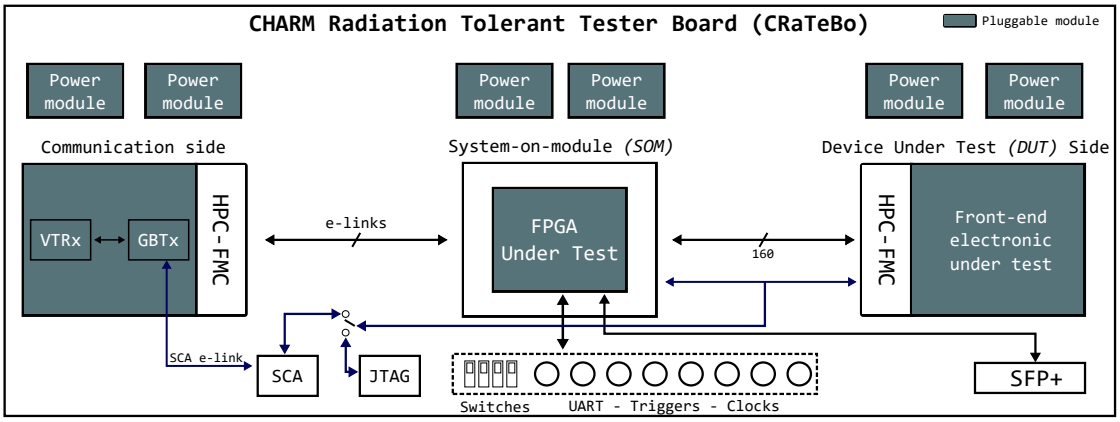

Figure 1. CHARM Radiation Tolerant Tester Board (CRaTeBo) block diagram.

by selecting the type of target, shielding, and test position [4]. For these reasons, CHARM is extensively used for the radiation qualification of all the systems before their installation in the LHC tunnel. However, differently from facilities where tests are performed using particle beams whose size is in the order of centimeters, at CHARM the whole system is exposed to radiation. This constraint limits the possibility of using commercial development kits because other components may fail, reducing the observability of radiation effects on the Device Under Test (DUT), or preventing the test in case of destructive events. Therefore, a dedicated test board should be prepared, increasing the development time for the radiation test setup. To address these challenges, the CHARM Radiation Tolerant FPGA Tester Board (CRaTeBo) was developed. It is designed to ease the radiation testing process of FPGAs and other systems providing all the essential features to conduct radiation testing, i.e. interface to the FPGA, communication link, and power supply. These features have a great degree of flexibility to accommodate many kinds of tests. Moreover, all the components are either radiation qualified COTS or radiation-hardened by design. Its flexibility, coupled with its radiation tolerance, provides a platform that dramatically reduces the user burden in the test setup preparation.

2 Implementation

CRaTeBo is thought to be as versatile as possible to allow radiation testing of systems with different requirements in terms of supply and interfaces. The board features a custom System-on-Module (SOM) socket to host FPGAs. It mounts a High-Pin Count FPGA Mezzanine Card (HPC-FMC) connector compliant with the ANSI/VITA 57.1 standard [5], which allows testing those FPGA-based applications that may involve additional electronics such as acquisition systems, control and radio-frequency applications. A radiation-tolerant link is available on a second HPC-FMC connector for communication with the DUTs. A flexible power scheme is implemented through a set of interchangeable power modules that can be adapted according to the system under test. Figure 1 shows the block-diagram of the board with all its main functionalities described hereafter.

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2.1 GBT/Versatile Link interface

The communication between CRaTeBo and the host-PC is based on the Versatile Link [6]. It is a bidirectional optical link operating at rates up to 4.8 Gbit/s. For such link, the board uses the Giga-Bit Transceiver ASIC (GBTx) [7], a radiation-hardened by design serial transceiver implementing the GBT protocol [8]. It can survive up to 1 MGy of TID, and a Displacement Damage (DD) of 1×10^{16} 1 MeV neutron equivalents/cm^2 . The ASIC is mounted on the L-GEFE FMC mezzanine card, which was developed in the context of the GBT-based Expandable Front End (GEFE) [9] project. On one side, the GBTx transceiver communicates with the FPGA under test through multiple low speed (40 at 80 MHz, 20 at 160 MHz or 10 at 320 MHz) electrical links named e-links. On the other side, it communicates with an FPGA-based back-end through the Versatile Link using the VTRx [6], a radiation tolerant (up to 500 kGy of TID, and a DD of 2×10^{15} 1 MeV neutron equivalents/cm^2) optical transceiver. The main reason for choosing this communication link is its widespread use in LHC systems for high-energy physics experiments and beam line control. Therefore, when testing systems based on this communication link, CRaTeBo simplifies the test development because the link is already implemented. In addition, the GBT/Versatile link brings two more advantages. Firstly, it enables reliable communication with the DUT, preventing the corruption of experimental data and allowing testing over an already validated radiation-tolerant communication link. Secondly, the link provides the opportunity to test more demanding designs involving high-data rate processing, such as high-data speed ADC/DAC used in the acquisition system for detector electronics. Nonetheless, the availability of the FMC connector enables future development of other communication interfaces when needed. Wireless modules are currently under development in this regard.

2.2 FPGA System-on-Module

The board implements a System-On-Module (SOM) socket to host FPGAs. A custom solution was developed since no standard SOM form-factor existed on the market. It uses three SAMTEC ADF6-60-03.5-L-4-2-A high-density connectors, providing 260 populated I/Os for FPGA signals. The FPGA has access to the e-links for communication with the back-end through the Versatile Link, and to the second HPC-FMC connector to interface with any analog/digital electronics. In addition, it is connected to LEDs, buttons, switches, and six external signals through on-board SMA connectors. Figure 2 shows two SOMs developed up to now for the PolarFire FPGA, from Microchip, and the GateMate FPGA from CologneChip [10]. Nonetheless, other international collaborations are underway for testing other FPGAs.

2.3 Front-End interface

There are many circumstances in which an FPGA application runs in tandem with some specific digital or mixed-signal system, such as an ADC mezzanine card for sampling the analogue signals from a beam position monitor (BPM) system. In these cases, it is useful to test the full system under radiation. For this purpose, CRaTeBo provides an HPC-FMC connector, defined in the ANSI/VITA 57.1 standard, that can be used to test applications including FMC-based front-end electronics. In addition, the compliance with the standard enables testing of any other commercial module based on it.

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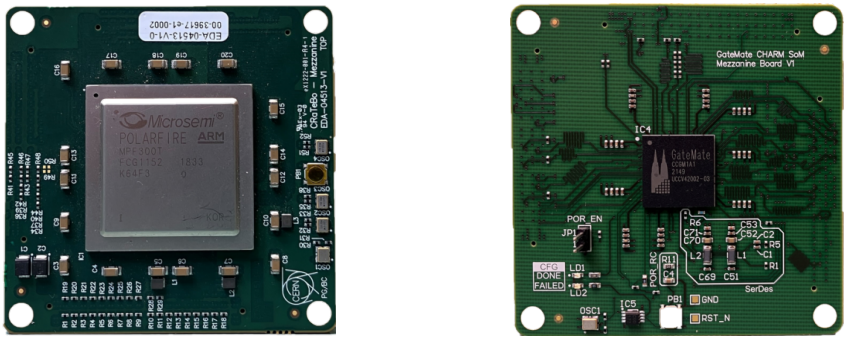
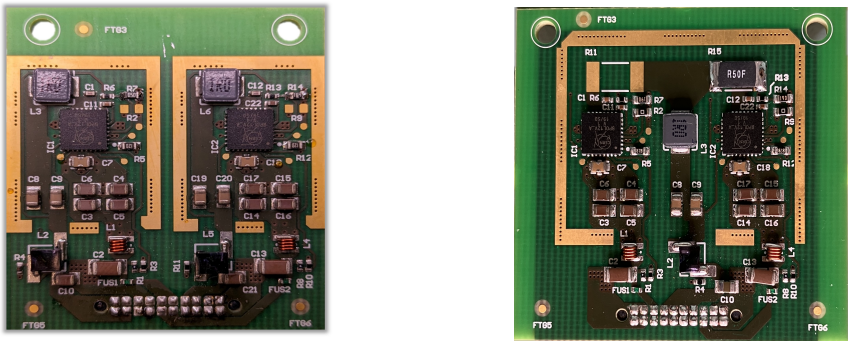


(a) PolarFire SOM (b) GateMate SOM

Figure 2. SOMs FPGA developed for CRaTeBo.



(a) Single power module (b) Parallel power module

Figure 3. Two power modules developed for the CRaTeBo.

2.4 Power supply

The board features a flexible power scheme that can be adapted to the voltage requirements of the system under test. It uses interchangeable radiation-tolerant power modules visible in figure 3. The modules come with either the BPOL12 radiation-hardened DCDC converter developed at CERN [11], (up to 500 kGy of TID and a DD of 1.2×10^{15} 1 MeV neutron equivalents/cm^2), or with radiation-qualified Commercial Off-The-Shelf (COTS) components, tested up to 1 kGy. In the latter case, the modules can be replaced before reaching their TID threshold. The power modules come in two configurations, with a parallel or a single output respectively. The first can drive more current. Therefore, it supplies the FPGA core, considering that some FPGA application may be more demanding in terms of current consumption. The latter supplies the remaining peripherals. The board features two independent 12V inputs, for the carrier and the FMC respectively. Decoupling the two supplies prevents potential radiation-induced destructive events on the mezzanine card from propagating to the carrier board. Figure 4 shows a diagram of the CRaTeBo power scheme.

2.5 Slow Control Adapter

CRaTeBo mounts the Slow Control Adapter (SCA) [12], an integrated circuit developed at CERN as part of the GBT chip-set for distributing control and monitoring signals to front-end electronics. It

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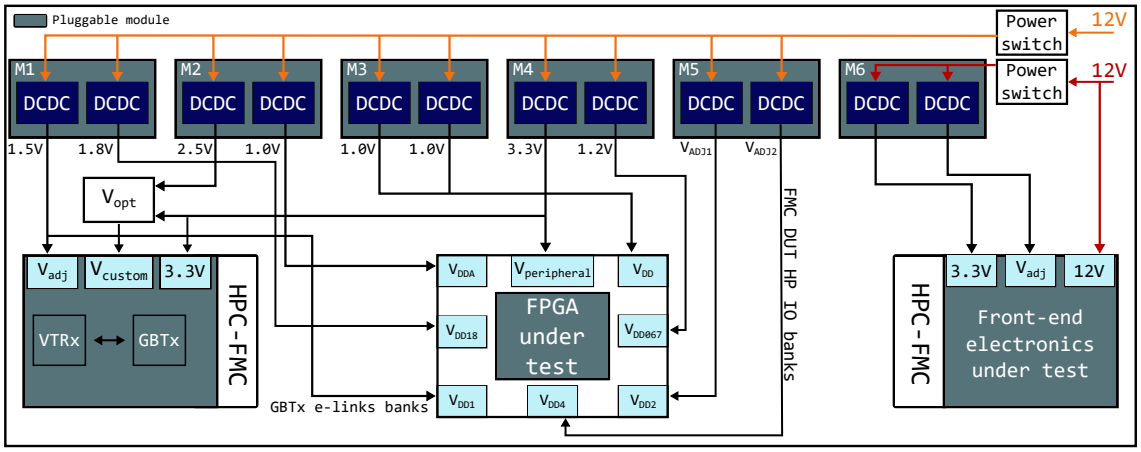

Figure 4. CRaTeBo Power supply scheme.

is designed according to radiation-tolerant design techniques providing robustness against SEE and TID (up to 1 MGy). The SCA is connected to a dedicated port on the GBTx ASIC through e-links. It embeds a JTAG master connected to the SOM. Therefore, it enables the user to program the DUT through the radiation tolerant GBT/Versatile link. It also embeds an I2C interface to the DUT on the FMC and a 12-bit ADC monitoring the on-board voltages.

2.6 JTAG configuration

The JTAG chain can be configured using a set of jumpers to obtain the desired programming chain. In particular, two sources are available for selection: the on-board 10-pin JTAG connector and the JTAG master on the GBT-SCA. The first, is useful for debugging/development purposes outside of the radiation environment, where standard JTAG programmers can be used. On the other hand, selecting the GBT-SCA allows the configuration of the DUTs through the Versatile optical link, which is essential when programming the device when it is exposed to radiation. Both sources can be used to program either the FPGA on the SOM or the front-end electronics on the FMC connector. Additionally, the FPGA on the SOM can be used as a JTAG master to configure the front-end electronics.

2.7 Other features

In addition to the features described above, CRaTeBo provides an SFP+ connector, 4× user LEDs, 4× switches, and 6× SMA connectors linked to the FPGA. Among the SMA connectors, 4× of them can be used to provide clock signals from external source. The remaining two connectors are compatible with the CERN accelerator triggering signals, based on Transistor-Transistor Logic (TTL). The trigger signal is particularly useful to trigger data acquisition only when necessary. CHARM is a pulsed beam facility, where the particle spill lasts around 300 ms, with an average of two spills per minute. The trigger is synchronized with the spill, therefore it can be used to trigger a data transfer from the DUT to the host-PC, rather than acquiring data continuously. This helps reducing the necessary bandwidth and storage, in particular for high data-rate applications where it would be very high if data were continuously sampled.

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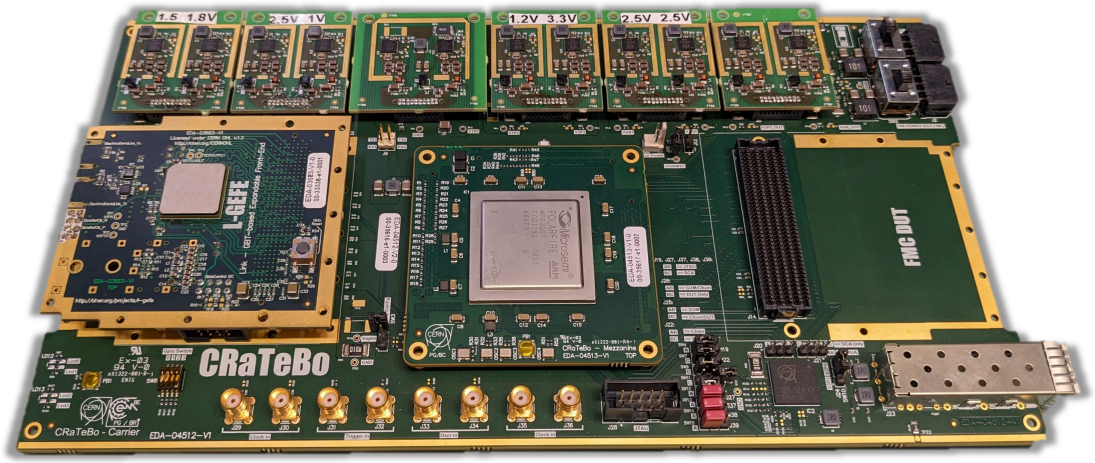

Figure 5. CRaTeBo carrier card with the L-GEFE module, power modules and PolarFire SOM.

3 Irradiation test setup

CRaTeBo will be permanently installed in the CHARM facility at CERN, offering the users a testing platform to carry out their experiments. In CHARM, the radiation environment replicates the one present in the LHC tunnel, where the High-Energy Hadrons (HEH), with an energy above 20 MeV, are the main responsible for Single Event Effects (SEE). The facility is available five days per week for eight months. The permanent installation of CRaTeBo would significantly increase the testing time, which is now limited by the impossibility of using commercial development kits, requiring more time for developing radiation-tolerant cards. The board, shown in figure 5, is installed in the experimental area in position G0, one of the 13 positions available for radiation testing in the facility. In this location, the DUTs are subject to roughly 30 Gy/week and to a HEH fluence of roughly 9.75×10^{10} p/cm^2/week. Considering the radiation levels expected in the LHC locations during the HL-LHC [13], in particular the shielded areas, testing in G0 for 1 week will be equivalent to $\sim$ 20 years of operation in UJ, which is the average life time of a system installed in the LHC tunnel. In addition, CRaTeBo could also be placed in other positions in CHARM, such as G16, where it will be exposed to a HEH fluence of 5×10^{11} p/cm^2/week, which corresponds to a HEH fluence of 2×10^{13} p/cm^2/year. Moreover, multiple boards could be installed in the test position during the year, allowing testing more systems or collecting more statistics. Given the available features, CRaTeBo can be used in different configurations to carry out radiation testing of a variety of FPGA-based systems, spanning from stand-alone FPGAs to more complex systems such as wireless applications.

Figure 6 shows a schematic representation of the full setup architecture. CRaTeBo, installed in the experimental area, hosts the FPGA under test and the eventual analog/mixed electronic on the mezzanine card. The L-GEFE enables communication between the experimental area and the control room through the Versatile Link. The two areas are connected with $\sim$ 40 meters of cables accessible through patch-panels. In the control room, the AMD Virtex-7 FPGA VC709 board is

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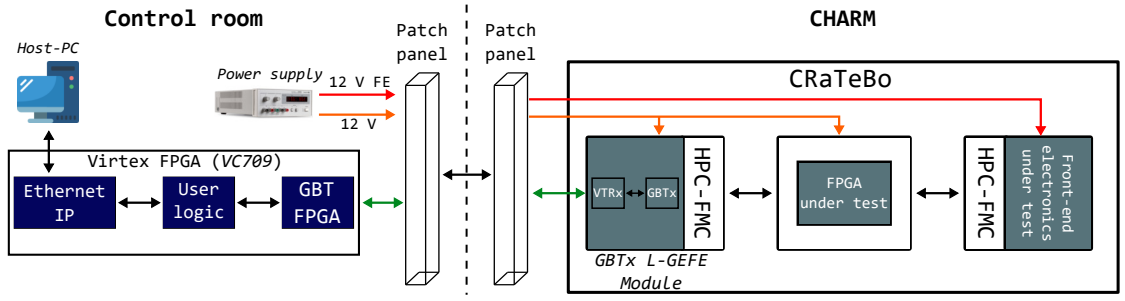

Figure 6. Test setup for a radiation test of a system relying on the GBT/Versatile Link.

installed. It mounts a Virtex-7 FPGA implementing the GBT-FPGA core, enabling communication with the GBT protocol with the system under test. Depending on the user needs, it can also embed additional user logic necessary for the experiments. The VC709 is connected to an host-PC through a 1 Gb/s Ethernet interface, but if a higher data rate is necessary, PCI-Express can be used instead. The interface between the host-PC and the VC709 is still under development, therefore no tests have been performed yet using this configuration. Nonetheless, tests are foreseen in the near future. An example use case for such configuration could be the testing of WorldFIP based application. WorldFIP is a fieldbus network protocol that implements real-time distributed control. At CERN, it is used to control and monitor instruments all around the LHC tunnel. An FMC-compatible WorldFIP card [14] was developed to ease the test of equipment before it is installed, and Front-End Computers (FEC) at CERN are prepared to carry out such tests. Thanks to CRaTeBo, users will be able to test their WorldFIP-based application in a radiation environment representative of the LHC tunnel with minimum effort on the test setup development.

4 Alternative test setups

Even though the main goal of the board is to ease radiation testing in CHARM, CRaTeBo finds application also in other facilities. When performing radiation testing, focused beam is the preferred option to prevent interaction with the card and avoid generation of secondary particles. However, there is still the chance of observing destructive Single-Event Latch-Up (SEL) from surrounding components because the collimation is not fully effective outside of the beam area. In addition, there are also facilities where the beam size is bigger than the DUT size. In these occasions, CRaTeBo greatly simplifies the test process, as shown in the following experiments where the board been used to carry out radiation tests of various systems in other irradiation test facilities.

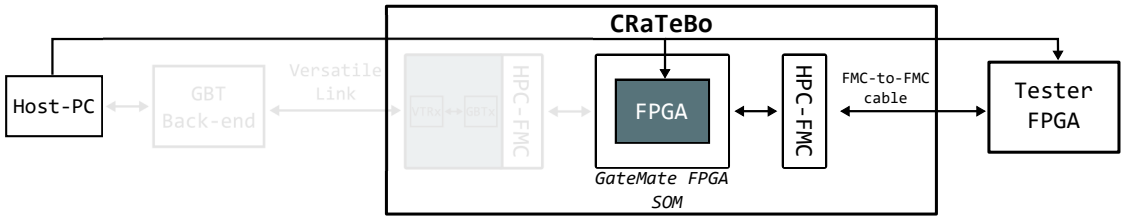

Figure 7. Test setup for FPGA testing.

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Figure 7 showcases the configuration used to carry out a TID test on the GateMate FPGA, an SRAM-based FPGA from CologneChip. The SOM and the related test are part of a collaboration with the Fachhochschule Dortmund University. Being interested only in the TID effects, the test was carried out in the Cobalt-60 (CC60) facility at CERN. Since the target dose was in the order of kGy, using a commercial development board to perform the test would have been challenging. Firstly, shielding is not always easy, given that the FPGA is usually in the center and surrounded by peripherals. In addition to that, when testing at a high dose rate to save time, the DUT is closer to the source, making it even more difficult to shield in the space available. Secondly, even if shielding is applied, the residual dose could still be high enough to induce significant degradation in commercial components. For these reasons, the experiment was carried out using CRaTeBo. The test consisted in measuring the frequency of multiple ring oscillators implemented in the FPGA under radiation to retrieve the propagation delay variation with the dose. This is useful to estimate the timing margins to take into account when designing an FPGA application targeting radiation environments. Thus, CRaTeBo hosted the GateMate SOM on which the ring oscillators were implemented. Their outputs were connected to the HPC-FMC connector and connected to a Tester FPGA, not exposed to radiation, through a 1.5 meters FMC-to-FMC cable. The Tester read the frequency of the ring oscillators and reported it to the Host-PC through an Ethernet interface. In this case, the GBT/Versatile link was not employed because the test was carried out using an home-made test procedure based on PYNQ [15], which allows to minimize the test logic in the FPGA under test to get more reliable results. Prior to irradiation, the oscillation frequency of each ring oscillator was measured through the PYNQ tester board. Then, the DUT was irradiated for three days while measuring the ring oscillators' frequency. The board accumulated a total dose of 9 kGy. Knowing the number of logic element composing a ring oscillator, the propagation delay variation can be retrieved by comparing the measured frequency with the one prior to irradiation. The complete results analysis are reported in [16]. The GateMte exhibited a maximum delay variation of 8% at around 4 kGy, which then started decreasing reaching 6% at 9 kGy. It has to be noted that it would have been challenging to perform the test using the GateMate development kit, since it would have been exposed to a significant amount of dose that the voltage regulators could not whitstand. As already mentioned, even by applying shielding, the residual dose absorbed by the regulators would be still high considering that 9 kGy were reached.

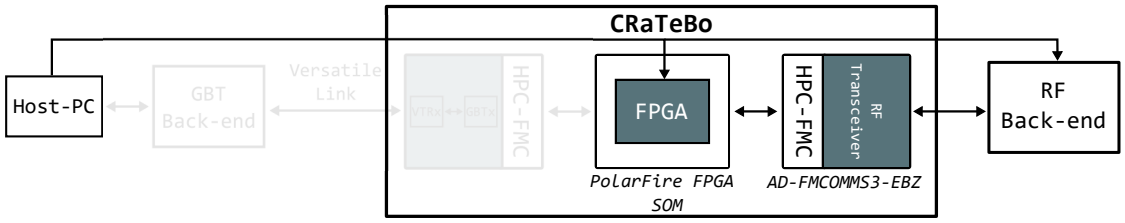

Figure 8. Test setup for radiation testing of a Software-Defined Radio.

Figure 8 shows instead the setup for the radiation test of a Software-Defined Radio (SDR), a wireless platform made of a Radio Frequency (RF) front-end combined with an FPGA. Such test was carried out at the TNF facility in TRIUMF, Canada's particle accelerator [17]. The SDR under test comprises the PolarFire FPGA mounted as a SOM, and the AD9361 Agile RF Transceiver [18] mounted on the HPC-FMC slot. The first is a flash-based FPGA, the latter is a RF front-end fully configurable in

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bandwidth (up to 56 MHz), gain, frequency (60 MHz–6 GHz). At TNF, the irradiated area is 5×12 cm, much bigger than the DUT size. Therefore, on commercial boards the peripherals surrounding the FPGA would have been irradiated, thus the test was carried out using CRaTeBo. The main objective of this test was the evaluation of complex failure rate, like radiation-induced resets of the system or Single-Event Functional Interrupt (SEFI). Since the irradiated area was much bigger than the DUT size, using CRaTeBo it was possible to suppress external sources of problems such as FPGA restarts due to resets of voltage regulators or other peripherals. Moreover, the AD9361 was tested using the AD-FMCOMMS3-EBZ evaluation board [19], that is not radiation tolerant. However, on CRaTeBo the supplies of the carrier and the FMC slot are decoupled, therefore potential destructive events would have not propagated to the carrier card. For this reason, it was not necessary to develop an ad-hoc radiation tolerant FMC module to host the AD9361 which would have increased the time and the cost to perform the radiation test. The application under test consisted of a packet-based transmission based on Pulse Position Modulation (PPM) at 1 Mb/s. The PolarFire FPGA implemented the processing algorithms for packets generation, modulation and filtering, and it interfaced with the AD9361 for the RF conversion. A second SDR, working as a receiver, was installed in the control room and used to monitor the availability of the transmission link under irradiation. Given the low data-rate of the application, it was not necessary to use the GBT/Versatile link, and a UART communication was used instead.

5 Conclusions

Radiation testing of FPGA-based systems is a challenging task, especially in those facilities where the beam size is bigger than the DUT, or in facilities such as CHARM, where the whole device is irradiated. In this case, the use of commercial modules is not recommended, thus requiring the development of a radiation tolerant setup. CRaTeBo was developed to address this challenge by providing a radiation tolerant carrier card with a communication interface, a flexible power scheme, and multiple DUT interfaces. The communication interface is based on the GBT/Versatile link implemented through the GBTx radiation-hardened ASIC developed at CERN, and the VTRx radiation tolerant transceiver. A custom SOM socket is available for interfacing the FPGA under test, and an additional HPC-FMC connector enables testing of front-end electronics. Power is supplied through interchangeable power modules built with radiation-hardened DCDC converters (bPOL12V), or radiation-qualified COTS. Thanks to its features, CRaTeBo can be adapted to test a large variety of FPGA-based systems, such as FPGA qualification or wireless applications. Its effectiveness has been already demonstrated with two irradiation campaigns carried out in two facilities were the use of commercial development kit was not straightforward, i.e. CC60 at CERN, and TNF at TRIUMF. Once the Host-PC interface is ready, CRaTeBo will become a permanent installation in the CHARM facility at CERN. Moreover, it will be advertised and offered to CERN users as a service, giving them the opportunity to test their systems in a radiation environment representative of the LHC, minimizing development time and costs.

Acknowledgments

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