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HL-LHC BPM ELECTRONICS DEVELOPMENT AS A CASE STUDY FOR DIRECT DIGITIZATION AND INTEGRATED PROCESSING TECHNIQUES IN ACCELERATOR INSTRUMENTATION

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Abstract

The technological evolution of analog-to-digital and digital-to-analog converters increases the amount of data that can be processed in the digital domain. Therefore, direct digitization enables many advanced signal processing techniques and is attracting more and more attention in the field of accelerator instrumentation. The future HL-LHC Beam Position Monitor (BPM) data acquisition system to be installed near the ATLAS and CMS experiments is a clear example of an application with demanding signal processing requirements that could greatly benefit from this trend. The investigated architecture is based on an RF System-on-Chip from Xilinx, which allows fast RF conversion and high-performance digital processing to be integrated in a single chip for multiple channels. This paper compares the estimated performance and cost of such an integrated solution with an architecture based on discrete components.

INTRODUCTION

The state-of-the-art of Analog-to-Digital Converters (ADC) is continuously evolving, providing converters with better resolutions and higher sampling rates. To compare different components when power dissipation is not a key metric, a valuable figure of merit is the performance P defined as a product of the effective number of logical levels – a function of the Effective Number Of Bits (ENOB) – and the maximum sampling rate f_s [1]:

$$P = 2^{\mathrm{ENOB}} \cdot f_s \tag{1}$$

The evolution of P [2] demonstrates how the performance of ADCs has improved since the nineties, especially in the mid-high sampling rate range of gigasamples per second. These days high-resolution high-sampling-rate ADCs are not only widely available, but also their performance P is among the best across all ADC families.

As a consequence, direct digitization of broadband signals, that is the minimization of the analog-conditioning hardware and the placing of the digitization stage early in the processing chain, paired with sophisticated digital signal processing, has become technically possible and economically attractive. This trend is also present in the field of particle beam instrumentation, in particular in the domain of Beam Position Monitors (BPM).

Direct digitization of broadband BPM signals is a viable solution for measuring positions of individual bunches in the Large Hadron Collider (LHC) at CERN [3] and it opens the door to more advanced digital signal processing which is often not feasible in the analog domain.

The simplification of the analog processing chain comes at the cost of more complex digital electronics. Direct digitization requires interfacing advanced fast ADCs and laying out high-speed serial lanes to the processing logic, typically a Field Programmable Gate Array (FPGA). The technical complexity is even higher for systems acquiring several high-speed channels, that must be handled by a single processing element.

When having a distributed acquisition chain is not a requirement (e.g., acquisition systems that are not exposed to radiation), and when there is a high density of high-frequency signals which need to be processed simultaneously, it is worth investigating the use of integrated solutions such as the RF-System-on-Chip (RFSoC) [4, 5]. This technology integrates several state-of-the-art RF data converters with high-performance resources for digital signal processing in a single integrated circuit and is being explored by the beam instrumentation community [6–9].

CERN is currently studying the feasibility of using the RFSoC, or a similar technology, as a base for the new BPM system which is being designed for the High-Luminosity upgrade of the LHC (HL-LHC). It is an example of a system installed in a radiation-free area which requires the digitization of multiple broadband signals and advanced bunch-by-bunch processing.

HL-LHC BPM ELECTRONICS

The new HL-LHC BPM system will include 24 directional-coupler (stripline) pick-ups that will be installed near the ATLAS and CMS experiments where both counter-rotating beams exist in a common vacuum chamber [10, 11]. To distinguish each beam independently, a directional-coupler pick-up features four long stripline electrodes, as shown in Fig. 1. The striplines are designed such that a passing beam generates a large bipolar impulse on its upstream port with only a small residual impulse generated on the downstream port. Therefore, the signal generated on each of the 8 BPM ports is a combination of a large signal induced by one beam and a residual signal excited by the other beam. Reconstruction of the beam position in a given measurement plane is possible by comparing the power of signals induced by that beam on the BPM electrodes installed in that plane.

As both beams arrive at the BPM location within a time comparable to the output impulse duration, the signals induced by individual beams overlap significantly causing a measurement error. The challenging accuracy requirements

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defined in the HL-LHC BPM system specification [12] require that this error is corrected.

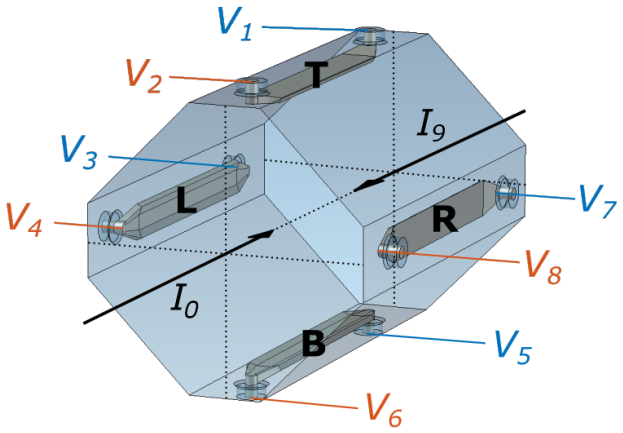

Figure 1: Model of a directional coupler BPM with four striplines – top (T), bottom (B), left (L) and right (R) – and eight ports numbered 1–8. The two counter rotating beams are represented by the two arrows, I_0 and I_9. The even-numbered ports in red are upstream for beam I_0, and the odd-numbered ports in blue are upstream for beam I_9.

Signal Processing Requirements

Various data processing techniques have been studied to develop an algorithm which would reduce the error caused by the counter-propagating beam [13, 14]. The proposed solution along with the system performance specification [12] define the set of requirements for the signal acquisition and processing electronics.

First of all, the algorithm relies on fast digitization of the eight stripline signals on a bunch-by-bunch basis. The power of each impulse is computed numerically. Previous publications have shown that for LHC stripline BPMs, similar to the HL-LHC BPMs, achieving beam position measurement resolution in the order of micrometers requires sampling rates reaching a few gigasamples per second with an ENOB between 9 and 10 [3].

Secondly, the developed counter-beam compensation algorithm is applied to each of the 8 BPM signals and uses coefficients derived from the signals of the remaining ports [15]. Hence, all acquired signals must be processed in parallel with processing results being exchanged in real time. Therefore, the eight signals from a BPM should be processed within the same logic device.

In addition, the power computation and the counter-beam compensation algorithm make significant use of multiplications, divisions and square roots. The chosen logic device should feature sufficient resources, i.e., look-up tables (LUT), flips-flops (FF) and digital signal processors (DSP), to implement this foreseen demanding digital signal processing.

Also the amount of internal and external memory as well as the bandwidth at which it can be accessed and read out must be compatible with the various acquisition modes defined in the specifications [12].

Finally, to achieve the required measurement stability, it is foreseen to periodically calibrate the gain of each of the eight channels. The system should therefore be equipped with one Digital-to-Analog Converter (DAC) per port to generate controlled calibration signals.

The resources available in the first generation of the RFSoC (RFSoC Gen1) were estimated to be sufficient to implement an early version of the processing algorithm in 2021 [14]. Table 1 lists the resources required to process a BPM (eight ports) based on the current system specification; the resources needed to acquire the data from 8 ADCs sampling at 5 GSps are accounted for, based on the measurement of the resources needed for an acquisition gateware using the evaluation board ZCU208 [16], equipped with a third generation RFSoC (RFSoC Gen3).

Table 1: Summary of the estimated amount of resources required to process the raw ADC data, compute the signal power and compensate the counter-beam power on a bunch-by-bunch basis for eight BPM ports, together with other operations required by the specifications [12]. DACs are listed for calibration but no calibration logic was accounted for. The calculated Double Data Rate (DDR) memory maximum bandwidth (BW) corresponds to continuously acquiring all bunches at each revolution. The estimated read-out bandwidth allows the back-end to continuously read all available data at the maximum specified rate. The third column lists the equivalent percentage of the resources of the RFSoC Gen3 equipped with a 4 GB DDR4 memory, assuming for the read-out an Ethernet protocol over a 1000 Mbps link running at 50% efficiency.

Resources	Required qty.	%RFSoC
ADCs	8	100
DACs	8	100
Internal memory	30 Mb	48
DSP	172	4
LUT	20521	5
FF	50644	6
DDR	768 Mb	3
DDR WR peak BW	22 Gbps	24
Read-out BW	54 Mbps	10

ARCHITECTURE STUDY

Although the RFSoC Gen3 meets the system's requirements, it should also be scrutinized against a different system architecture based on discrete components in terms of performance and cost.

ADC Survey

One of the critical components defining the system's performance is the ADC. Figure 2 summarizes the results of an ADC survey which compiled the resolution and maximum

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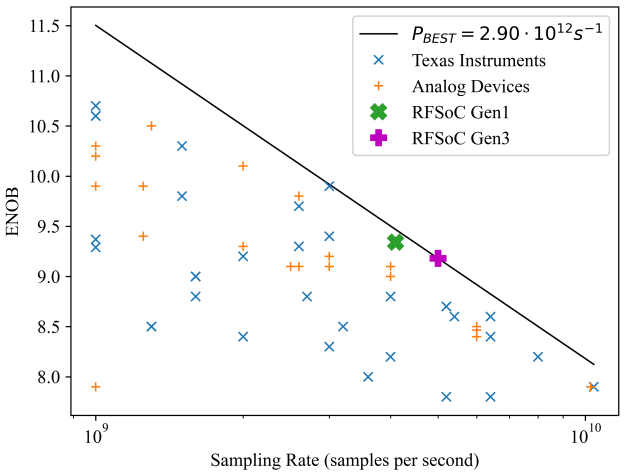

Figure 2: Plot of the ADC resolution (ENOB) versus its maximum sampling rate. The survey covers two generations of the RFSoC and the commercially available components from Texas Instruments and Analog Devices with a sampling rate exceeding 1 GSps and a resolution above 7.5 ENOB. The resolution was extracted from datasheets [17, 18] for an input frequency as close as possible to the half of the maximum sampling rate.

sampling rate of a population of commercially-available converters with a sampling rate exceeding 1 GSps and an ENOB greater than 7.5. The solid line corresponds to the maximum identified value of performance P (see Eq. 1) which was observed for the RFSoC Gen3. For the remaining ADCs, the closer the marker of an ADC is to the solid line, the better the ADC's performance is.

The component closest in performance P to the RFSoC Gen3 is the Texas Instruments ADC32RF55, a dual-channel ADC with a sampling rate of 3 GSps and an ENOB of 9.9. Hence, a discrete-component solution using this ADC will be compared to an RFSoC-based acquisition system.

Discrete Components Implementation

In addition to eight ADC channels, an HL-LHC BPM acquisition requires an equal number of DACs for calibration. For this exercise, Texas Instruments DAC38RF97 was selected as a suitable component.

Given the required resources laid out in Table 1 and the number of transceivers needed to interface the sixteen converters (96), a suitable FPGA candidate is the Altera Intel 10AX115. Table 2 lists indicative prices for all mentioned Integrated Circuits (IC).

Table 2: Indicative prices for small quantities of ICs found online [19]. ADC – Texas Instruments ADC32RF55; DAC – Texas Instruments DAC38RF97; FPGA – Altera 10AX115; RFSoC – Xilinx XCZU47DR.

IC	ADC	DAC	FPGA	RFSoC
k$	1.9	0.1	10	20.3

Comparison

Table 3 lists the total price of the ICs for each of the two architectures, showing them to be comparable, with the RFSoC being about 10% more expensive.

Table 3: Total IC cost for the two system architectures.

Arch.	Discrete	RFSoC
IC cost (k$)	18.0	20.3
IC count	9	1

The price estimation does not include the cost of designing the board and implementing all needed interfaces. The RFSoC-based architecture counts significantly fewer ICs requiring less PCB area, less power dissipation and fewer high-speed lanes. It is worth mentioning also the availability of processing cores in the RFSoC, which can potentially ease the implementation of slow control and the communication with the back-end.

A point in favour of the discrete component architecture is the availability of comparable ICs from different vendors. The RFSoC is currently produced and distributed as an off-the-shelf component by a single company. A similar technology is proposed by a competitor company, Intel, though not as an off-the-shelf component [20].

CONCLUSIONS

Direct digitization of broadband signals is becoming technically possible and economically attractive thanks to the evolution of ADCs sampling at several gigasamples per second. Components such as the RFSoC provide an integrated platform for direct digitization, drastically cutting down the number of ICs and interfaces, especially for multi-channel systems. Through the case-study of the HL-LHC BPM acquisition electronics we have compared the estimated cost and performance of a system based on the RFSoC with one based on discrete components. Performance wise, a market-wide survey concluded the RFSoC features one of the best commercially available ADCs in its market segment. Cost wise, both solutions appear to be comparable, with the RFSoC being about 10% pricier which is well within the final price uncertainty. Moreover, the cost for additional components and the board design and production, likely to be lower for the RFSoC, was not taken into account. Nevertheless, a major drawback of the RFSoC solution is vendor lock-in as currently there is only a single supplier providing such a solution off the shelf. The risk concerning the long-term availability of the RFSoC technology appears to be extremely low though, given the historical reliability of the supplier, the rising of competing products and the targeted applications, i.e., telecommunications and satellites.

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