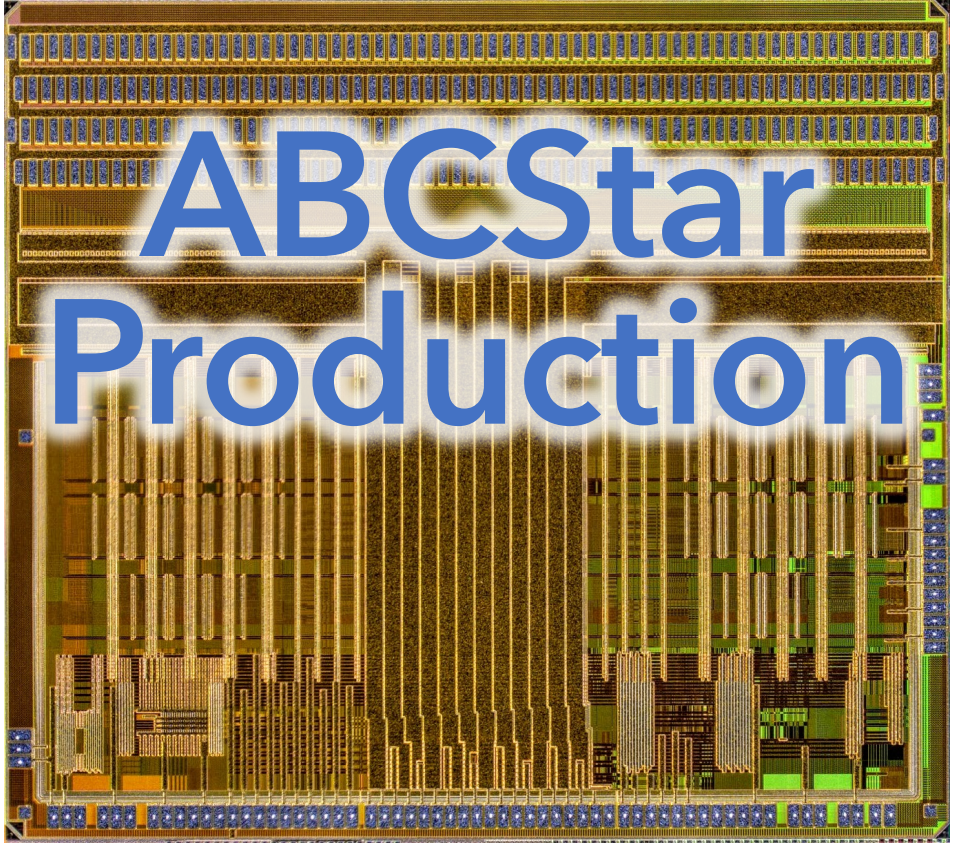


Jaya John John

on behalf of the ATLAS Inner Tracker (ITk) Strip ASICs community

13th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD13)

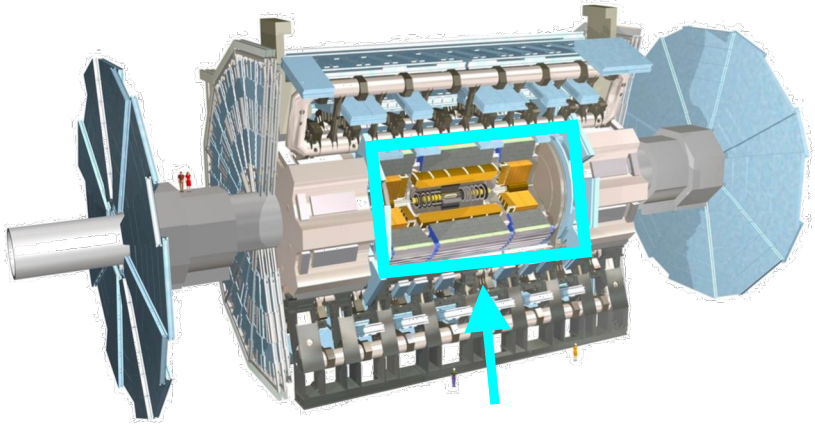
Vancouver, 6 December 2023

UNIVERSITY OF OXFORD

ATLAS ITk

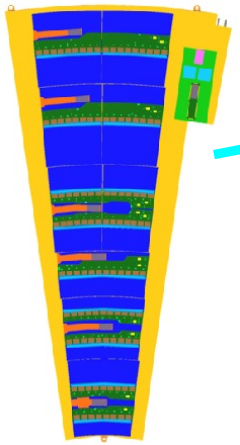
ABCStar within the ITk Strip detector

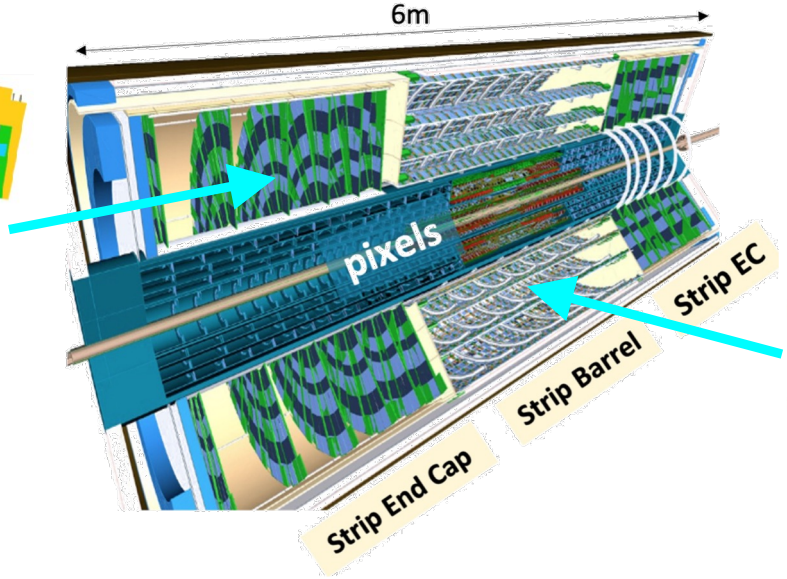
A Toroidal LHC ApparatuS



Inner Tracker (ITk)

Petal



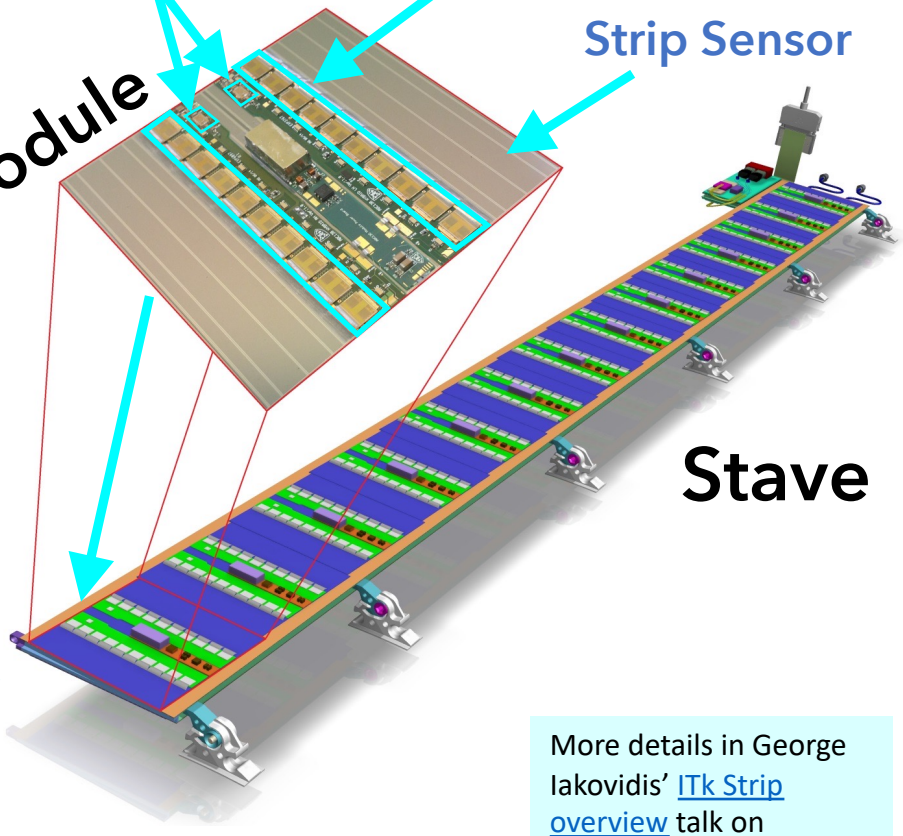


HCCStar
(Hybrid Controller Chip)
Reads and controls
up to 11 ABCStars

ABCStar
(ATLAS Binary Chip)
Front end readout chip

Strip Sensor

Module

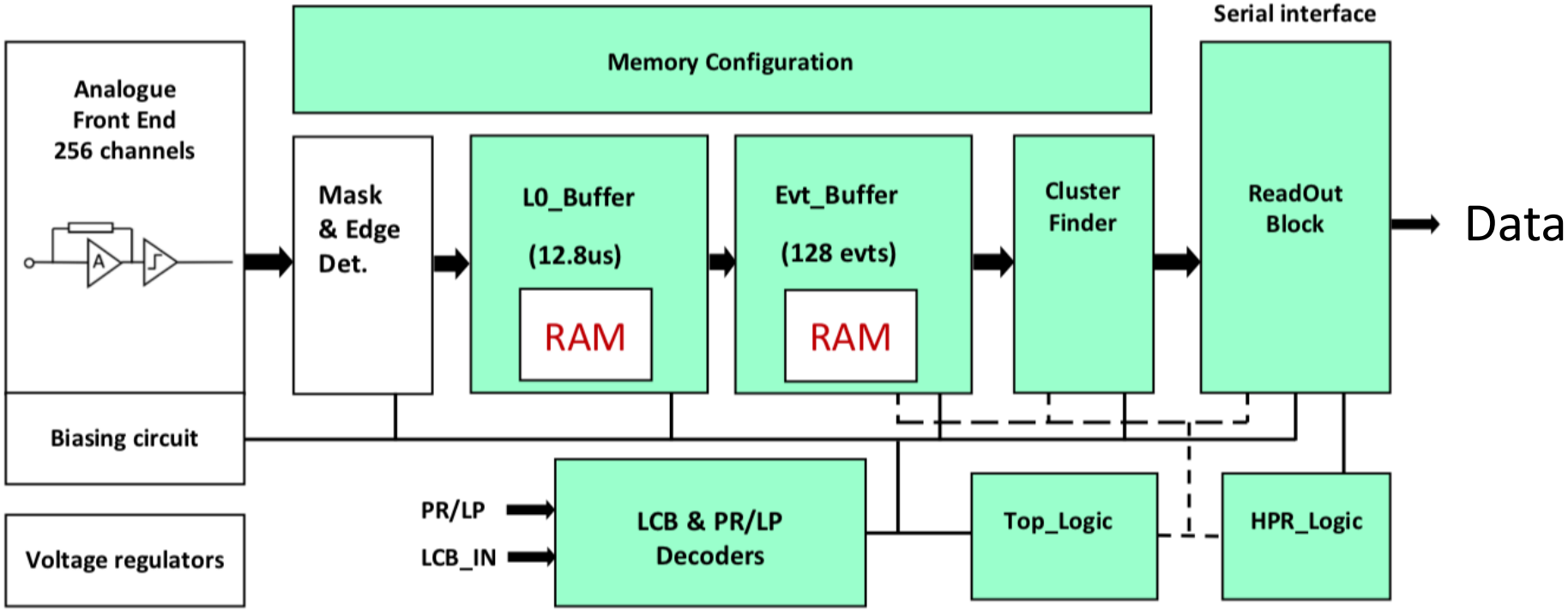


Stave

More details in George Iakovidis' ITk Strip overview talk on Monday

ABCStar front end readout chip

The ABCStar reads ITk silicon strip sensors.
It applies thresholds, digitizes signals, then stores them in memory pipelines. It outputs those hits chosen by system triggers.



Production flow

Manufacture → Probe → Dice → Pre-irradiate → Distribute

Silicon wafers of chips are manufactured by the foundry in lots of 25 wafers.

Batch size: 25 wafers
Delivery: 25-100 wafers

Each chip on each wafer is probed: needles connect to the chip to power and exercise its functions. Chips are graded based on test results.

Batch: 25 wafers (ABC)
15 wafers (HCC+AMAC)

Our dicing vendor thins the wafers down to 300µm, then dices (cuts) the wafer into chips. The chips are placed in special containers: gelpacks.

Batch: 25 wafers (ABC)
15 wafers (HCC+AMAC)

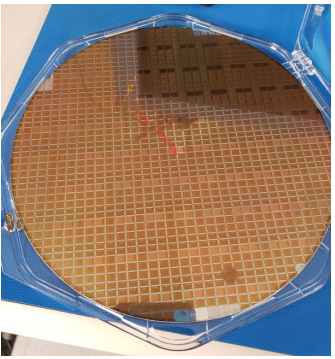
To avoid a peak in current supply, the chips are irradiated using gamma to 5 Mrad.

Batch: varies in time
80 - 150 wafers equivalent

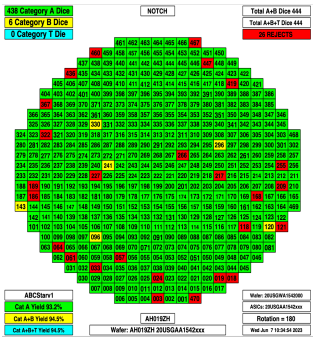
Based on requests from Production Management and Modules co-ordinators, chips are sent to institutes that build hybrids, powerboards and Patch Panel 2 (PP2).

Batch: 3 months of stock, varies by site, see backup slides for details

wafer

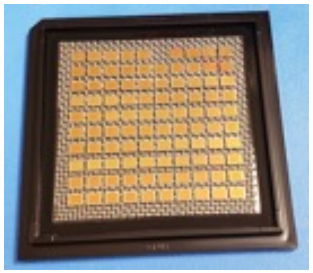


wafer map



Probing is our Quality Control (QC), performed on each chip

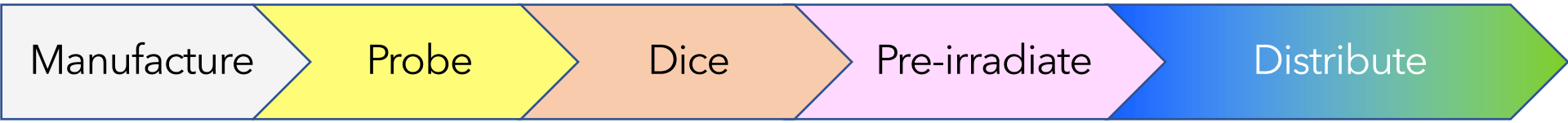
gelpack

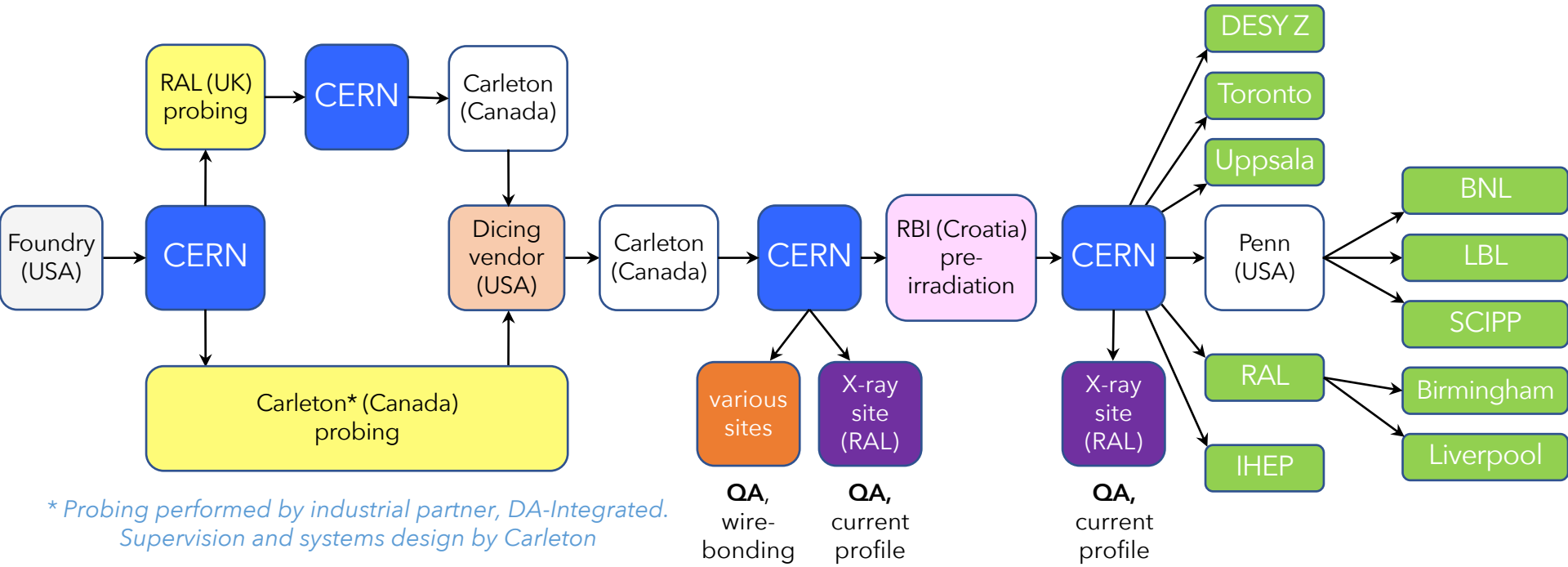


pallet of gelpacks

gelpacks for distribution

Detailed flow





** Probing performed by industrial partner, DA-Integrated. Supervision and systems design by Carleton*

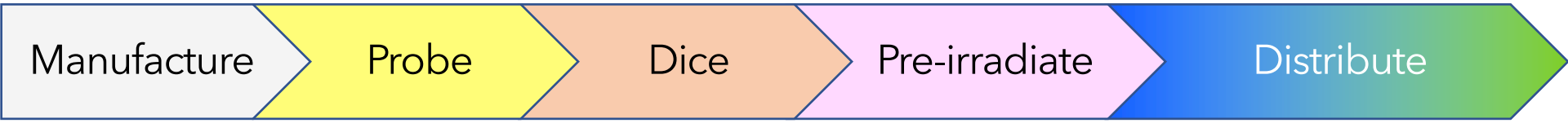
QA = Quality Assurance

Production status

ABCStar chips…	
Needed	311,373
Available at end (est.)	318,147
Spares, estimated	6,774
Spares as % of needed	2.2%

ITk Strip ASICs are deep into production.

Here is the current % complete for each step for ABCStar:



Manufactured	Probed	Diced	Pre-Irradiated	Distributed
94.7%	83.5%	43.3%	35.8%	3.4%

Ready for production

Production probing began in January 2022.

Planned completion dates:

probing:	May 2024
dicing:	June 2024
pre-irradiation:	April 2025

Production should be boring

Production should be boring

Ideally, pre-production allows all issues to be discovered and resolved

then production can be smooth, routine and efficient

nice and boring

2022 was **not** boring for ABCStar

What would you do if you found a chip issue,
one-third of the way through production,
with 250 wafers already delivered, out of 750?

2022 was **not** boring for ABCStar

What would you do if you found a chip issue,
one-third of the way through production,
with 250 wafers already delivered, out of 750?

This is the story of:

- *Finding an issue, deep in production*
- *Investigating it*
- *Mitigating it*
- *…and how future chips might be able to avoid this*

The issue

good
minor flaws
rejected

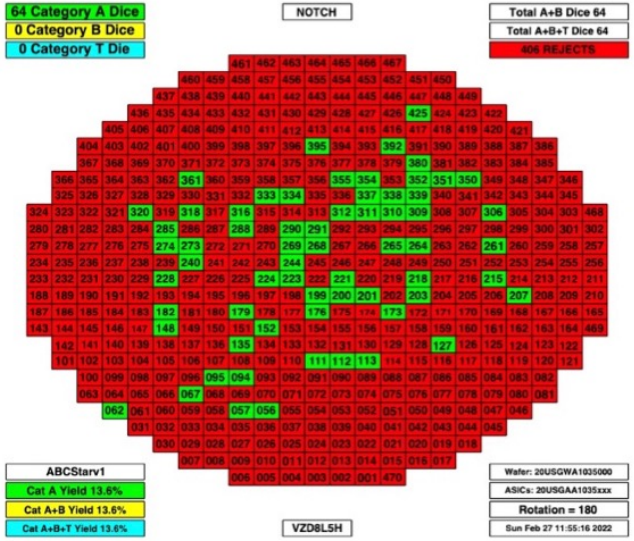
In Jan 2022 – start of Production for ASICs – we began probing a new lot of ABCStar and saw very low yield: **31%** *(vs. average 86%)*

The failures were mismatches in the digital test vectors.

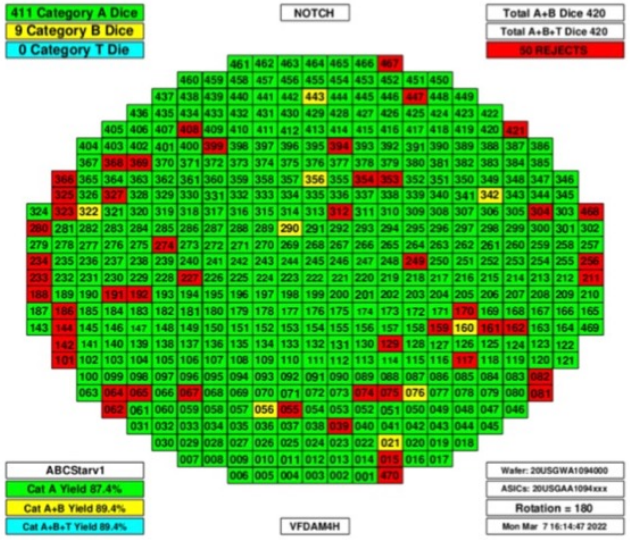
In these digital tests, we:

- "play" a series of inputs from digital chip simulations onto real chip input pads
- capture the real chip outputs
- check that those outputs match the simulation outputs
- **Any** mismatch is a failure

14% yield - from the low yield lot



87% yield - from a 'normal' lot



Initial investigations

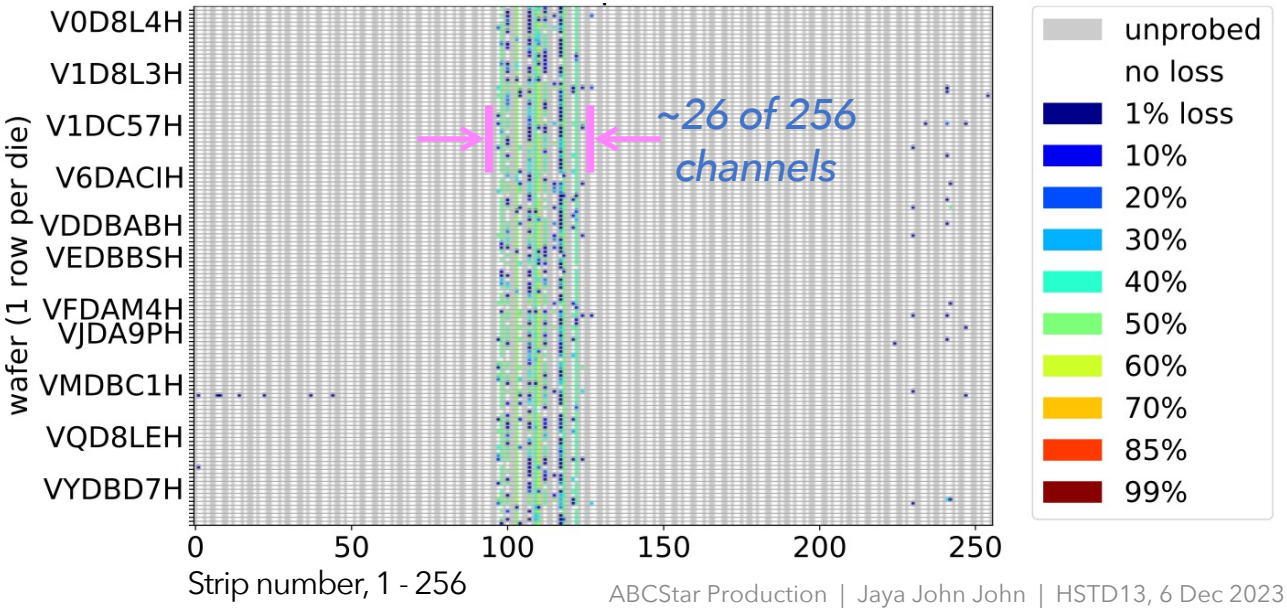
In the chip outputs, expected hits were missing.

The packet outputs from the chips were well formatted ("good grammar").

→ it was the input to the packet builder that had changed.
The ABCStar was losing some hits.

This was not ideal, with 250 wafers out of 750 already delivered.

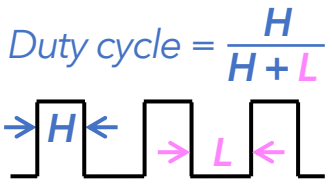
Physical location of hit loss across chip
Hit loss % vs strip number, for 11 wafers



How bad is it?

- Very dependent on foundry lots – most lots not affected much
- ~26 out of 256 channels affected
- Overall % loss is small, depends mainly on lot, see next slide

Outcome of investigations

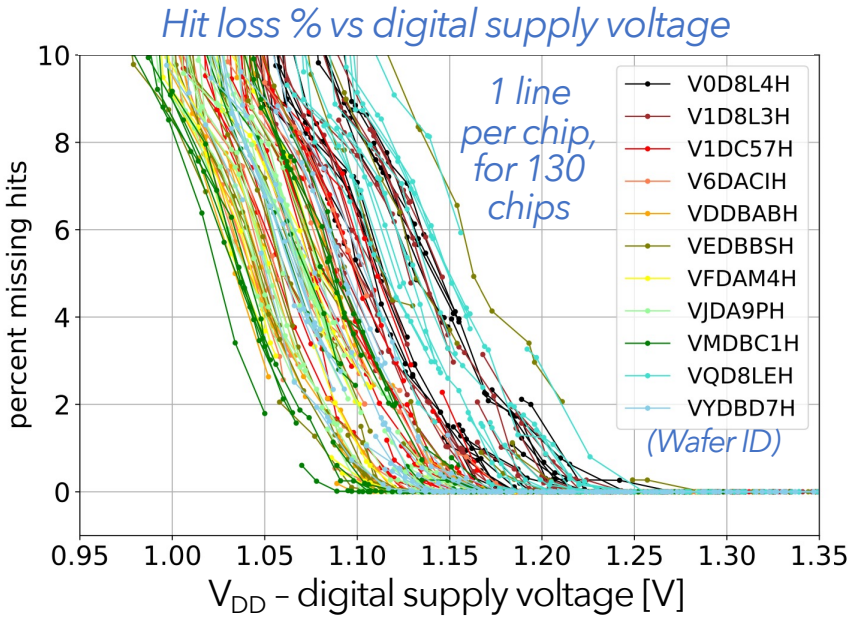


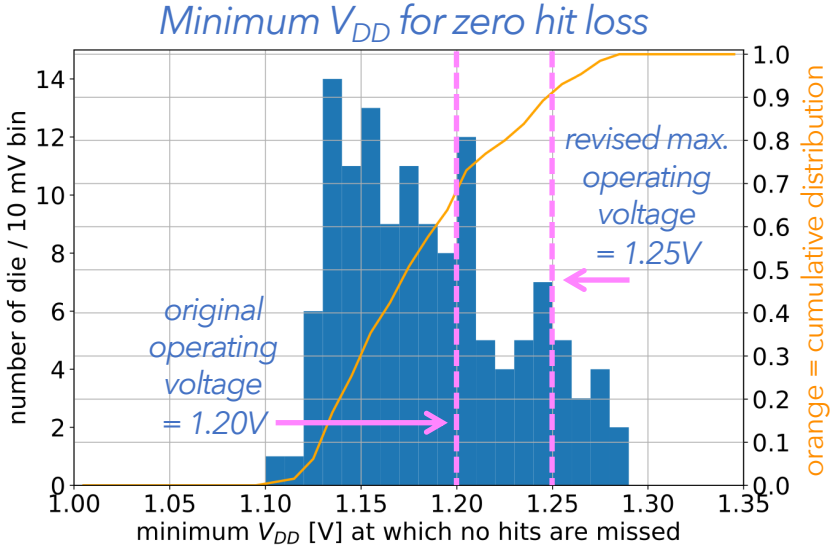
Change / Trend	Effect on hit loss
Increase digital supply voltage (V_{DD} from on-chip regulator)	Reduced, large effect
Decrease clock frequency	Reduced
"Silicon is faster" (on-chip ring oscillator frequency)	Reduced
Increase clock duty cycle	Reduced large effect
Lower temperature	Reduced
Higher irradiation dose	Increased, small effect

cancel

→ all this indicates a setup timing issue, data arriving too late vs. the clock edge used to sample it

→ all changes that make the chip operate faster will help





Foundry investigations

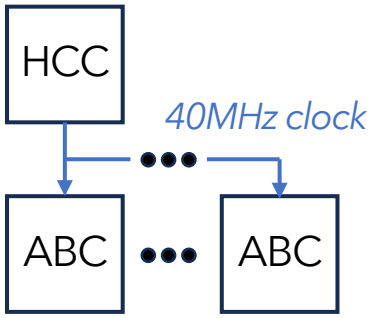
The foundry worked closely with us to establish:

1. There were no manufacturing faults at the foundry
2. By correlating our observed yields for different lots to process records at the foundry, the foundry confirmed that faster transistors alleviate the issue
3. The foundry manufactured experimental wafers using well-known speed increase recipes, as trials to increase the yield for future production wafers.

Unfortunately, while the speed-ups helped with the SRAM issue in isolation, they were overall neutral for yield – due to an increase in analogue failures.

So we decided not to change the wafer recipe.

Solution: higher voltage



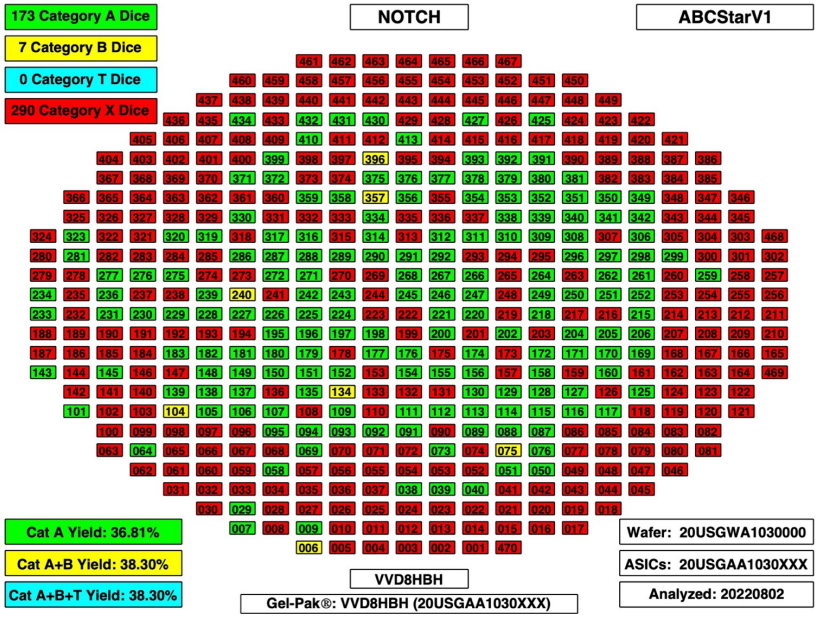
Additional note: we found that the HCCStar supplies a 49% duty cycle to the ABCStar (reminder, 49% is worse than 50%)

Based on available handles, we adopted this mitigation:

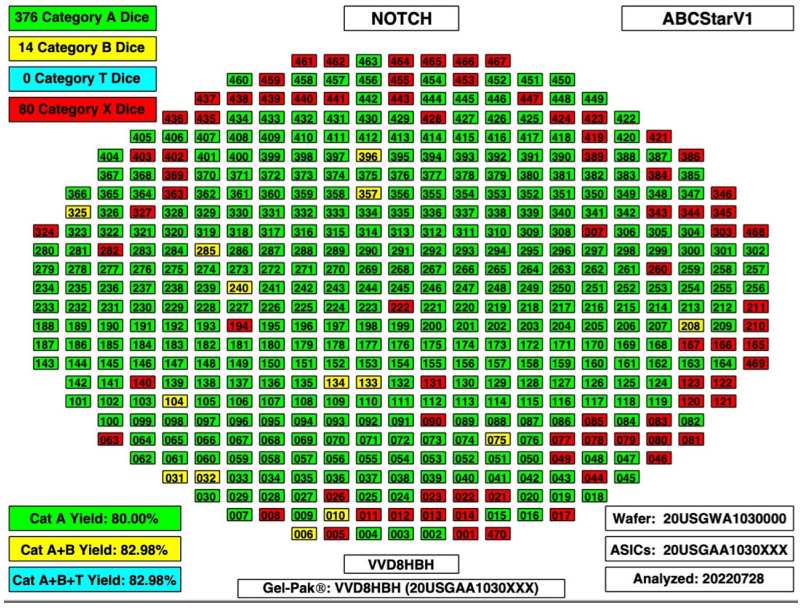
- We increased the on-chip digital voltage regulator setting from 1.20V up to max. 1.25V if needed
- We probed chips using a 49% duty cycle and voltages up to 1.25V.
- Any chip with no hit losses at 49% and VDD <= 1.25V is now seen as good.

A wafer from the lowest-yield lot

Operating at 1.20V – 37% of chips pass



Operating at 1.25V – 80% of chips pass

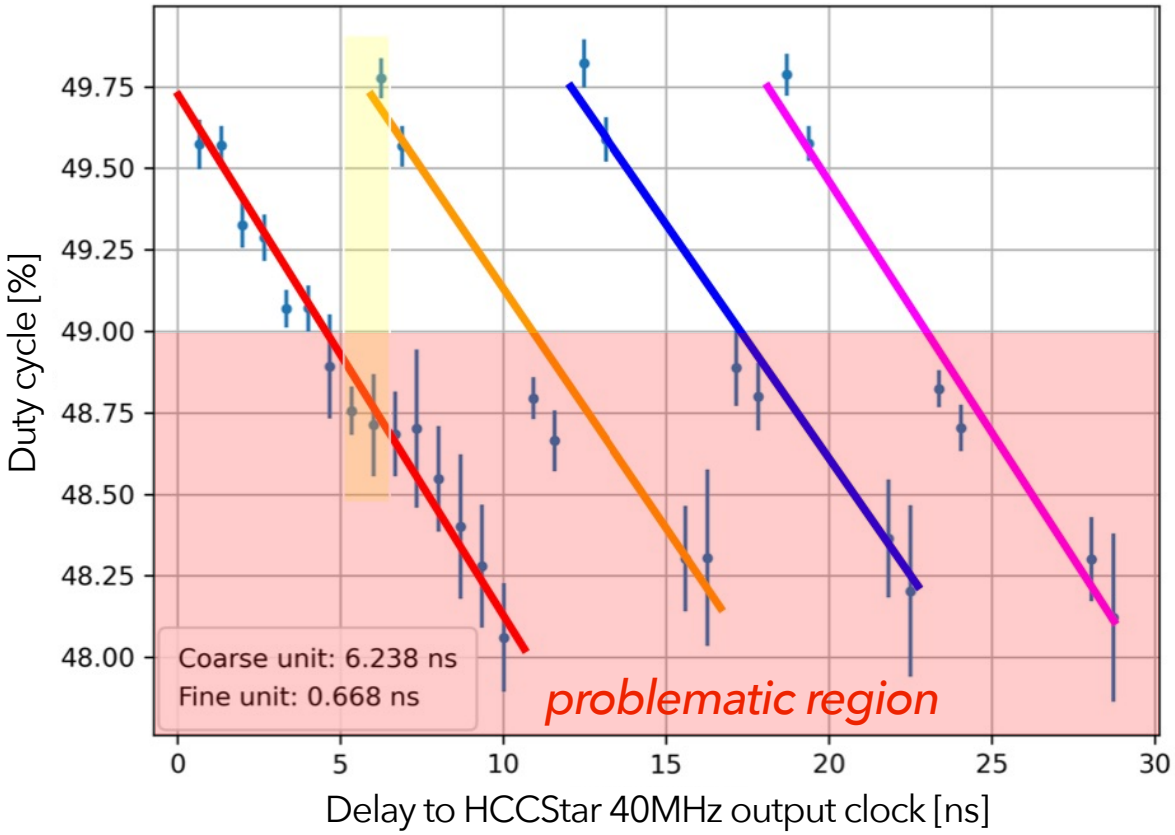


A twist in the tale

Further investigations in spring 2023 showed that in fact the HCCStar duty cycle could go as low as 48%.

→ The thousands of ABCStars already probed using 49% could lose hits in the detector, as things stood.

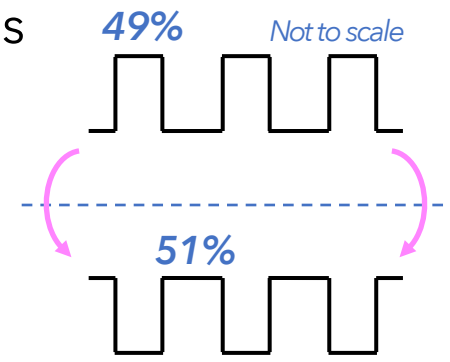
Duty cycle vs. delay of 40MHz clock, for a typical HCCStar, at -20°C



40MHz clock delay settings: 1-15, 16-17, 23-24, 30-31, 32-33, 39-40, 46-47, 48-49, 55-56, 62-63

Solution part 2: clock inversion

A great way to fix a duty cycle issue is to invert the clock. For a differential clock, swap the 2 phases.



Now it was clear: we needed this.

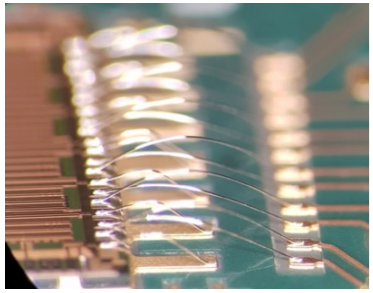
New questions: where in the system to invert and at what cost?

We could not change the chip or hybrid designs, due to cost, timeframe and the number of hybrid designs affected.

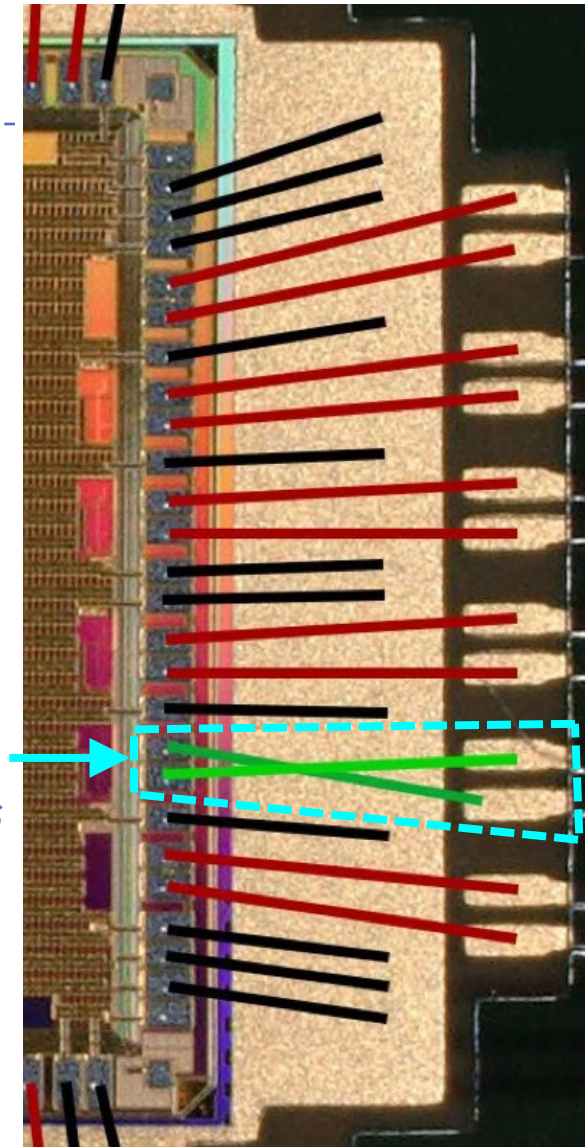
After discussion: crossing the wire-bonds of the clock pair coming out of the HCCStar was the best (least bad) choice.

Thanks to our Modules colleagues.

Crossed bonds



HCCStar bonding diagram



Did the mitigations work?

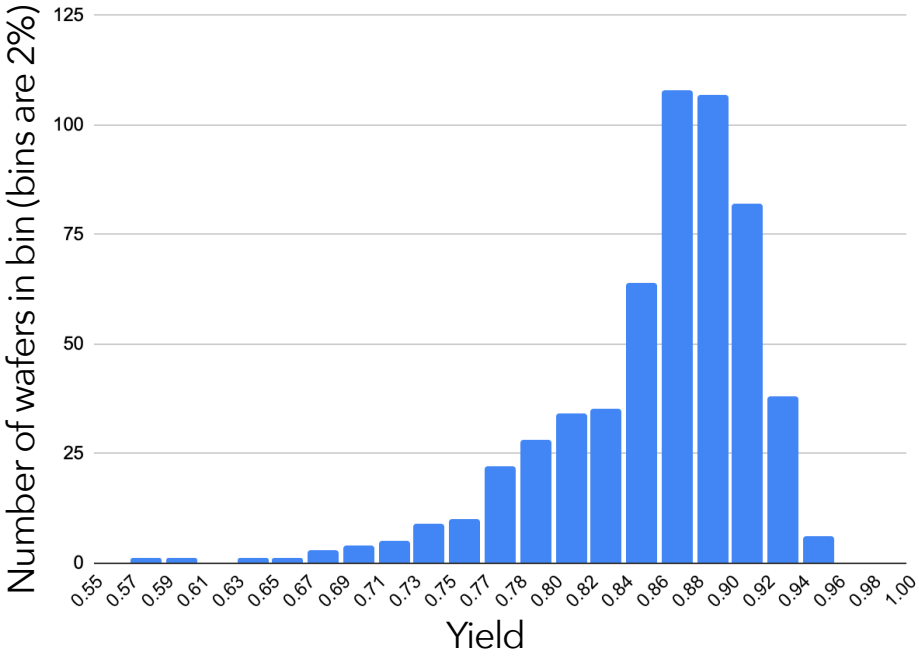
The combination of the 2 mitigations:

- Increasing the digital chip supply voltage
- Inverting the clock, giving a duty cycle ≥ 50%

Has minimized chips rejected due to SRAM hit loss.

ABCStar yields have improved from averaging **66%** before to **86%** after the mitigations.

ABCStar yields per wafer, after mitigations



What happened?

What can we learn?

How did this happen?

The ABCStar SRAM issue arose because:

- The timing models of the SRAM block were ~10 years old, made according to best practice then. Better tools now exist. We believe:

  SRAM timing library was inaccurate → chip tools had wrong specs, put too little buffering → signals delayed vs. clock edge → some hits lost
- The SRAMs worked during prototyping (previous versions, ABC130 and ABCStarV0), so they were regarded as "silicon proven"
- When finalising the production version, the ABCStarV1, the schedule was delayed. There was considerable pressure to submit the design. So we did not re-check blocks that were believed to be working fine.
- However, in prototyping, we manufactured only one production lot.
- So we did not see the full range of variation of process space of manufacturing. So we did not see the hit loss issues, which only appeared for slower wafers.
- So "silicon proven", with only 1 run, is less proof than it might seem.

How can we avoid this?

In chip design, we rely on libraries of models for simulations, covering ranges of: voltages, temperature, process variations and radiation dose. But models can have errors. There is a good back-up available:

Foundries offer "striping":

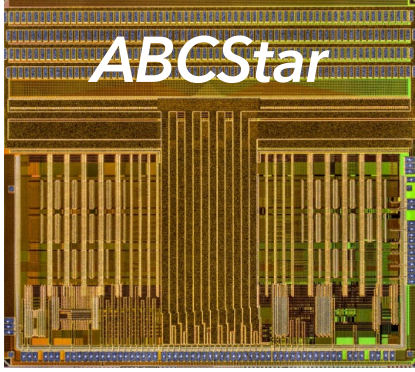
- They will build experimental wafers to cover a representative range of process outcomes (all corners: slow-slow, slow-fast, fast-slow, fast-fast)
- The costs are modest. At our foundry, experimental wafers cost 150% of an engineering run wafer.

So when planning new projects, let's:

- Include the money for striping
- Include the time to order and characterise striped wafers

Bonus: we are more likely to learn about yield issues earlier.

Conclusions



The ABCStar, the front-end readout ASIC for ITk Strips, is deep in production: **36%** complete.

Happily, production is quite boring now: steadily progressing.

Production should complete by April 2025.

We discovered a hit loss issue, now understood and mitigated.

A root cause was an over-reliance on "silicon proven" before learning about real process variations in wafer manufacturing.

To avoid this, future projects can plan to use striping, to learn about process variations early on, which will help to:

- Avoid design issues
- Learn about real yields much earlier

Thanks to…

You for your attention.

Production, investigations and mitigations: (alphabetically)

Bill Ashmanskas (Penn), James Botte (Carleton), Bruce Gallop (RAL), Michael Hank (Penn), Guglielmo Frattari (Brandeis), Jaya John John (Oxford), Jan Kaplon (CERN), Paul Keener (Penn), Kostas Kloukinas (CERN), Thomas Koffas (Carleton), Joe Kroll (Penn), Pedro Leitão (CERN), Bobby McGovern (Penn), Daniel Camarero Muñoz (Brandeis), Bryce Norman (Carleton), Peter W. Phillips (RAL), Luise Poley (TRIUMF),Craig Sawyer (RAL), Evelyn Thomson (Penn), Georg Viehhauser (Oxford), Sven Wonsak (Liverpool)

Questions?