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Design optimization of a Dual-Interlocked-Cell in 65 nm CMOS tolerant to Single Event Upsets

F. Márquez,[a,*] **F.R. Palomo,**[a,c] **F. Muñoz,**[a] **D. Fougeron**[b] **and M. Menouni**[b]

[a] *Group of Electronic Engineering (GIE), University of Sevilla, Seville, Spain*
[b] *Aix Marseille University, CNRS/IN2P3, CPPM, Marseille, France*
[c] *CERN, 1211 Geneva 23, Switzerland*

E-mail: fmarquez@gie.us.es

Abstract: Dual-Interlocked-Cell (DICE) latches are tolerant to Single Event Effects (SEE) by design owing to intrinsic redundancy. In nanometric technologies, as in the 65 nm scale, there are new SEE vulnerabilities associated with charge sharing between nodes. Herein we present a systematic analysis of the robustness against radiation using a simulation software tool for analog and mixed-signal circuits (AFTU) that emulates the possible effects generated by particle impacts. In this paper, we evaluate the influence of SEE on circuit performance using this tool as an RHbD assessment for designers. An exhaustive study of the possible vulnerabilities of the DICE architecture is performed, including an evaluation of the proximity between critical nodes at the layout level. As a result, we propose several modifications to the cell implementation to optimize its robustness against Single Event Upsets (SEU). An assortment of five designs with different variations of the original DICE scheme was sent for fabrication on a new chip and tested under ion beams, with promising results showing a clear improvement in the SEU sensitivity of the cell. The best results come from a redesign of the load circuitry to avoid a SET2SEU effect and full interleaved layout to avoid charge sharing effects after a single event.

Keywords: Models and simulations; Radiation-hard electronics; Accelerator modelling and simulations (multi-particle dynamics, single-particle dynamics); Heavy-ion detectors

*Corresponding author.

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1 Introduction

The inner tracker readout integrated circuit for the pixel detector in the ATLAS and CMS experiments of the High Luminosity Large Hadron Collider (HL-LHC) upgrades at CERN [1], is currently under development using a 65 nm CMOS process by the CERN-based RD53 collaboration [2]. The chips will operate close to the beam pipe, hence they are subjected to high levels of Total Ionizing Dose (TID) of about 500 Mrad and Non-Ionizing Energy Loss (NIEL) corresponding to an equivalent fluence of $2 \times 10^{16}\ \mathrm{n_{eq}/cm^2}$. High levels of radiation can lead to degradation of transistor performance and/or radiation-induced transient effects, like Single Event Effects (SEEs), that cause temporal or even permanent failures in the functionality. Displacement Damage is not an effect to primarily worry about for MOS microelectronics because they are majority carrier devices [3]. Although significant research has been done to understand the effect of TID accumulation on MOS transistors and, specifically, on digital standard cells [4, 5] there is still work to be done about Single Event Upsets (SEUs) cross-sections of memory elements built with digital standard cells [6–8].

SEEs are caused by energetic particles striking in such a way that the liberated charge modifies the performance of the circuit. They can affect directly by overriding the value in the storing node (SEU) or indirectly by causing transients (Single Event Transient, SET) on signals such as clock, set, or reset that drive the storage nodes of a memory element. SEU events in the LHC are dominated by hadrons with energy greater than 20 MeV. It is assumed that all hadrons above this value have the same effect: the generation of ionization in the bulk of the device by a Si recoil or by the ejectile of a nuclear reaction [9, 10]. The expected Linear Energy Transfer (LET) spectra are limited up to

15–16 MeV·cm^2/mg, so the radiation hardening of memory elements can be achieved by redundancy or by ensuring that the SEU device cross section is negligible below that LET limit.

Redundancy is possible when these memory elements are triplicated, using one of the Triple Modular Redundancy (TMR) methodologies or using a Radiation Hardened by Design (RHbD) memory cell, as offered by Dual Interlocked Cell (DICE) [4]. Structures including D flip flops based on DICE latches have redundant storage nodes and restore the original cell state when an SEU error is introduced in a single node [11, 12], allowing better radiation hardening. The cost to pay is an increased area, typically 2.5 times larger compared to a standard D flip flop, as in the DARE65T ESA library (65 nm CMOS technology) [13]. However, TMR methodologies also require more than a 3 factor in area due to triple redundancy and additional voters. DICE cells need at least two almost simultaneous particle hits to produce an SEU, decreasing the probability of error. However, as the device size shrinks, redundancy becomes less efficient due to the charge sharing between the sensitive nodes as the space between them is reduced [14], such as the 65 nm technology node for LHC.

Last but not least, the LHC community is aware of the problem of conversion of SETs into SEUs (SET2SEU). In particular, this issue was observed in the latches of the FE-I4B read-out chips [15], responsible of reading the pixel detectors located in the ATLAS experiment IBL (Insertable B-Layer). The FE-I4B chip is manufactured in a 130 nm technology node and it uses single DICE memory cells to store pixel configuration values and TMR DICE latches to store chip global configuration values. The ATLAS group observed, by statistical data analysis while LHC was operating, that SETs in the DICEs load lines were transformed into memory flips. That SET2SEU situation was not corrected nor in the single DICEs nor even in the TRM blocks and was dominant over the observed SEU statistics, therefore requiring a careful evaluation.

Consequently, the use of tools that allow designers to locate sensitive nodes and harden circuits before radiation tests is an interesting approach to increase the robustness of electronics for harsh-radiation environments. Whereas there are exhaustive analyses of charge sharing employing 3D simulation tools such as TCAD [16] or from a more physical perspective [17], this paper focuses on a complementary approach that optimizes the time required to find vulnerabilities against radiation in designed circuits. The proposed methodology is based on a tool, called AFTU [18], which uses electrical models to emulate particle impacts with a certain level of charge, allowing fast analyses based on transient simulations to provide RHbD circuits [19, 20]. In this way, the computational cost is drastically reduced with respect to 3D simulations and the SEU study is carried out performing simulations that last similar times to the ones used to properly design the circuits. Experimental results validate this approach as a successful method to help designers in the RHbD process without the need for complex models with high computational cost.

In this paper, we present a methodology to design an RHbD DICE cell in a 65 nm technology, including the I/O electronics. The RHbD approach is twofold: redundancy in the I/O load lines to tackle with the SET2SEU issue and an interleaved layout to avoid the effects of double nearby particle hits or charge sharing from a single hit. The added redundancy in the I/O electronics was deemed necessary after a complete analysis of the SEU hardness with the AFTU simulation tool. The paper is structured as follows: section 2 shows the SET and SEU study of the chosen structure (topology, performed simulations, and results analysis); section 3 describes a proposed modification to the scheme to increase its robustness, whereas section 4 summarizes the different versions of DICE sent for fabrication and main results obtained from experimental measures. Finally, some conclusions of the work carried out are presented in section 5.

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2 SET and SEU sensitivity analysis

2.1 DICE latch topology

The DICE latch schematic studied in this work is shown in figure 1. It is based on the conventional cross-coupled inverter latch structure. The 4 nodes n1 to n4 store data as 2 pairs of complementary values. For example, when the stored data are 0 then n1-n2-n3-n4 = 0101 and, particularly, n1 is low and n4 is high. If we assume a positive upset pulse at node n1, the transistor MP2 is blocked, avoiding the propagation of this perturbation to node n2. At the same time, the MN4 transistor will propagate a negative pulse to node n4 that blocks MN3 and prevents level corruption at node n3. The perturbation is then removed after the transient since nodes n2 and n3 have conserved the true information.

However, if two sensitive nodes of the cell storing the same logic state (n1-n3) or (n2-n4) change the state level due to the effect of a double particle impact, immunity is lost and the DICE latch can be altered. The SEU probability in this scheme can be reduced by layout considerations, as explained in [11, 12], where different options were studied and measured experimentally. However, in this article, a faster method is proposed to estimate possible vulnerabilities and harden the design prior to radiation tests by performing SET/SEU simulations.

Figure 1. DICE latch schematic.

2.2 SET and SEU simulations

The Analog FTU Hardware Debugging System (AFTU) is a tool to evaluate the SEE sensitivity of analog/mixed-signal circuits at the transistor level [18]. To perform this task, the tool uses a testbench from the circuit under test to emulate radiation conditions by means of added configurable sources.

For the proposed circuit, an analog metric has been settled to detect potentially dangerous transient pulses, determining its maximum voltage deviation (from values of nonirradiated signals) and maximum recovery times (Trec). The current sources used as charge injection elements follow

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the double exponential model [21]. Standard formulas (2.1) and (2.2) are applied:

$$Q_{\text{inj}} = dLET\frac{e \cdot \rho}{E_p} \tag{2.1}$$

$$I_{\text{rad}} = \frac{Q_{\text{inj}}}{\tau_d - \tau_r}\left(e^{-\frac{t}{\tau_d}} - e^{-\frac{t}{\tau_r}}\right) \tag{2.2}$$

where e is the electron charge, ρ is the Si density, $E_p = 3.6\,\text{eV}$ is the e-h pair energy creation, $d = 1\,\mu\text{m}$ is the collection depth inferred from the available technology information, Q_{inj} is the injected charge, τ_d is the collection time of the junction and τ_r is the time constant for generation of the ion track.

The user can define a test campaign using some configuration files and parameters, so that the tool will automatically generate an output file with statistical results following some predefined heuristics to determine the SEU vulnerabilities of the scheme. As a first step to evaluate the circuit's SET/SEU sensitivity, a general campaign using AFTU is carried out to emulate the impacts on all transistors in the scheme. To this purpose, the chosen heuristic is based on comparing the selected signals, after receiving an impact, with a nonirradiated pattern; the user settles a threshold value corresponding to the maximum allowed voltage deviation to determine the time, given by Trec, in which the signal significantly differs from its nominal value.

Based on the recovery times obtained from simulations, we can classify the sensitive transistors into three different classes:

1. Class I: transistors affected by a transient glitch at the latch output, with no permanent effect (SET).

2. Class II: transistors whose state, when impacted, generates a change of the state at the output (SEU).

3. Class III: a pair of transistors simultaneously affected that generate an SEU at the latch output.

To determine the SET/SEU sensitivity of the DICE, all transistors of the latch shown in figure 1 are studied after an emulated impact for every possible state. To this purpose, an input signal with a 2 ns period and a 0.2 ns load pulse width has been selected, with a simulation range of 8 ns to evaluate every possible input/output state. Four impact times (at 3, 4, 5 and 6 ns) have been considered to determine all potential SEU occurrences (figure 2) for every pair of input/output combination. Therefore, a SET does not result into an SEU when its width value is below 1 ns (the output latch recovers to its original state before loading a new input value), while every Trec value over 1 ns indicates the occurrence of an SEU. The values obtained for this first exploration are shown in table 1 (left) considering only impacts on isolated transistors.

From the analysis of these results, we can see that there were some transistors that could generate an SEU due to an isolated impact, which should not happen due to the DICE latch structure. This effect is explained later in this paper in more detail.

In addition to this first campaign, simultaneous impacts on different pairs of latch transistors were emulated to perform a study of the sensitivity of the design to double impacts that could potentially generate an SEU. Different layout distributions can help improve circuit performance, as seen in [11]. Taking this into account, an analysis of the SEU sensitivity of the different pairs of

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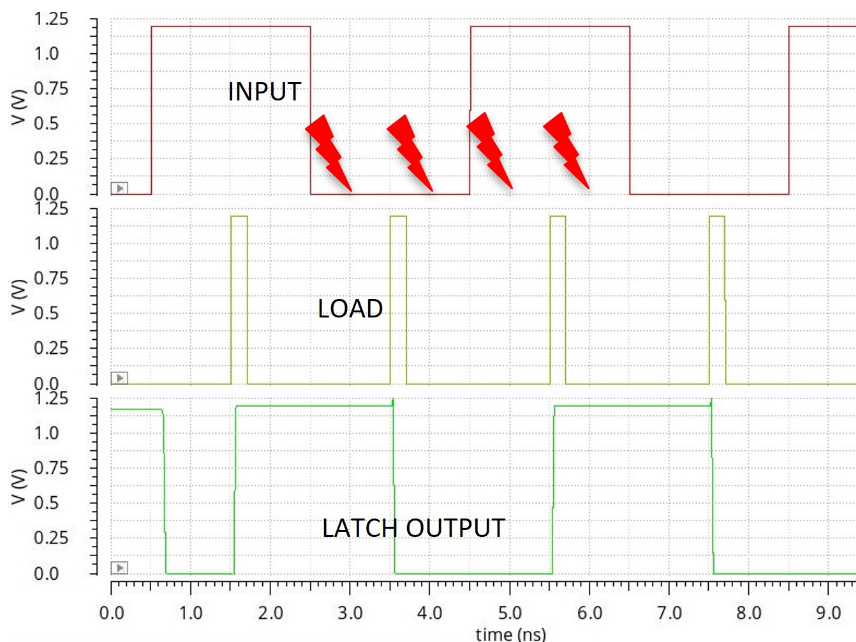

Figure 2. Input signals and impact locations for all possible states.

transistors is extremely interesting to determine possible new distributions of the cell at the layout level to obtain a more robust version against radiation.

For the case of double impacts, the effects produced at the output will always be in the form of SEUs as the state is changed and stored due to the DICE latch structure. From the results obtained in this campaign and those summarized in table 1, we can establish a SET/SEU classification of the transistors according to the criteria previously defined. Table 2 (left) summarizes the different classes of transistors found during the analysis using AFTU, as functions of the injected charge.

As expected, impacts in transistor pairs generate an effect at the output in the form of SEUs (class III). However, the presence of class II transistors is unwanted, as the DICE structure should only be sensitive to impacts that affect two nodes simultaneously. This effect is explained because the input inverter is connected to both load transistors, sharing a common node that can generate a SET2SEU in nodes storing the same logic state (n1-n3) or (n2-n4), as seen in [15]. In section 3, a solution to this problem is proposed using separate inverters for the input scheme.

3 DICE latch redesign for radiation hardening

The analysis of the results from simulations allows the identification of two main issues in the previous version of the DICE scheme. On the one hand, a possible modification to the input scheme used with the DICE latch is proposed. On the other hand, a study of the layout disposition of the transistors is performed to identify a possible improvement in the implementation of a new version of the cell to avoid SEUs by charge sharing even in the case of a single impact

First, a new latch input scheme is proposed to avoid sharing the input nodes through the load transistor, as shown in figure 3. With this proposed scheme, an impact on any of the inverter and/or load transistors will only generate a transient SET instead of an SEU, improving the robustness of

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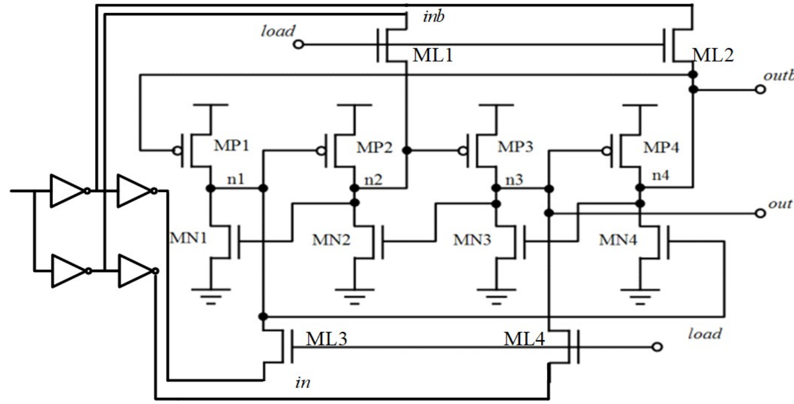

Figure 3. New implemented DICE latch schematic.

Table 1. Effect of impacts on isolated transistors.

		Original Design			New Design		
Transistors	In|Out	T_{rec} [ns] after an impact with Q_{inj} [pC] of					
	state	0.2	0.3	0.5	0.2	0.3	0.5
MN2	0	0.47	0.53	0.61	0.53	0.61	0.68
MP2	1	0.46	0.52	0.61	0.52	0.61	0.67
MN3	0	0.38	0.45	0.53	0.45	0.53	0.59
MN1	1	0.38	0.44	0.52	0.44	0.52	0.59
ML1,2	0|0	> 1	> 1	> 1	No effect	No effect	No effect
	1|0	0.21	> 1	> 1	No effect	No effect	No effect
ML3,4	1|1	> 1	> 1	> 1	0.21	0.38	0.44
	0|1	0.21	> 1	> 1	0.13	0.31	0.38

the DICE latch. Simulations with this scheme are summarized in table 1 (right), where it can be observed that the DICE is no more sensitive to single impacts, in contrast to the results previously shown in table 1 (left) for the original version of the scheme.

In table 2 (right), the results obtained from simulations to evaluate the sensitivity of the new scheme to double impacts are summarized. Comparing these data with those for the original design (left), we can note that this scheme also shows a better performance since all class II errors are eliminated, and even the number of sensitive pairs (class III) is reduced. Furthermore, the critical charge required to generate an error in the DICE circuit increases from 0.05 to 0.2 pC. According to equation (2.1), these values correspond, respectively, to an increase in LET from approximately 5 to 19 MeV·cm^2/mg.

From the analysis of these data and a geometric inspection of the implemented layout, a modification of the previous floorplan was proposed to increase the robustness of the scheme. This can be achieved by optimizing the location of several sensitive pairs of transistors to maximize the distance between them. The different flavors of the layout implemented in the chip prototype will be described and the SEU test results will be compared in the next section.

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Table 2. Different classes of transistors under study.

Q_{inj} [pC]	Class	Transistors	
		Original design	New design
0.05	I	MN2, MP2, MN3, MN1	**None**
	II	None	**None**
	III	(MP2-MP3), (MP2-M2), (MN2-M7), (MN2-MP4)	**None**
0.1	I	MN2, MP2, MN3, MN1	**None**
	II	None	**None**
	III	(MP2-MP3), (MP2-MN4), (MN2-M7), (MN2-MP4), (MP2-ML2), (MP2-ML4), (MN2-ML1), (MN2-ML3), (MP1-MN3), (MP1-ML1), (MP1-ML3), (MN3-MP4), (MN3-ML1), (MN3-ML3), (MN1-MN4), (MN1-ML4), (MN1-ML2), (MP3-MN1), (MP3-ML2)	**None**
0.2	I	MN2, MP2, MN3, MN1	MN2, MP2, MN3, MN1, ML3,4
	II	ML1, ML3, ML2, ML4	**None**
	III	(MP2-MP3), (MP2-MN4), (MN2-MP1), (MN2-MP4), (MP2-ML2), (MP2-ML4), (MN2-ML1), (MN2-ML3), (MP1-MN3), (MP1-ML1), (MP1-ML3), (MN3-MP4), (MN3-ML1), (MN3-ML3), (MN1-MN4), (MN1-ML4), (MN1-ML2), (MP3-MN1), (MP3-ML2)	(MP2-MP3), (MP2-MN4), (MP2-ML3), (MN2-MP1), (MN2-MP4), (MN2-ML2), (MP1-MN3), (MP1-ML4), (MN1-MN4), (MN1-ML3), (MN3-MP4), (MN3-ML2), (MP3-MN1), (MP3-ML1), (ML2-ML4), (ML3-ML1)
0.3	I	MN2, MP2, MN3, MN1	MN2, MP2, MN3, MN1, ML3,4
	II	ML1, ML3, ML2, ML4	**None**
	III	(MP2-MP3), (MP2-MN4), (MN2-MP1), (MN2-MP4), (MP2-ML2), (MP2-ML4), (MN2-ML1), (MN2-ML3), (MP1-MN3), (MP1-ML1), (MP1-ML3), (MN3-MP4), (MN3-ML1), (MN3-ML3), (MN1-MN4), (MN1-ML4), (MN1-ML2), (MP3-MN1), (MP3-ML2)	(MP2-MP3), (MP2-MN4), (MP2-ML3), (MN2-MP1), (MN2-MP4), (MN2-ML2), (MP1-MN3), (MP1-ML4), (MN1-MN4), (MN1-ML3), (MN3-MP4), (MN3-ML2), (MP3-MN1), (MP3-ML1), (ML2-ML4), (ML3-ML1)

4 Experimental results

In this section, the experimental SEU test results corresponding to the DICE latches implemented on a fabricated 65 nm CMOS prototype will be detailed and commented on.

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4.1 Test chip

The RD53SEU chip (figure 4) is a mini ASIC made from a collaboration between the Universities of Sevilla, Bonn, Marseille CPPM and Fermilab within the framework of the RD53 collaboration. It is a test chip designed to study soft error rates from SEE in a 65 nm CMOS process. As a multi wafer project, it has a 2 mm × 2 mm area with digital standard cells and DICE latches. The selection of the test structure and the outputs is done through a multiplexer logic, with the selection lines as inputs of the chip. DICE test structures are included to test their robustness against radiation, with different columns of 640 latches each, composed of several versions of the scheme studied in this work. Concretely, six different versions (table 3) were laid out and implemented to evaluate their performance. W_p and W_n are, respectively, the values of width for the pMOS (MP1-MP4) and nMOS (MN1-MN4) transistors, and L is the channel length which is set to the same value for 2 types of transistor.

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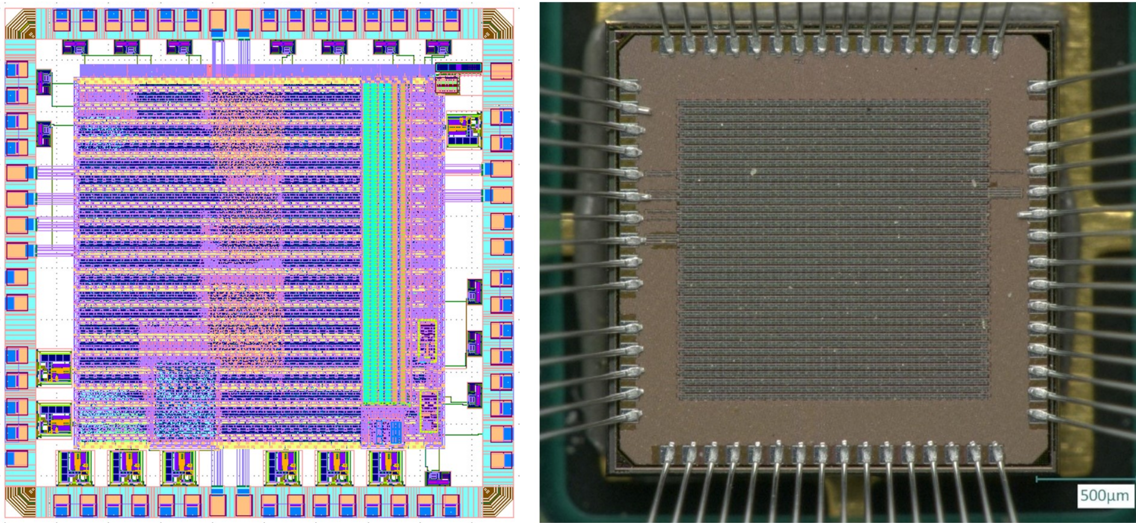

Figure 4. RD53SEU chip with SEU testing structures.

Table 3. DICE versions implemented in the RD53SEU chip prototype.

		W_p (nm)	W_n (nm)	L (nm)
DICE-1	Reference Design	400	200	60
DICE-2	New design	400	200	60
DICE-3	New design + different sizes	400	200	400
DICE-4		500	250	500
DICE-5	New design + interleaved layout (V1)	400	200	400
DICE-6	New design + interleaved layout (V2)	400	200	400

DICE-2 is the new implementation of the design and consists of adding inverters at the inputs while keeping the same transistor dimensions as the reference. DICE-3 and 4 are implemented to evaluate the effect of transistor dimensions (W and L) on SEU tolerance. They use the same design as DICE-2, but with a larger width W or length L. For DICE-3, the length is increased to 400 nm, and in the DICE-4 scheme the widths are 500 and 250 nm, while L is set to 500 nm. The proposed

modifications allow us to maintain a similar structure in the layout core of the DICE, with special attention to optimize area consumption. They only have an impact on the SEU tolerance without affecting delay, power, or threshold. Although dynamic power consumption can be slightly changed, these latches are used to retain configurations in a static way and are refreshed during operation. The objective, as previously discussed, is to avoid SEUs from a single impact due to charge sharing and to minimize the possibility of being affected by double impacts.

The interleaved structure used in DICE-5 and 6 is based on previous reported work [11], although for this new layout the distance between cells is increased and the placement of some transistors is optimized according to the SEU study performed. The layout disposition for a 4-DICE (A, B, C, D) matrix can be observed in figure 5, where the distance between sensitive parts of the same DICE can be noticed (approximately 7.5 micrometers). The DICE-2 to DICE-4 layouts show an increase in area of approximately 20% compared to the original latch (DICE-1). The version implemented in DICE-6 is similar to 5 but it also applies interleaving to the input inverters, with a different routing scheme allowing no additional silicon area. The interleaved layout of the DICE latch is 50% bigger than the original version (DICE-1), and it also increases the area occupation by a 28% compared to the non-interleaved versions (DICE-2 to DICE-4).

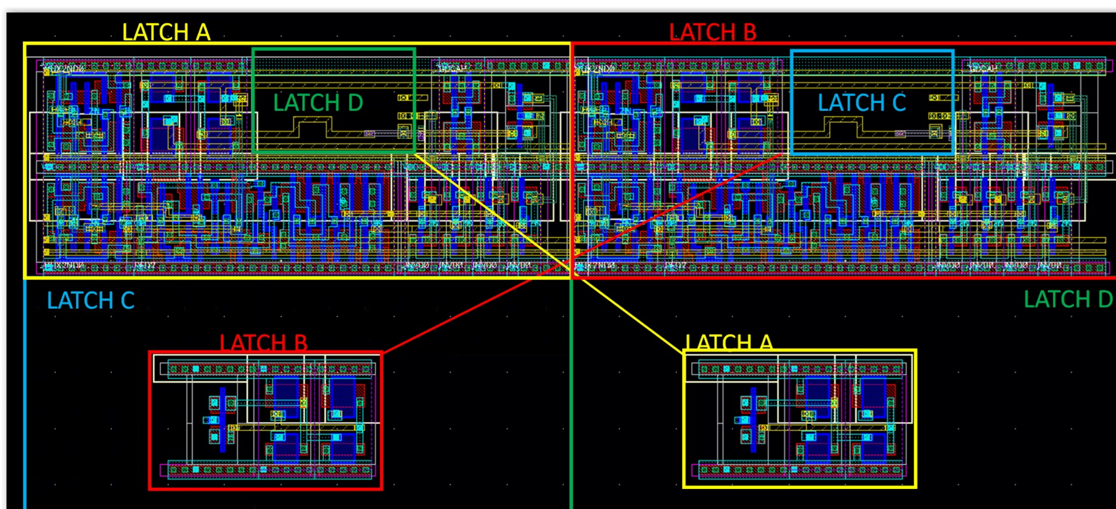

Figure 5. Interleaved layout structure in a 4 DICE matrix.

4.2 Testing setup

The experimental test setup used for the SEU measurements is shown in figure 6. It is composed of a daughterboard and motherboard connected by ribbon cables with DB25 connectors. The RD53SEU fabricated chip is wired to the daughter board and all communication with it is through the mother board. All IO signals are differential and are expected to drive long cables up to ~ 20 m. The FPGA on the mother board sends the timing signals and input data to the chip and receives the data from the chip. The NanoPC BeagleBone card communicates with the FPGA and stores the data on a USB flash drive for later analysis.

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Figure 6. Experimental test setup.

4.3 Heavy ions test facility

SEU tests were performed at the UCL Heavy Irradiation Facility in Louvain-La-Neuve, Belgium (figure 7). Table 4 shows the heavy-ion species used at UCL for the radiation testing of the RD53SEU device and their characteristics. The covered LET range is between 1.3 and 62.5 MeV$\cdot$cm^2/mg and the beam flux can be adjusted between a few particles/s$\cdot$cm^2 and 1.5×10^4 particles/s$\cdot$cm^2. During the test, the flux was set to the maximum and integrated to give the delivered total fluence Φ in (particle/cm^2) on the device. The homogeneity of the beam is $\pm 10\%$ on a 25 mm diameter.

Figure 7. RD53SEU experiment setup.

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Table 4. Heavy-Ion species used at UCL.

Ion	Energy (MeV)	Range (µm Si)	LET (MeV·cm^2/mg)
C	131	269.3	1.3
Al	250	131.2	5.7
Ar	353	120.5	9.9
Cr	505	114.0	16.1
Kr	769	94.2	32.4
Xe	995	73.1	62.5

4.4 SEU test description

To investigate the SEU effects in the different versions of the DICE latches under heavy ions irradiation, only static tests were performed in the RD53SEU test device.

The sequence of tests is performed as follows:

1. Write the data in the memories prior to beam irradiation.
2. Start the beam.
3. When the expected fluence is reached, the test is finished.
4. Read all the memories and compare them with the previous pattern.

The sequence can be repeated with different exposition times to obtain SEU events for all the latches studied. In fact, the test should show enough recorded events to be statistically representative of the chip behavior with respect to SEU.

The cross section per bit is defined as:

$$\sigma = \frac{N_{\text{events}}}{\Phi \times N_{\text{cells}}} \tag{4.1}$$

Where Φ is the total incident particle fluence, N_{events} is the number of SEU events counted during the test, and N_{cells} represents the number of identical DICE cells of the same bank considered for this test.

4.5 Experimental results

This section presents the results of the SEU test measured on the different versions of the DICE schemes presented earlier. In all plots, error bars include 95% statistical confidence intervals plus dosimetry uncertainties (10% for UCL).

Figure 8 shows the heavy-ion SEU cross section for the DICE-1 cell plotted as a function of the incident ion LET and fitted using the Weibull function:

$$\sigma = \sigma_{\text{sat}} \left[1 - \exp\left(-\frac{\text{LET} - \text{LET}_{\text{th}}}{W} \right) \right]^S \tag{4.2}$$

Where σ_{sat} is the saturated cross section for high values of LET. LET_{th} is the threshold LET for upsets, S and W are free parameters that define the shape of the Weibull plot.

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The SEU cross section was computed based on 640 configuration bits and a fluence of 1×10^7 ions/cm^2 allowing a sufficient number of events, especially for the low LET ions. The Weibull fit of the SEU data depicted in figure 8 shows a threshold LET of around 0.1 MeV$\cdot$cm^2/mg and a saturation cross section of 1.1×10^{-8} cm^2/bit, which is not a great improvement over a standard latch cell without redundancy.

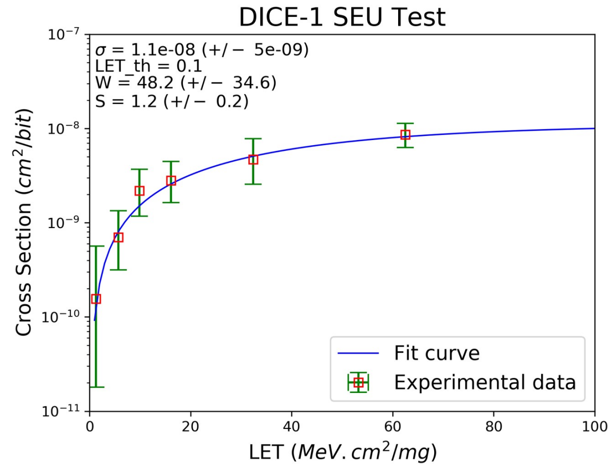

Figure 8. DICE latches without the input inverter duplication.

Figure 9 shows the heavy-ion SEU cross section of the DICE-2 cell. This cell was tested exactly under the same conditions as DICE-1, since the two cells were exposed to the beam at the same time and received the same particle fluence. We can observe that no SEU errors were observed for LETs smaller than 16 MeV$\cdot$cm^2/mg. For strong LET like for the Xenon ion, the effective cross section is around 1×10^{-8} cm^2, which is of the same level as what is observed on DICE-1. In this case, a strong charge is injected on the DICE and most of the SEU events are due to the charge sharing between the sensitive node (n1-n3) or (n2-n4), which makes the redundancy no longer effective.

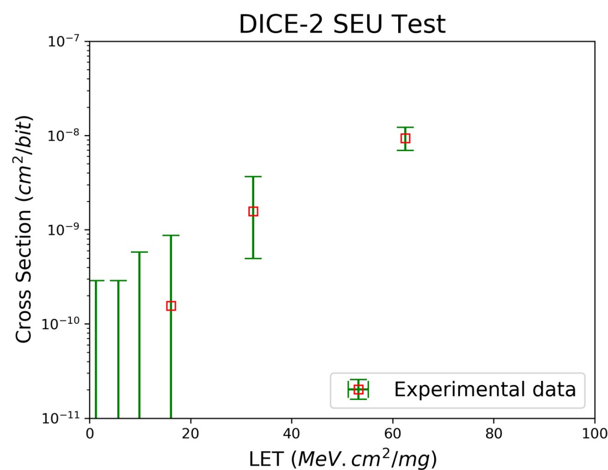

Figure 9. DICE latches with input inverter duplication.

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It is difficult to fit the DICE-2 SEU data with the Weibull function because no errors were reported for small LETs. However, it can be inferred from the measurement data shown in figures 9 and 10 related to DICE-2 and DICE-3 that the LET threshold for both cells can be evaluated between 10 MeV·cm^2/mg and 16 MeV·cm^2/mg. It can be clearly concluded that DICE-2 and DICE-3 are more tolerant to SEU than DICE-1. The results for DICE-4 show a similar response to those included for both previous designs. This shows that increasing the transistor size has little effect on SEU tolerances. If such a small effect does exist, it would have to be observed in high-fluence tests. These results confirm that most of the SEU observed for DICE-1 are, as mentioned in section 2, indeed related to the SETs on the input transistors (ML1 to ML4), as also expected from the work in [15] where the SET2SEU effects in the load lines were found to be dominant.

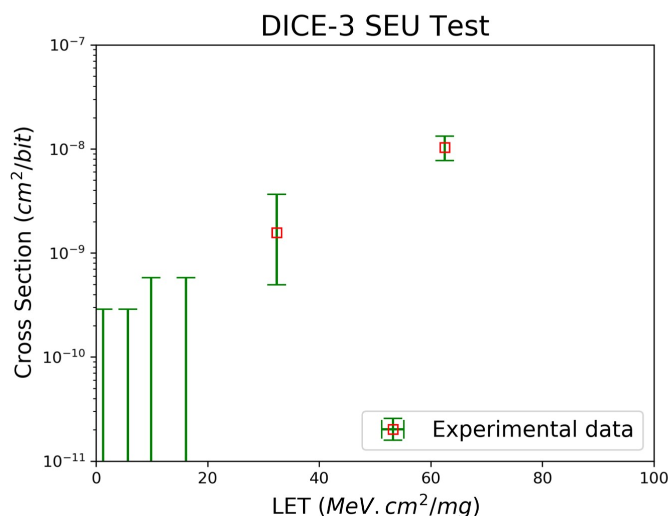

Figure 10. DICE latches with input inverter duplication and using long channel transistors.

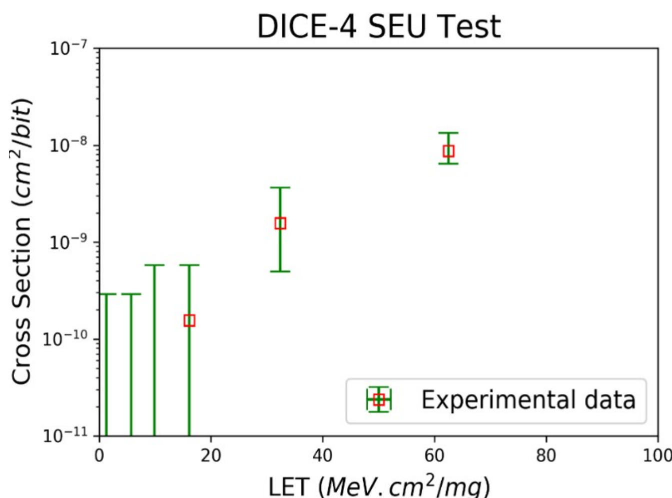

Figure 11. DICE latches with input inverter duplication and using wide channel transistors.

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Finally, we can mention that no disturbance was observed for DICE-5 and DICE-6 during the entire test campaign, even for the highest LET values. These results show that the new interleaving layout (DICE-5, 6) cells work well and drastically reduce the charge sharing effect. So it seems that the interleaved layout can remarkably increase SEU tolerances. Of course, this is achieved by making the layout more complex and using more levels of metallization, which increases the cost of the design. The use of one version or another depends on SEE tolerance requirements. For applications where the detector is very close to the beam, making particle flow quite high, DICE 5 and 6 are recommended despite the added complexity of the layout. However, for detectors far from the beam, DICEs 2 to 4 may be sufficient. As the maximum LET values expected in HL-LHC are below 16 MeV·cm^2/mg, the presented DICE schemes appear to be an effective solution to avoid the presence of SEUs.

5 Conclusions

The presented work shows an exhaustive study of a DICE latch circuit in 65 nm CMOS technology using an automated tool to determine its SET/SEU sensitivity. The analyses carried out allow designers to detect vulnerabilities before testing and propose several modifications at the architecture and layout level to increase its robustness. Additionally, the simulations to emulate particle impacts are similar to the transient ones used to design the circuits, with no need of 3D analysis tools that can increase the computational cost and simulation times. The implemented schemes have been measured on a new test chip and show promising performance in harsh-radiation environments, with a drastic increase in the robustness of the proposed interleaved layout. The proposed DICE 5 and DICE 6 latches demonstrate insensitivity to single events under realistic conditions in the beam test. The SEU threshold is not only above the expected LET in the LHC environment (16 MeV·cm^2/mg), but these schemes also show insensitivity to charge sharing for particle hits with very high LET (> 60 MeV·cm^2/mg). The price to pay is an increase in layout area (by a 50% factor) relative to the original DICE latch, in addition to higher complexity in the design routing and more levels of metallization required. DICE 2–4 latches are sufficiently resistant to SEU and SET2SEU for the LHC environment, so they are a valid option to consider when area occupancy in the chip is an issue. They only show charge sharing effects at LET values bigger than expected in the LHC environment. For LET values beyond 30 MeV·cm^2/mg, charge sharing can be a problem so DICE 5 and in particular DICE 6 (full interleaved layout) are the recommended options even paying the price of an increased area consumption.

The methodology followed to obtain an RHbD DICE structure illustrates the utility of using AFTU to optimize the SEE tolerance of memory structures and, in general, other digital or analog designs. The experimental results shown in this paper demonstrate the reliability of the tool as an efficient assistance for designers to improve the tolerance of circuits to SEU/SET in a previous stage to radiation tests.

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