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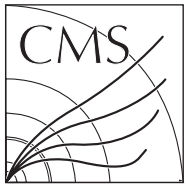

The Compact Muon Solenoid Experiment

Conference Report

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Serial powering characterisation for the CMS Inner Tracker at the High Luminosity LHC

Rudy Ceccarelli for the CMS Collaboration

Abstract

The CMS tracking system will be completely replaced in order to operate in the extreme conditions of the High Luminosity LHC.The new tracker will consist of two main subdetectors the Inner Tracker, containing pixel modules, and the Outer Tracker, consisting of strip and macro-pixel modules.In the Inner Tracker silicon sensors will be read out by the CMS Readout Chip (CROC).The chip, built in 65 nm CMOS technology, is able to withstand high radiation doses (500 Mrad) and hit rates ($3\,\mathrm{GHz/cm^2}$ on the innermost tracking layer) during operation.Moreover, it must handle a finer sensor granularity ($2500\,\mathrm{m^2}$ pixels) and operate at low detection thresholds ($1000\,\mathrm{e^-}$).The Inner Tracker will make use of the serial powering scheme to provide the about 60 kW required by thousands of modular units.The Shunt-LDO (SLDO) regulator is the part of the CROC responsible for providing the power by draining a constant current in time, independently of the chip power consumption needs.Tests performed with Single Chip Cards (SCC) in serial configurations are reported in this paper.

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Serial Powering Characterisation for the CMS Inner Tracker at the High Luminosity LHC

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Abstract: The CMS tracking system will be completely replaced in order to operate in the extreme conditions of the High Luminosity LHC. The new tracker will consist of two main subdetectors: the Inner Tracker, containing pixel modules, and the Outer Tracker, consisting of strip and macro-pixel modules. In the Inner Tracker silicon sensors will be read out by the CMS Readout Chip (CROC). The chip, built in 65 nm CMOS technology, is able to withstand high radiation doses (500 Mrad) and hit rates (3 GHz/cm^2 on the innermost tracking layer) during operation. Moreover, it must handle a finer sensor granularity (2500 µm^2 pixels) and operate at low detection thresholds (1000 e$^-$). The Inner Tracker will make use of the serial powering scheme to provide the about 60 kW required by thousands of modular units. The Shunt-LDO (SLDO) regulator is the part of the CROC responsible for providing the power by draining a constant current in time, independently of the chip power consumption needs. Tests performed with Single Chip Cards (SCC) in serial configurations are reported in this paper.

Keywords: Front-end electronics for detector readout; Radiation-hard electronics; Particle tracking detectors (Solid-state detectors)

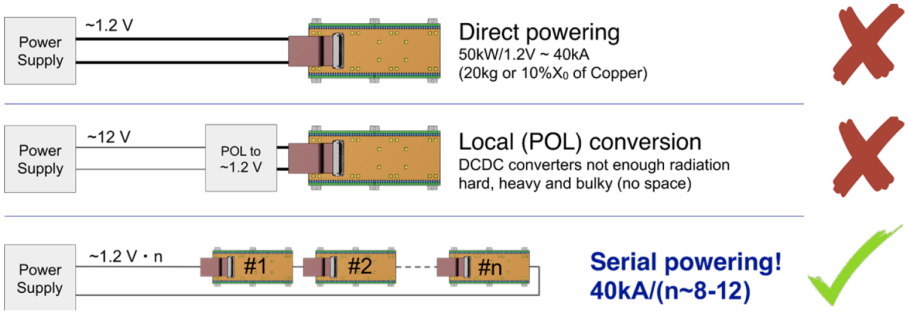

Figure 1. Comparison of three different types of powering schemes for the CMS Inner Tracker.

Contents

1 The Serial Powering Scheme in the CMS Inner Tracker Upgrade

The CMS experiment [1] Phase-2 tracker, foreseen for the High Luminosity phase of the Large Hadron Collider (HL-LHC), has two major systems: the Inner Tracker, closer to the collision point and containing pixel modules, and the Outer Tracker, containing strip and macro-pixel modules [2]. The Inner Tracker have stringent design requirements, such as a radiation tolerance of at least 500 Mrad, high rate capabilities (up to 3 GHz/cm^2), high granularity ($50 \times 50\,\mu m^2$ pixel cells) and low thresholds and noise. These requirements require a very high power consumption, of the order of 50 kW for the Inner Tracker

The CROC is the new CMS pixel readout chip, developed inside the RD53 collaboration [3], a joint CMS and ATLAS effort to develop the pixel electronics of the experiment upgrades for the HL-LHC. The CROC is designed in 65 nm CMOS technology, features 1.5×10^5 pixel channels and requires about $8 - 10\,\mu A$ per channel: by adding the power consumption of the chip periphery, the total needed current is around 1.5 A, with a supply voltage of 1.2 V.

A direct powering scheme would require large cross-section power cables, which would dramatically increase the passive material in the tracker. A possible approach, based on the present pixel tracker, is based on DC-DC converters. However, these are affected by two problems. In the first place, they are not radiation resistant enough for the Inner Tracker environment. In the second place, they are large and heavy objects that are difficult to place inside the tracker, while also adding significant passive material near the collision point. While this scheme is indeed used in the Outer Tracker,

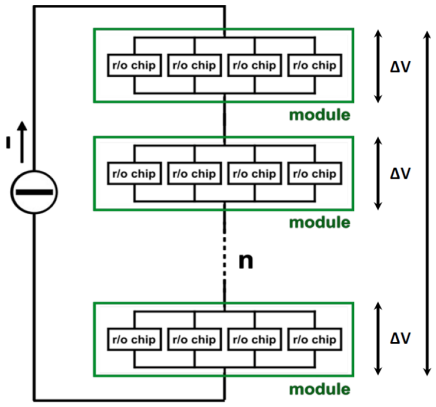

Figure 2. Schematic representation of a serial powering chain: the chips inside a module are powered in parallel.

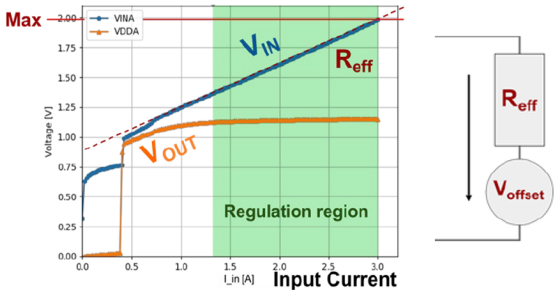

Figure 3. Equivalent circuit of SLDO: the CROC is seen as an effective resistance plus an offset voltage.

since it is far less affected by these problems, the Inner Tracker has opted for a serial powering scheme instead [4]. Figure 1 shows the main differences of the three powering options.

The Inner Tracker is organised in serial powering chains of up to ten modules: each module in the inner (outer) layers will have a single sensor bump-bonded to two (four) ROCs, which are usually referred to as "double" ("quad") modules. Doubles will be installed in the two innermost tracker layers, while quads will be installed in outer layers.

The ROCs of each module are connected in parallel, as shown in Figure 2: the ROC includes a highly specialized circuit that combines the functionality of a current shunt and a Low-DropOut (LDO) regulator, thus referred to as Shunt-LDO (SLDO). The SLDO ensures that power and current consumption are kept constant, independent of hit and trigger rates. Moreover, the SLDO is designed to ensure appropriate current sharing between multiple chips, powered in parallel. Thanks to this scheme, the serial chain presents itself as a constant load to the power supplies: the SLDO manages the ROC power consumption variations. Figure 3 shows the equivalent circuit of the SLDO: an effective resistance plus an offset voltage. For low current values there is a transient, for which this chip is still not operative. Once a high enough current is reached, the output voltage is kept constant regardless of the input current.

The current injected in the power loop must satisfy the highest possible load current, including an extra headroom to comply with fast dynamic current variations of the digital logic of the chip.

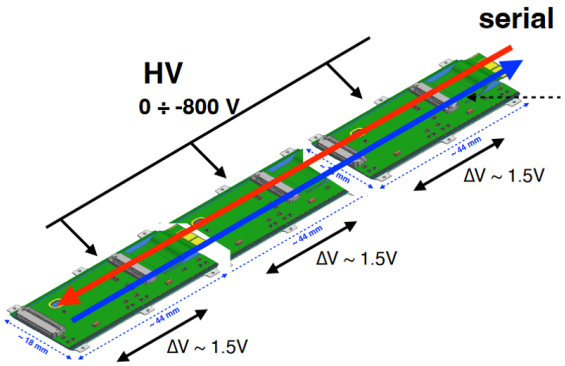

Figure 4. Prospective view of pixel modules in serial power chain: the bias voltage to deplete the silicon sensors is provided in parallel.

Consequently, each serial power chain will require an injected current of up to 8.0 A (for a "quad" module), out of which 6.0 A would be consumed by the pixel chips and 2.0 A would be the extra current headroom (25%). Since it is crucial that the digital current variations do not affect the sensitive analogue front-end part of the chip, two SLDOs are integrated on the chip, one per power domain (digital and analogue).

One downside of the serial powering scheme is that it is more susceptible to failures, since a malfunction in one module propagates to all the chain. Therefore a careful study of the possible failure scenarios is necessary.

Each module in a chain works with a different local ground, since the output of a module is the input of the following one. Since the bias voltage (needed to deplete the silicon sensors) is provided with a direct powering scheme (as shown in Figure 4), with the modules in a chain connected in parallel, the applied bias voltage on the silicon sensors is different through the chain. There are two independent high voltage lines for a chain of ten modules therefore, considering a maximum voltage drop of 2.5 V between two modules, the maximum bias voltage difference between two modules in a chain is about 10 V. This could lead to performance differences along the chain for some types of pixel sensors.

Two types of pixel sensor technologies will be used for the future Inner Tracker: traditional planar pixel sensors, where the electrodes are parallel to the sensor surface, and 3D pixel sensors, where the electrodes are orthogonal to the sensor surface [5]. The latter feature a higher radiation resistance thanks to a reduced drift distance, therefore they will be installed in the innermost tracker layer. Another key feature of 3D sensors is that the bias voltage needed to deplete 3D sensors is smaller with respect to planar sensors: usually the depletion voltage of 3D sensors is as small as 5 V. Therefore, the effect of the bias voltage drop inside a serial powering chain is more pronounced for 3D sensors. The goal of this Paper is demonstrate that the performance of 3D modules is not affected by this bias voltage drop.

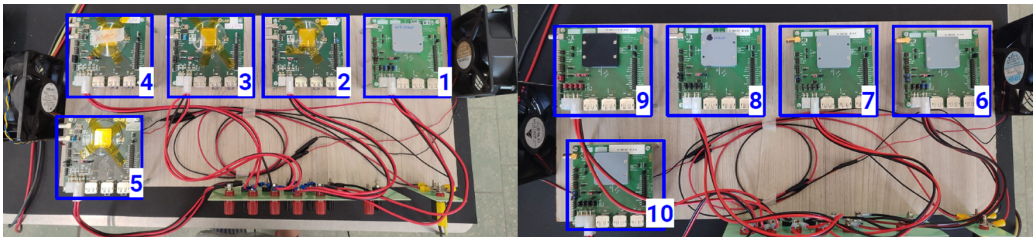

Figure 5. Photograph of the experimental setup, showing a serial power chain of 10 CROC modules (with 3D or planar pixel sensors).

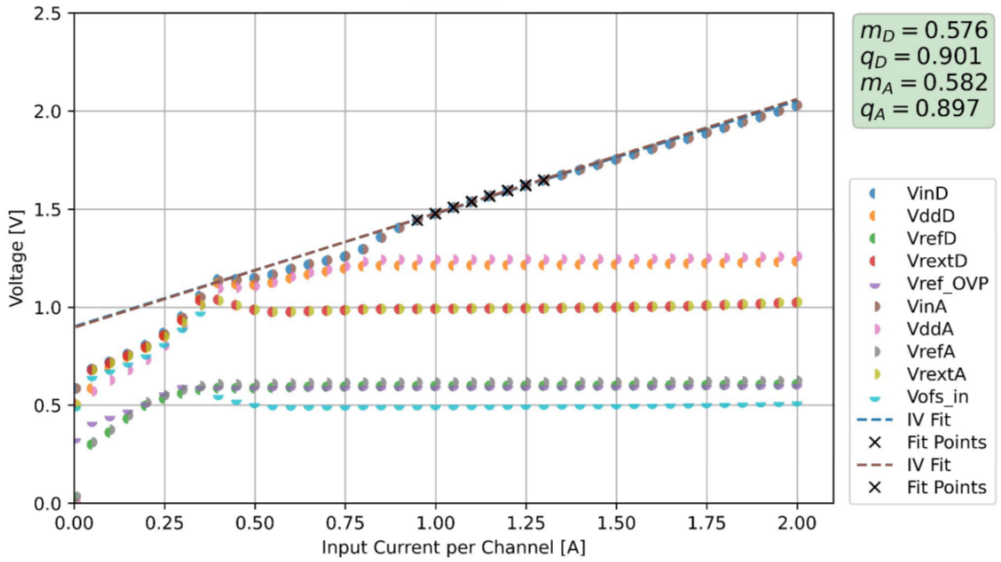

Figure 6. IV curve of the 3D CROC module under test inside the serial power chain: the behaviour is the same as when operated in stand-alone. Several chip parameters are monitored during the scan, such as the LDO-regulated digital and analogue voltages (VDDD and VDDA), which are around 1.2 V, as expected.

2 3D Sensor Performance in a Serial Powering Chain

In order to test the performance of a 3D module in a serial powering environment, a serial powering chain of ten modules was prepared. The modules were made by a sensor coupled to a CROC and mounted into a Single Chip Card (SSC). The SCC is designed for testing, and is useful to check the behaviour of the chip before assembling the full modules (doubles and quads). The ten modules featured a variety of pixel sensors, both 3D and planar. Figure 5 shows a photograph of the setup. Four fans were placed near the modules in order to cool down the system.

One 3D module of the chain was taken as reference and measured in several scenarios. Figure 6 shows the IV curve of the 3D module under test: the input current was increased from 0 A to 4 A, passing trough the working point of 2 A. The IV curve reports the current per (analogue or digital) domains, assuming a 50% sharing between them. In can be observed that VinD/A linearly increases with the current, similarly to Figure 3. Several voltages are measured on the SCC during the IV scan: in particular, VDDD/A are the LDO-regulated digital and anlogue voltages, which are

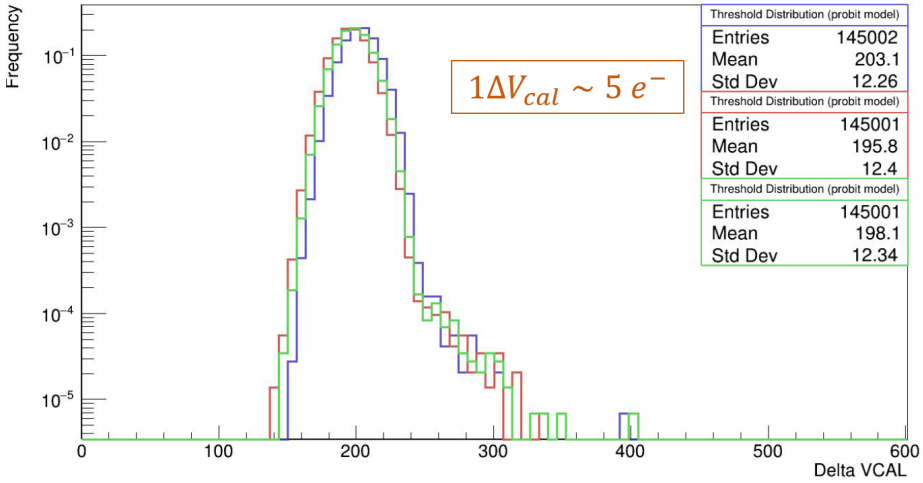

Figure 7. Threshold distribution of the 3D CROC module under test in three different positions of the serial power chain: blue is the first position, red is the sixth position and blue is the tenth position. No significant differences can be observed.

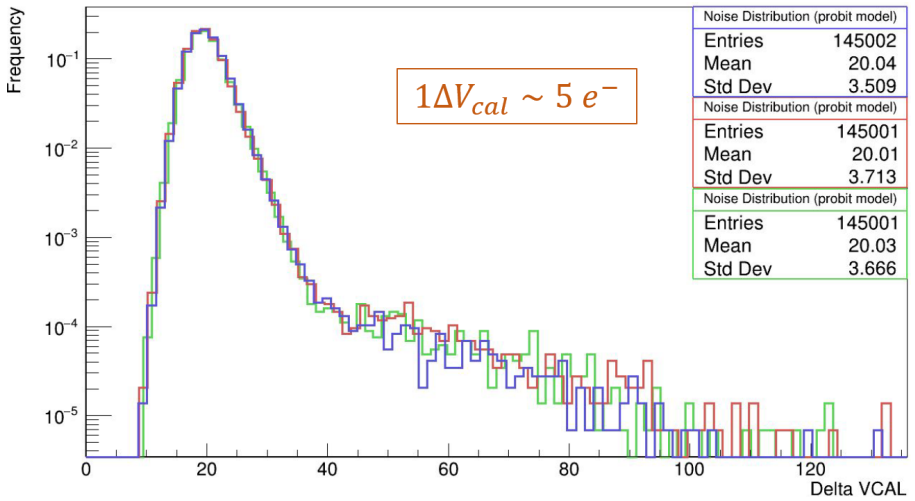

Figure 8. Noise distribution of the 3D CROC module under test in three different positions of the serial power chain: blue is the first position, red is the sixth position and blue is the tenth position. No significant differences can be observed.

both around 1.2 V as expected. This IV curve was performed both inside the chain and in standalone (i.e. individually powered): no differences were observed.

The 3D module under test was first tested in standalone, with a bias voltage of 30 V: it was tuned to an average pixel threshold of 1000 e^-. Then, the 3D module was tested in three different position of the chains. It should be noted that the 30 V of bias voltage is referred to ground (which correspond to the last position of the chain). Therefore, the effective bias voltage of the 3D module varies depending on its position inside the chain. Figure 7 and Figure 8 show the threshold and noise distributions of the 3D module under test for three different positions in the chain: first (in blue), sixth (in red) and tenth (in blue). No significant differences can be observed in the three positions: the threshold and

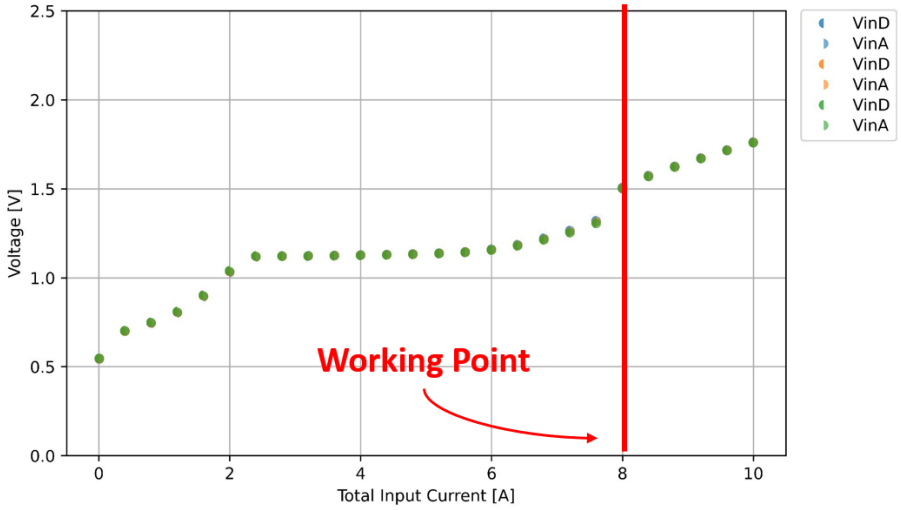

Figure 9. IV curves of thee CROCs in parralel with a disabled CROC: their offset voltages are shorted together. The current working point for a "quad" module is highlighted.

noise distributions have average values of 1000 e^- and 100 e^- respectively, compatible with values observed in standalone.

In conclusion, this test showed that the performance of a 3D pixel module is not affected by the serial powering scheme.

3 Offset Voltage Sharing

The two (four) ROCs in a "double" ("quad") module have their respective offset voltages shorted together. In this way little variations between the ROCs are corrected and the current sharing between the chips is improved. However, this configuration opens a possible failure scenario: if one of the chips stops working, the other one (three) in parallel will have a lower offset voltage, and therefore an higher current is needed to turn on the chips.

This scenario was tested by switching off one CROC while keeping other three CROCs in parallel on. Figure 9 shows the IV curve of the three CROCs in parallel: they are perfectly superimposed. The ohmic behaviour of the SLDO starts at 8 A, which is the working point for a "quad" module. Therefore, the system can sustain this failure scenario.

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