TESTS OF THE TIMING SYSTEM PROTOTYPE

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In this note some results, which were obtained by the execution of the very compressed test program, are described. The examinations have shown the correct and reliable operation of the tested prototypes within the preselection range with the exception of their borders. The analysis of the reasons for these exceptions and the proposed changes in the logic schemes which have been made and checked are considered in the note.

Since the edge positions of the preselectors will not be used under normal operation conditions, the main purpose of the modifications is to improve the "foolproof" properties of the timing system.

1. Test arrangement

In order to measure the number of the timing pulses the "General Radio" counter of type 1192 was used. However, a special adapter was needed to convert the timing pulses into the control signals which had to be applied to "START" and "STOP" inputs of the counter. Two types of such adapters have been made for two different kinds of measurements, namely :

type "A" (fig. 1) - to count the total number of the train pulses;

type "B" (fig. 2) - to check the ordinal index of the selected pulse.

The exact definition of the selected pulse index becomes rather delicate in the case of the RF scaler test. The problem is to take into consideration all delay times between the positive edge of the selected RF pulse and the negative edge of the corresponding count pulse to produce the control signal "STOP" at the proper instant (fig. 3). The proposed adapter of the type "B" eliminates this problem and gives reliable results without any difficulties since the pulse train to be applied to "input A" of the counter passes the adapter gate which interrupts it automatically just after the selected pulse (fig. 2).

Connection schemes for the measurements are shown on figs. 4,5,6. The following remark concerning the RF 1999 generation must be taken into account at the time of the test. It has been noticed that the "RESET" pulse applied to the RF 1999 generator can cause a "parasitic" pulse on its output under certain conditions (fig. 7). It is clear that such

a pulse does not interfere with the normal operation of the RF scalers at all, but can distort the measurement results. That is the reason why the counter has to be kept in the "STOP" state during the reset time. This is provided by a proper choice of the timing pulses for the "START" and "STOP" control signals (fig. 5).

2. Results of the RF scaler prototype tests

2.1a The selection of the pulses from the RF 1999 train by the RF pre-scaler prototype corresponds to the formula

$$N_{pulse} = 10^3 - N_{pre}$$

for the whole preselection range from 0 to 999.

Here : N_{pulse} - ordinal index of the selected RF 1999 pulse;

N_{pre} - index of the pre-pulse set on the preselector.

2.1b The RF post-pulse selection corresponds to the formula

$$N_{pulse} = 10^3 + N_{post}$$

for a preselection range from 1 to 999 only, where

N_{post} - index of the post-pulse set on the pre-selector.

If the RF post-scaler preselector is set on "000" position, the output pulse is not generated.

In this exceptional case the post-scaler is preset to a number 999, while the decoding used for the post-scaler is "998". Therefore, the first decoder pulse appears at 998-999+1000 = 999 pulses. But the 1000th pulse, corresponding to the "000" preselection, cannot pass an output coincidence gate since the coincidence is only established with the second decoder pulse for the post-pulse mode.

To provide the generation of the "000" post-pulse as well, it is proposed to use the same decoder "999" for both the pre-scaler and the post-scaler but, in the case of the post-pulse mode, to add a supplementary "1" to the nine'scomplement information of the preselector. This supplementary pulse can be formed from the negative edge of the preset pulse to be introduced into the counter when the preset is finished (fig. 8).

2.2 The stability of the propagation time of the selected pulse is very important from the point of view of the FES performance. The influence of some factors on the delay time between the output pulse of the post-scaler prototype and the corresponding input pulse

of the RF 1999 distribution amplifier has been estimated. The propagation delay time (t_{pd}) was measured by means of the "Hewlett Packard" oscilloscope of type 180 A(with plug-in unit of type 1801A) and, being normally equal to 62 ns, had the following behaviour:

a) under temperature increase from 25 to 45°C the t_{pd} decrement remained within the display resolution of ~ 0.5 ns;

b) under ± 5°/o voltage variations of the +24 V power supply the t_{pd} deviations were within the display resolution;

c) under ± 5°/o voltage variations of the +5V power supply the t_{pd} deviations were less than ∓ 2 ns;

d) under ± 5°/o amplitude variations of the 2 V input pulse (worse conditions) the t_{pd} deviations were less than ∓ 2 ns.

Thus, the stabilized power supplies will obviously cause the negligible t_{pd} instability. As for the jitter, it was not noticed at all during the test.

2.3 The post-scaler prototype operated correctly under temperature of 45 ± 2°C during a long time.

3. Results of the B+T scaler prototype tests

3.1 The selection of the pulses from the B+T train by the B+T post-scaler prototype corresponds to the formula

$$N_{pulse} = N_{ej} + N_{post}$$

for the whole preselection range from 0 to 99 999, if $N_{ej} > 0$. The post-pulse is inhibited if $N_{ej} = 0$.

Here :

- N_{pulse} - ordinal index of the selected pulse of the B+T train initiated by the "START" pulse;
- N_{ej} - index of the ejection pulse set on the kick parameter preselector.
- N_{post} - index of the post-pulse set on the post-scaler preselector.

3.2 The B+T pre-pulse selection corresponds to the formula

$$N_{pulse} = N_{ej} - N_{pre}$$

for the whole preselection range from 0 to 99 999, if $N_{ej} > N_{pre}$. The pre-pulse must be inhibited if $N_{ej} \leq N_{pre}$. But in fact the rule

is transgressed in two exceptional cases, when N_{pre} = 99 999 or N_{ej} = 00 000.

a) If N_{pre} is equal to 99 999, the comparator of the pre-scaler is preset to a number 00 000. Thus after an overflow of the counter its state will be 00 000 again and the output coincidence gate will pass the next B+T pulse with an ordinal index of

$$10^5+1-(10^5-N_{ej}) = N_{ej}+1$$

where the expression in parentheses is a number of the prerun pulses.
To eliminate the production of such a pulse it is proposed to apply to the output coincidence gate the gated B+T train which is interrupted after the overflow (fig. 9).

b) If N_{ej} is equal to 00 000, the number of the prerun pulses is 10^5. Thus, the overflow occurs before the "START" pulse, when the "START-STOP" flip-flop, gating through the B+T train, cannot register the overflow signal, being in the "STOP" state. Therefore, after the "START"pulse the pre-scaler begins to count from 00 000 and produce a pulse with the ordinal index of

$$99\ 999 - N_{pre} + 1 = 10^5 - N_{pre}.$$

To eliminate the production of such a pulse it is proposed to rearrange the present logic network so that it would be able to register the overflow signal, beginning from the "RESET" pulse, in order to close the output coincidence gate if the overflow would even occur before the "START" pulse (fig. 9).

4. Results of the kick parameter selector prototype tests

4.1 The selection of the pulses from the B+T train by the ejection pulse generator prototype corresponds to the relation

$$N_{pulse} = N_{ej}$$

for the preselection range from 1 to 99 999. The symbols used here are the same as in item 3.1.

If the kick parameter selector is set on "00 000" position, the ejection pulse must be inhibited, but in fact this requirement is not fulfilled because of the following reason. To set the counter to 00 001 before the "START" pulse, the supplementary pulse is formed by a one shot from the negative edge of the overflow signal. Since the comparator is set to 00 000, after the overflow the supplementary pulse will pass the output coincidence gate as the latter is connected with the one shot output. Thus, the first "ejection" pulse is produced after the 100 000 prerun pulses, the second one occurs after the 99 999 B+T pulses.

To eliminate the production of these pulses it is proposed to cut the conductor between gate 56 pin 13 and gate 34 pin 11 (drawing 374-103-1).

4.2 A number of the prerun pulses N_{prerun} has to correspond to the formula

$$N_{prerun} = 10^5 - N_{ej}$$

to provide the initial state of the pre-scaler before the "START" pulse in accordance with the right hand side of the equation. But in fact if $N_{ej} = 0$, the first prerun pulse gated through just after the "RESET" pulse can be occasionally lost for the pre-scaler and the initial state of the latter can be 99 999 instead of 00 000. The fault is caused by two reasons : -

a) In the pre-scaler the reset pulse formed by means of "C-input-10" is about 0.5 μs longer than that formed by "C-input-2" for the kick parameter selector. Thus, there is great probability that the first prerun pulse will be applied to the pre-scaler in the time of its reset and will not be registered.
In order to initiate the prerun train at the proper instant when the pre-scaler reset is finished, it is obviously necessary to provide a prevalence of the reset duration for the kick parameter selector over that for the pre-scaler. For this purpose it is proposed to increase artificially the transistor storage time in the "C-input-2" having extracted the resistor 220Ω from the collector circuit of the transistor 2N3704 (drawing 374-006-4). However, after the liquidation of this"rough" defect, a "fine" one described below is detected.

b) Since the 1,5 MHz oscillator is not synchronized with the "RESET" pulse, the front part of the first prerun pulse can be cut off by the input gate, which is opened by the negative edge of the reset pulse. Also, the first prerun pulse is always shortened by passing through the output gate as the latter is opened by the positive edge of this pulse with a propagation delay time about 35 ns. Thus, there is a certain probability that before the output gate the first prerun pulse will be long enough to be counted by the kick parameter selector counter, but after the output gate too short to be registered by the prescaler.
In order to produce the first prerun pulse with a constant and sufficient length it is obviously necessary to synchronize the 1,5 MHz oscillator with the "RESET" pulse. For this purpose it is proposed to insert a coupling diode 1N914 as shown on the fig. 10, through which the inverted reset pulse being applied to a base of the multivibrator transistor would provide its forced turn off. Thus, the next cycle of the oscillator would be started by a rear edge of the reset pulse always under the same initial conditions.

4.3 The RF1999 generator prototype operated without any fault. As for the stability of the propagation delay time between the output RF 1999 pulses and those of the input RF train, it is expected to be negligible (see item 2.2).

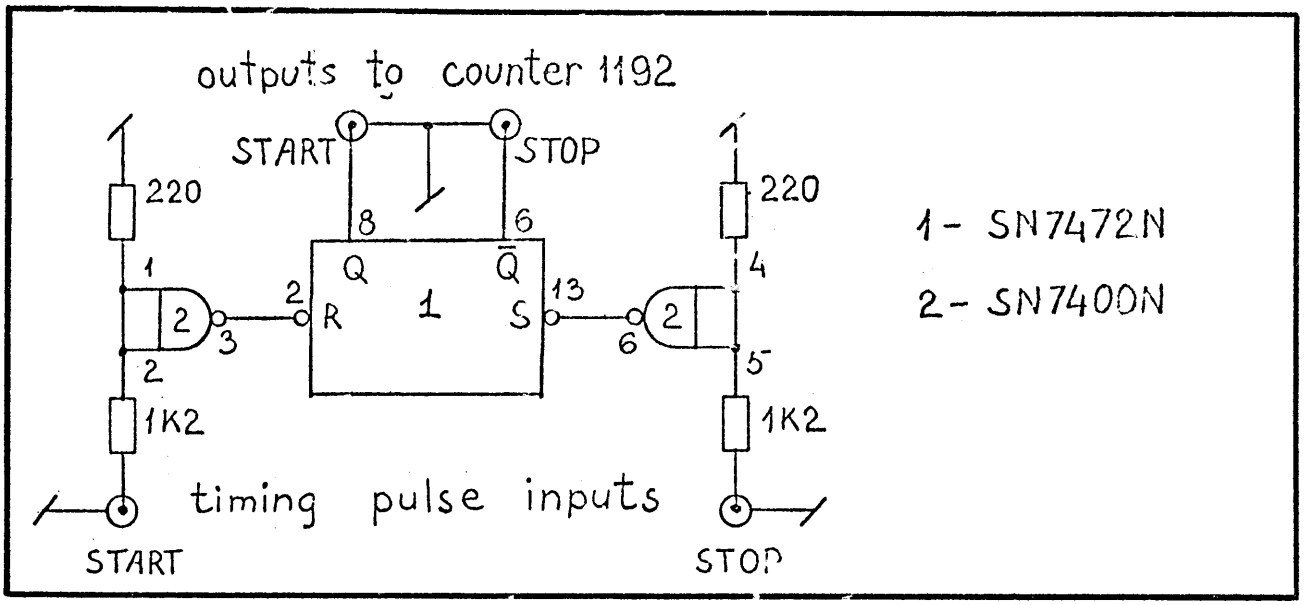


Fig. 1 : Adapter of type "A"

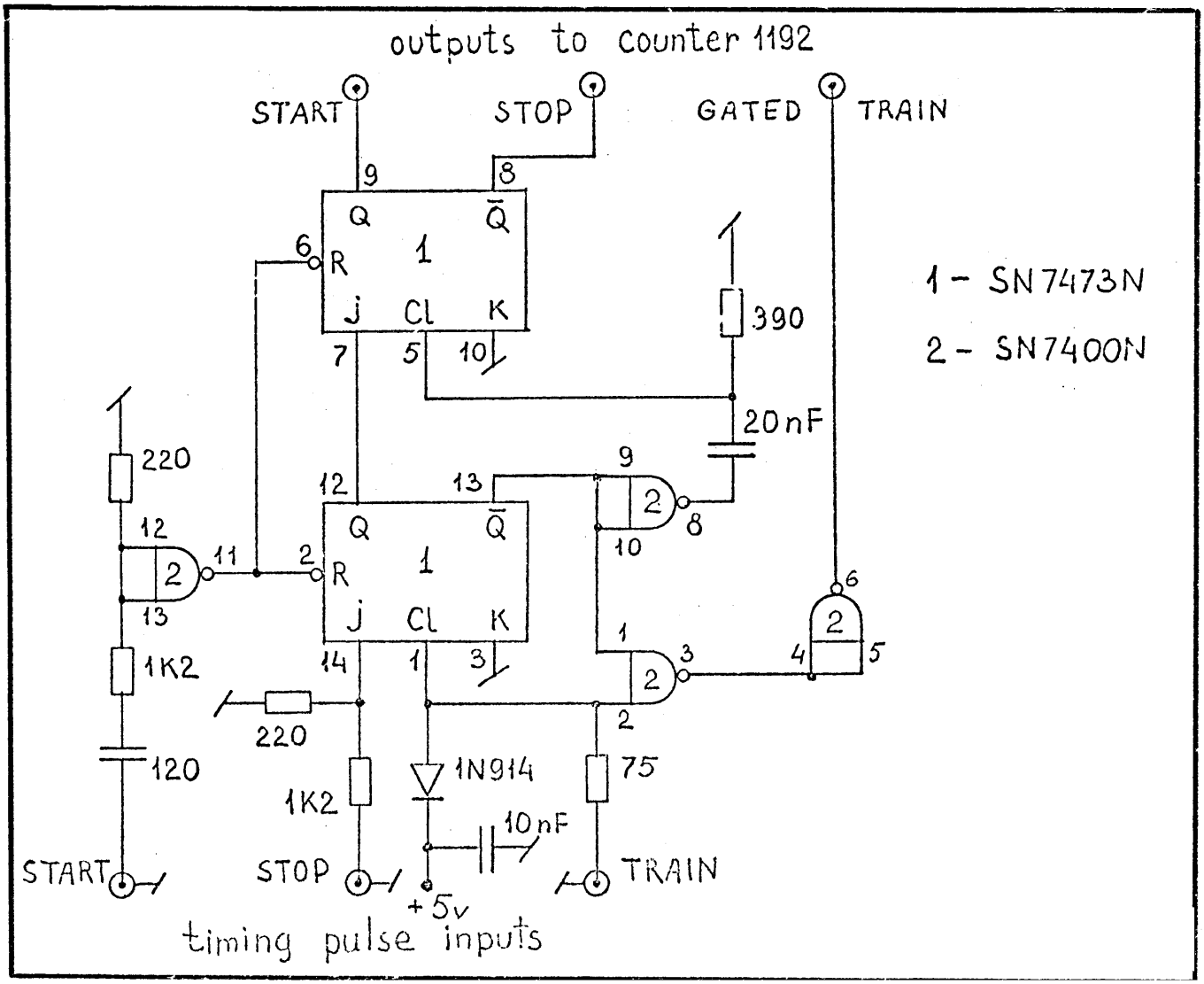


Fig. 2 : Adapter of type "B"

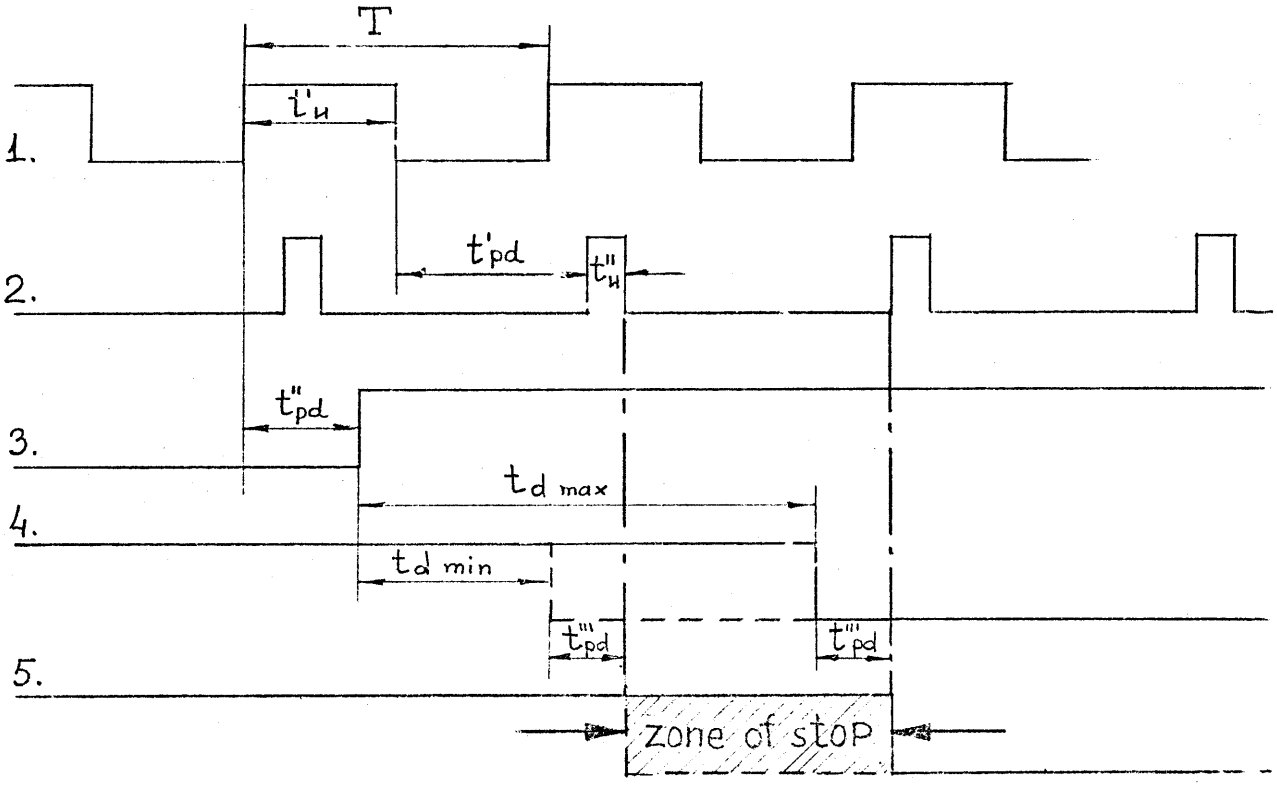


Fig. 3 : Definition of delay time for "STOP" signal

Pulses :

1 - RF 1999 train;

2 - Count pulses, formed in the counter 1192 from the negative edge of the corresponding RF 1999 pulses with a propagation delay time $t'_{pd} \simeq 100$ ns;

3 - RF scaler output pulse, formed from the positive edge of the selected RF 1999 pulse with a propagation delay time $t''_{pd} \simeq 60$ ns;

4 - Control signal, which has to be formed by an adapter from the positive edge of the output pulse and applied to input "STOP" of the counter 1192 with a delay time t_d which must be chosen as :

$$t''_u + t'_u + t'_{pd} - (t''_{pd} + t'''_{pd}) < t_d < T + t'_u + t'_{pd} - (t''_{pd} + t'''_{pd})$$

5 - Signal applied to the main gate of the counter 1192 and produced in it from the negative edge of the control signal "STOP" with a propagation delay time $t'''_{pd} \simeq 30$ ns.

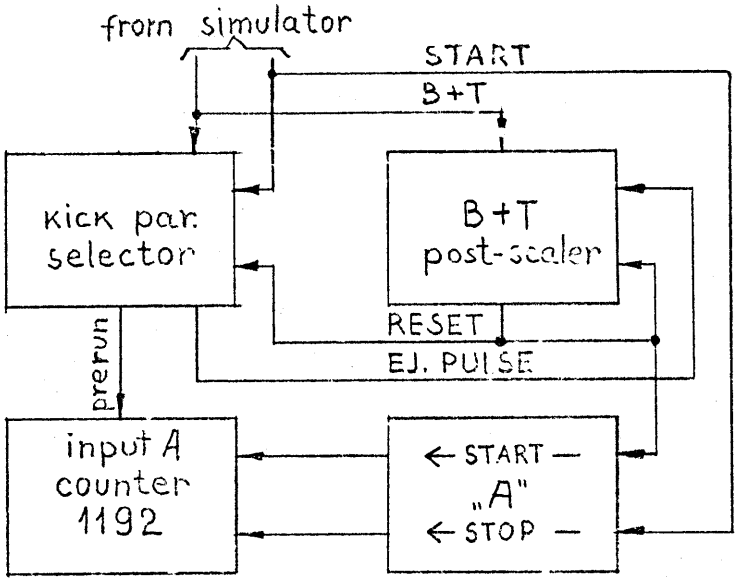


Fig. 4 : Prerun generation test scheme

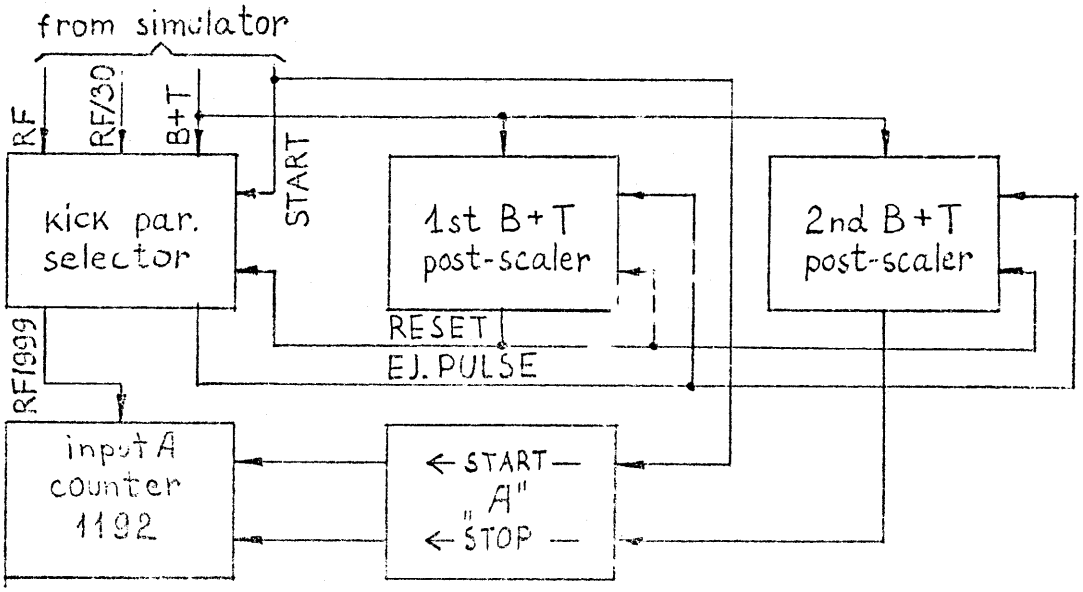
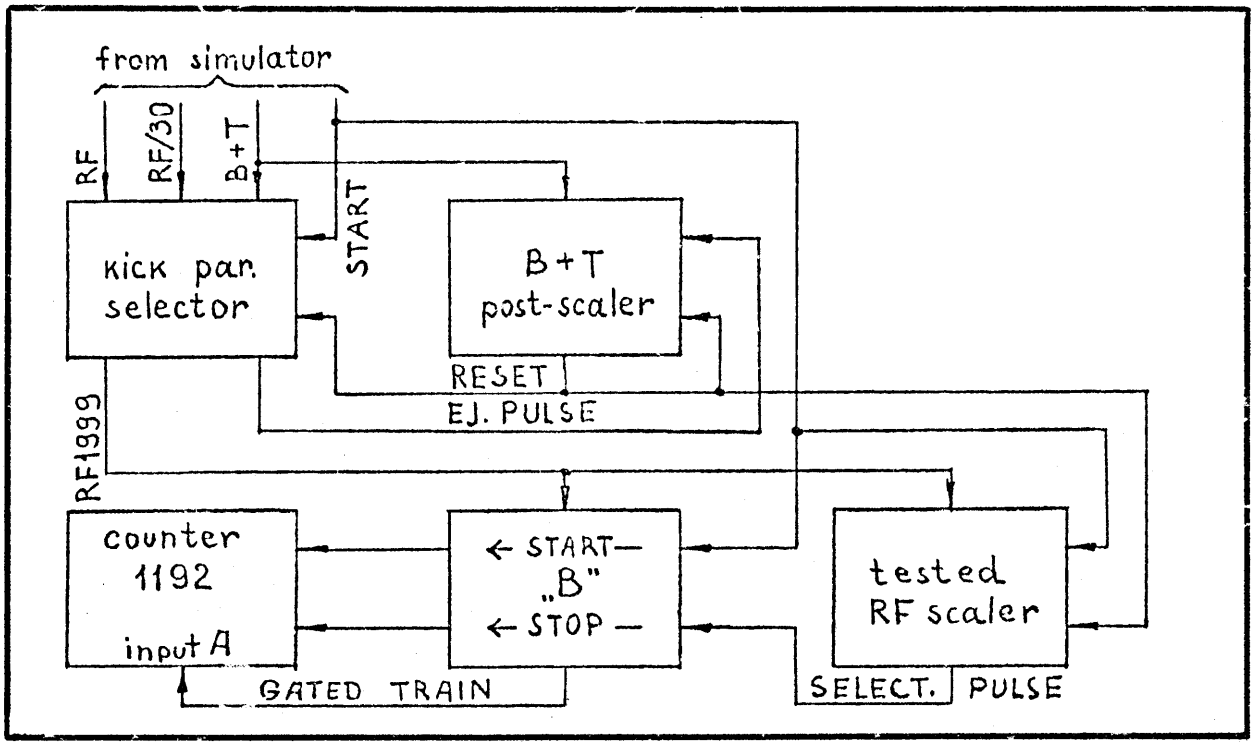


Fig. 5 : RF 1999 generation test scheme

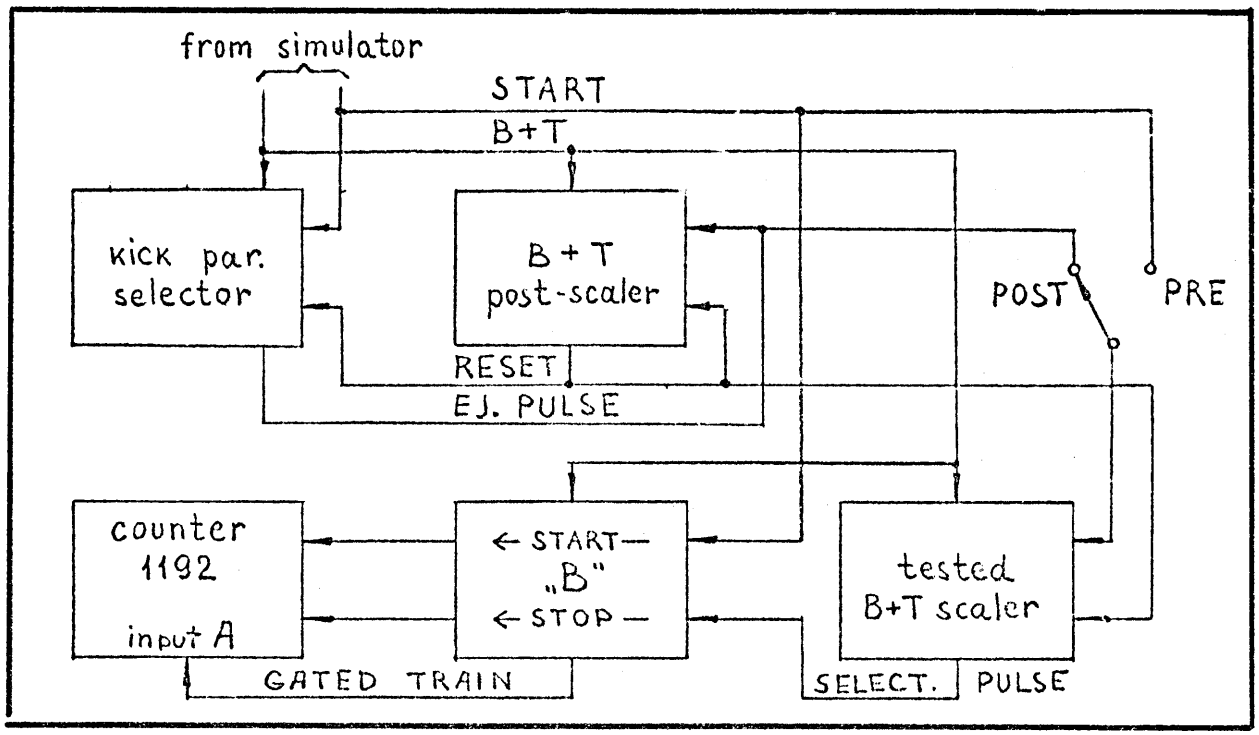
If $N_{post\ 1}$ and $N_{post\ 2}$ are the preselector position of the 1st and 2nd B+T post-scaler respectively, the following conditions must be fulfilled :

$$4 \leqslant N_{post\ 1} < N_{post\ 2}$$

to count all RF 1999 pulses but avoid the "parasitic" pulse registration.



a) RF pulse selection



b) B+T pulse selection

Fig. 6 : Pulse selection test scheme

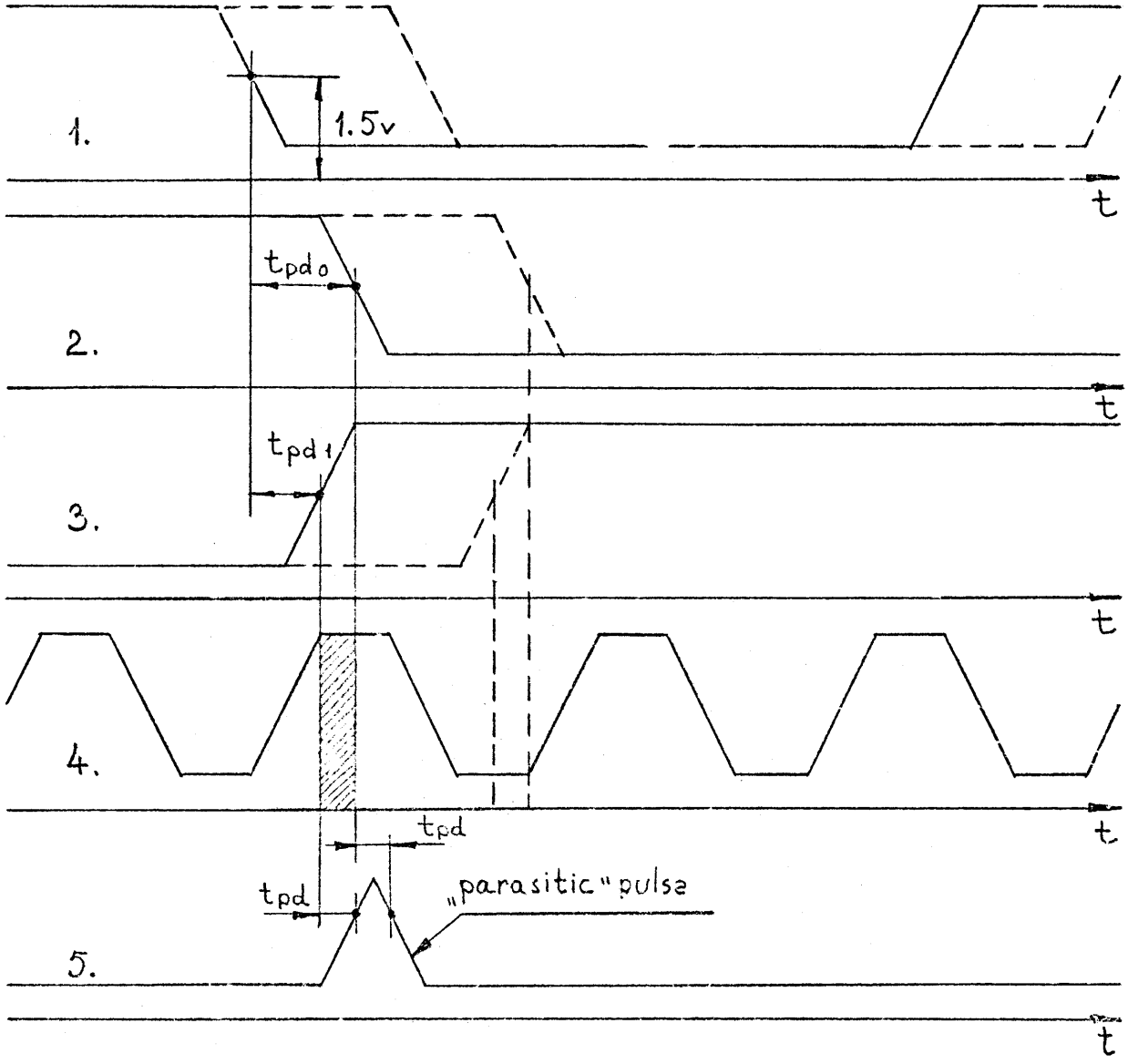


Fig. 7 : "Parasitic" pulse formation

Pulses :

1 - inverted "RESET" pulse applied to input "R" of the flip-flop 52 and to input "S" of the flip-flop 50;

2 - output "Q" of the flip-flop 52 applied to the 55 gate input (pin 9);

3 - output "Q" of the flip-flop 50 applied to the 55 gate input (pin 10);

4 - RF train applied to the 55 gate input (pin 11);

5 - output of the gate 55 (pin 8).

Notes :

1) for the flip-flops of type SN 74 H 72 N used here the $t_{pd_o} > t_{pd_1}$;

2) since the "RESET" pulse is not synchronized with the RF train pulses, the coincidence conditions can be absent (this case is marked by the dotted line) and as a consequence the "parasitic" pulse will not be produced;

3) the symbols used here correspond to the drawing 374-104-2.

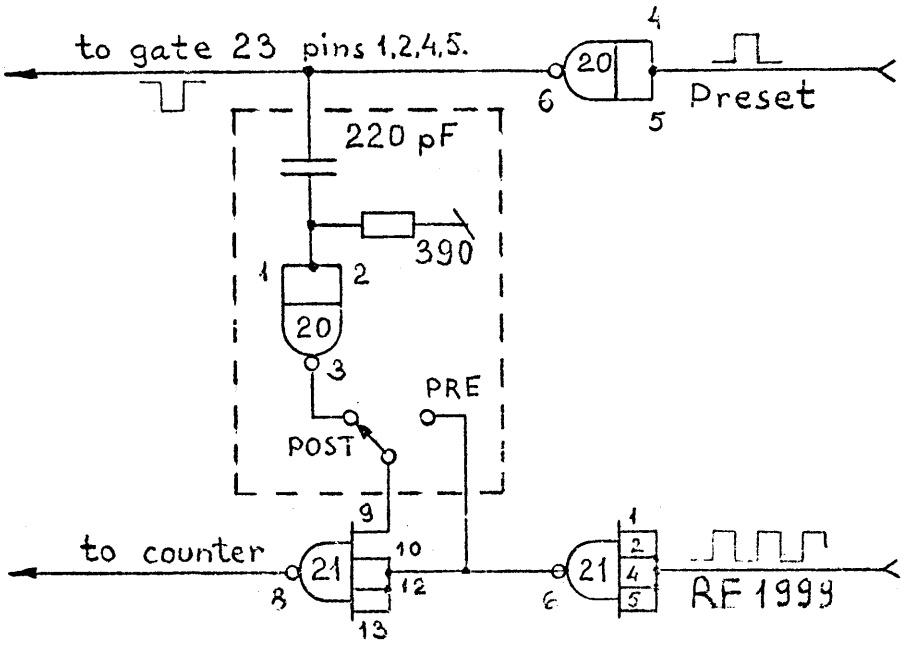
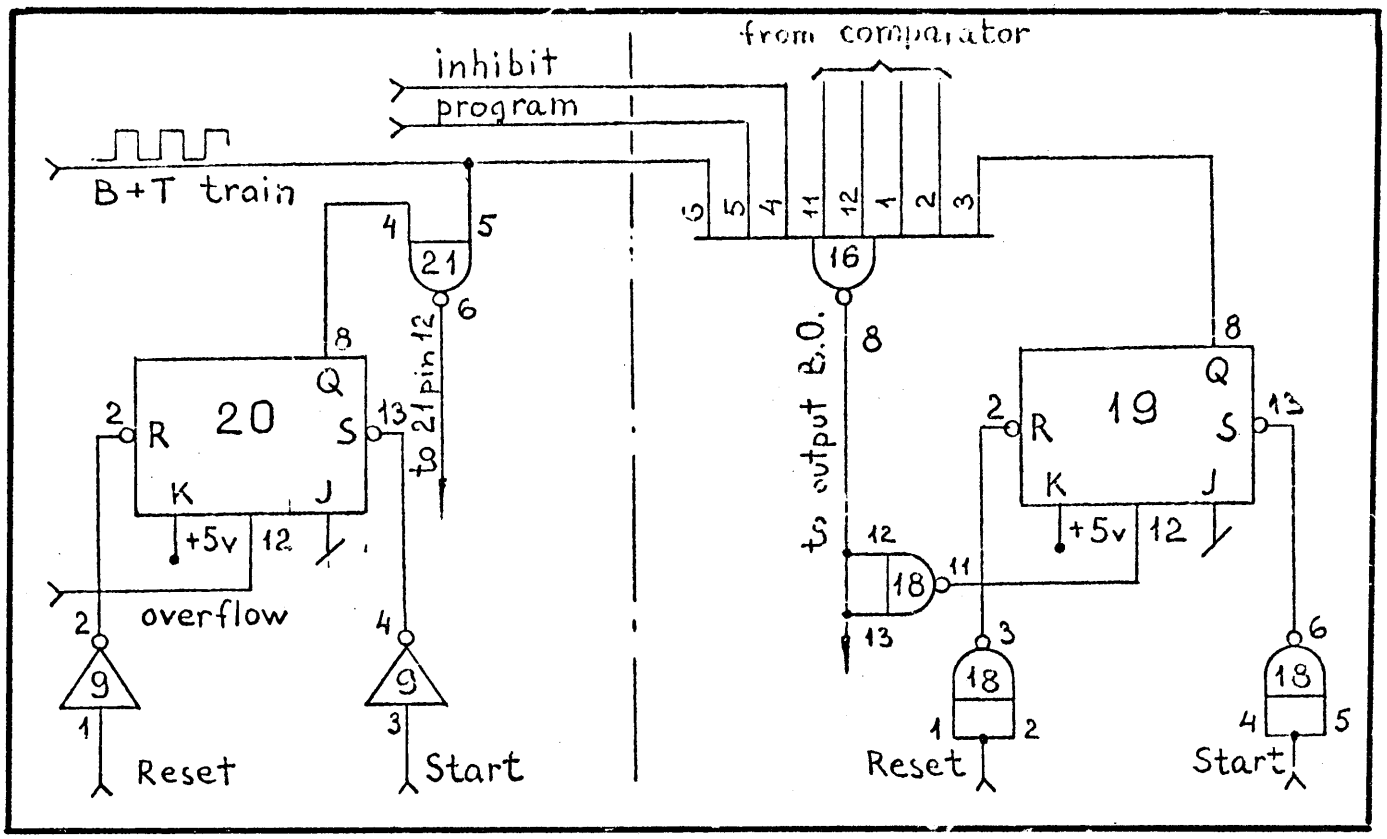


Fig. 8 : RF scaler modification

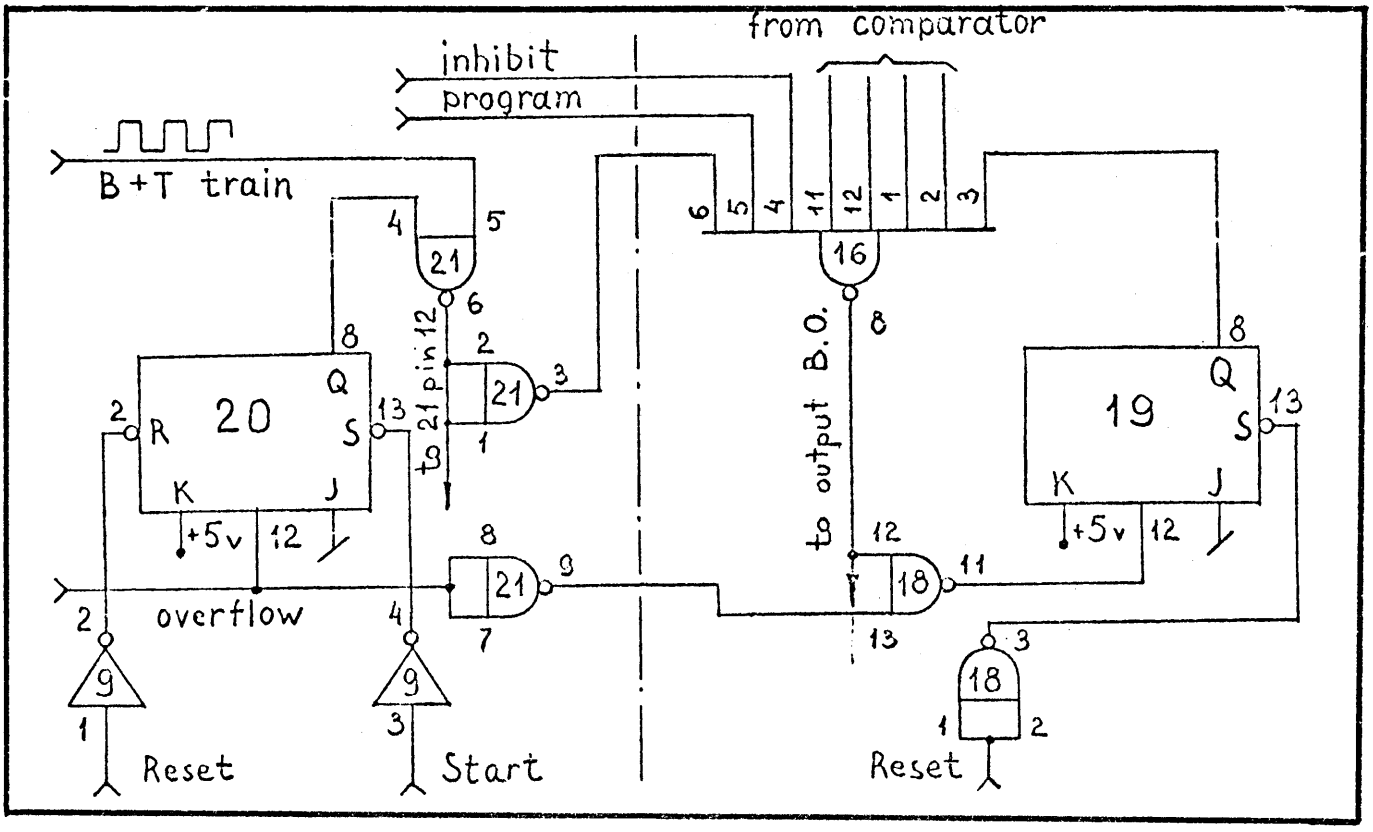
Notes :

1) The scheme part marked by a dotted line is inserted into the RF post-scaler to form the supplementary unit pulse;

2) The symbols used here correspond to the drawing 372-104-1.



a) Logic network before modification



b) Logic network after modification

Fig. 9 : B+T scaler modification

Notes : 1) the symbols used in the left hand side of the schemes correspond to the drawing 370-107-2;

2) the symbols used in the right hand side of the schemes correspond to the drawing 370-105-2.

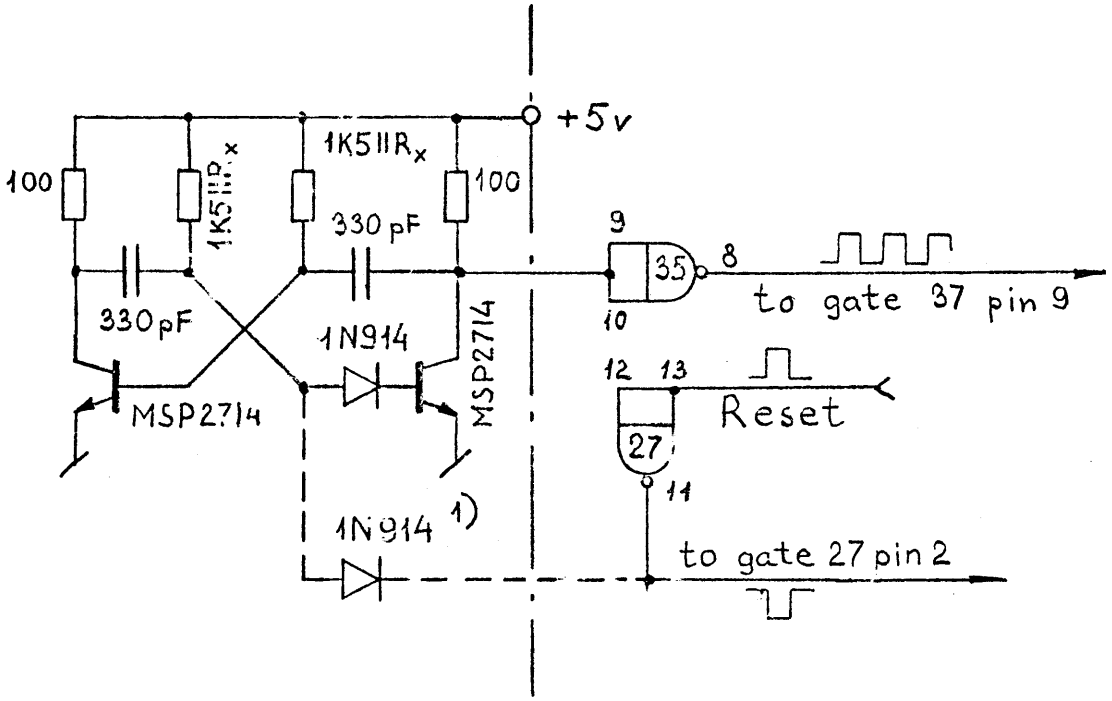


Fig. 10 : 1,5 MHz oscillator modification

Notes :

1) The coupling diode to be inserted as shown here;

2) the symbols used in the left hand side of the scheme correspond to the drawing 374-003-4;

3) the symbols used in the right hand side of the scheme correspond to the drawing 374-103-1.