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USER MANUAL FOR THE DUAL-DELAY VME-BOARD

H. Gaudillet and J. Schipper

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1. Introduction

The Dual-Delay Unit (DDU) is a VME card (6U - 1 slot) that has been developed to satisfy the needs to fine delay the "kick" pulses (for all the different kicker installations in the PS) from the VME environment.
The VME card has two channel inputs and can perform delays of up to 2 Êsec in steps of 1 nsec.
Although the module has been designed to meet the needs of the kicker section, it has been adapted for more general purposes.

The card accepts TTL inputs and the so called blocking signals (30V), as well as /TTL inputs .
The outputs available are of the TTL or /TTL standard.
Configuration of the input signals used is done by setting straps.

Furthermore a visual display, by means of LED's, is provided indicating if :

- input pulse is present (yellow LED)
- output is active (green LED)
- module has been accessed (yellow LED)

There is also the option to read back the delays set on both the channels.

2. Technical principle

The Dual-Delay Unit consists out of two identical digital delay lines, built around the Analog Devices AD9501, an 8-bit 255 nsec digital delay line used to perform the fine delays, i.e. 1 nsec steps.
By switching a bank of mono-stables each set to produce a delay of 256 nsec, the course delay can be obtained, i.e. 256 nsec steps.
Combining these two delays, a total delay of 2047 nsec in 1nsec steps can be obtained.
The circuit diagram of the DDU can be seen in fig. 1.

3. VME control of the Dual-Delay Unit

The Dual-Delay Unit is a slave module based on the A16/D16 short I/O addressing protocol.

The address modifier codes for the DDU are :
- $29 Short Supervisory Access
- $2D Short Non-Privileged Access

The address of the DDU is jumper selectable and covers the address lines A15, A14, A13, A12, A11, A10.
If the module is installed in a DSC in the PS use the standard VME module address for the DDU which is defined **$B000**.
The smallest address increment (if another module were to be installed) is **$0400**.
(This module would then be at address **$B400**)

The DDU has two channels if the Base address is $B000 then the addresses of the channels are :
- Channel 1 -> $B000
- Channel 2 -> $B002

The module name of the DDU in the PS database is **IocDUALDELAY**.

If the module is used in a DSC in the PS (*) the address pointer to the virtual address window can be found with the following code :

cc = IocModulPointer (IocDUALDELAY, lu, IOC_P1, &addr_ddu)

with ***addr_ddu** being the pointer to address the associated VME space.
More information on how to use the IocModulPointer code can be found in ref.1

(*) Note that the DSC's in the PS run under Lynx-OS, and this operating system uses virtual memory mapping, i.e. a program running under this OS can not access the physical memory directly.

4. Program example (principle)

If the delay desired on channel two is 2000 nsec. then :

- #define OFFSET_CH2 0x01 /* definition of offset addresses */
- short *addr_ddu; /* type declaration address pointer */
- short data; /* type declaration data */
- short val ; /* type declaration of read back value */
- int lu = 0 ; /* set logical unit 0 for first DDU */
- data = 2000; /* set delay to 2000 nsec */
- IocModulPointer (IocDUALDELAY, lu, IOC_P1, &addr_ddu); /* see ref. 1 */
- *(addr_ddu + OFFSET_CH2) = data; /* write delay channel 2 to DDU */
- val = *(addr_ddu + OFFSET_CH2); /* read delay channel 2 from DDU */

val is the optional read-back value and will be 2000 in this case.

Note that if all variables and pointers are of the type short and the address offsets are constants, the address offsets will automatically be incremented in the call *(addr_ddu + OFFSET_CH2), so that they point to a short.
Hence the fact that OFFSET_CH2 is **0x01** and **not 0x02**.

5. DDU module configuration (Straps set-up fig. 2)

Straps are indicated with a 'S' the first index number refers to the channel number and the second index number to the strap function.

- Select address A15 - A10 with its associated straps (0 or 1).

- S12 & S22 Select input /TTL or 50 ohms (50 ohms implies here that input is set to receive TTL or blocking signals.)

- S11 & S21 select input terminated (50 ohms) or high impedance if in TTL or blocking mode.

- S14 & S24 if strap in position 'OR' this channel will be a logical OR of both channels, if in position 'GND' output of this channel corresponds to the input.

- S13 & S23 if in position 1 maximum delay will be 256 nsec, if in position 2 maximum delay will be 2047 nsec.

The mono-stables with their individually controllable pulse duration should be set to give a delay of 256 nsec **each.**

Furthermore the offset and gain of the AD9501 have to be adjusted.
The adjustment procedure is described in **ANNEX 1.**

The output pulse width has been fixed at 1Êsec, but can be altered by replacing C115 and/or R121 for channel 1, and C215 and/or R221 for channel 2.

6. Technical Specifications

- Channels 2
- Input level TTL, /TTL, Blocking
- Output level TTL and /TTL
- Range 11-bit 2048 nsec (1nsec steps)
- Jitter <1nsec @ full-scale
- Input pulse width pw > 35 nsec
- Output pulse width ~1usec (can be altered)

The JEDEC output file for the programmation of the PLD AT22V10-25 used for handling the VME protocol can be found on the PC-network on G:\HOME\S\SCHIPPER\LOGIC\vme_a16.pp2.

7. References

1. USING DSC AT PS-PART OF THE USER'S MANUAL AND COOKBOOK.
A. Gagnaire, C.-H. Sicard
CERN PS/CO/Note 93-82 (Spec.)

DISTRIBUTION

Section Kicker PS/PA
W. Heinze, PS/CO
J.P. Riunaud, PS/PA

ANNEX 1

ADJUSTMENT PROCEDURE FOR THE DUAL DELAY UNIT

The measurements described are performed between input SK101/SK102 (SK201/SK202) and output SK103/SK104 (SK203/SK204) for channel 1 (channel 2). ('probing' inside the card is **not** necessary) The binary input data setting the desired delay will be referred to by 'data'.

1. Adjust offset AD9501 with P102 (P202) to minimum delay on output, with data = 0.

2. Adjust the gain AD9501 with P101 (P201) to a delay of 255 nsec on output, with data = 255.

3. Repeat 1 & 2 until both conditions are met.

4. Adjust P103 (P203) to a delay of 256 nsec on output, with data = 256.
   Verify with data = 511 (256 + 255).

5. Adjust P104 (P204) to a delay of 512 nsec on output, with data = 512.
   Verify with data = 767 (512 + 255).

6. Adjust P105 (P205) to a delay of 768 nsec on output, with data = 768.
   Verify with data = 1023 (768 + 255).

7. Adjust P106 (P206) to a delay of 1024 nsec on output, with data = 1024.
   Verify with data = 1279 (1024 + 255).

8. Adjust P107 (P207) to a delay of 1280 nsec on output, with data = 1280.
   Verify with data = 1535 (1280 + 255).

9. Adjust P108 (P208) to a delay of 1536 nsec on output, with data = 1536.
   Verify with data = 1791 (1536 + 255).

10. Adjust P109 (P209) to a delay of 1792 nsec on output, with data = 1792.
    Verify with data = 2047 (1792 + 255).

11. Repeat steps 1 - 10 for channel 2 with the pots indicated in brackets.

fig.1

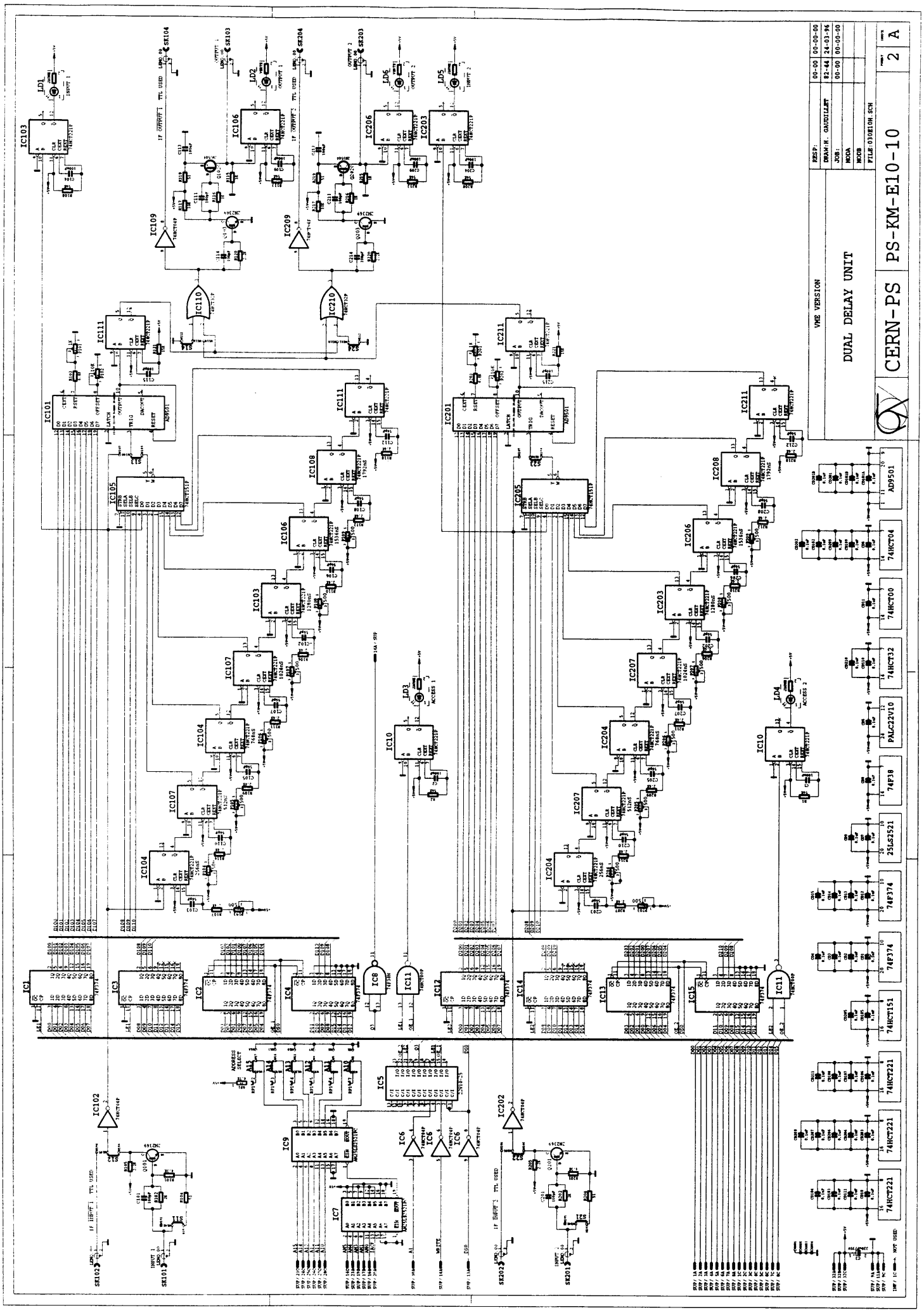
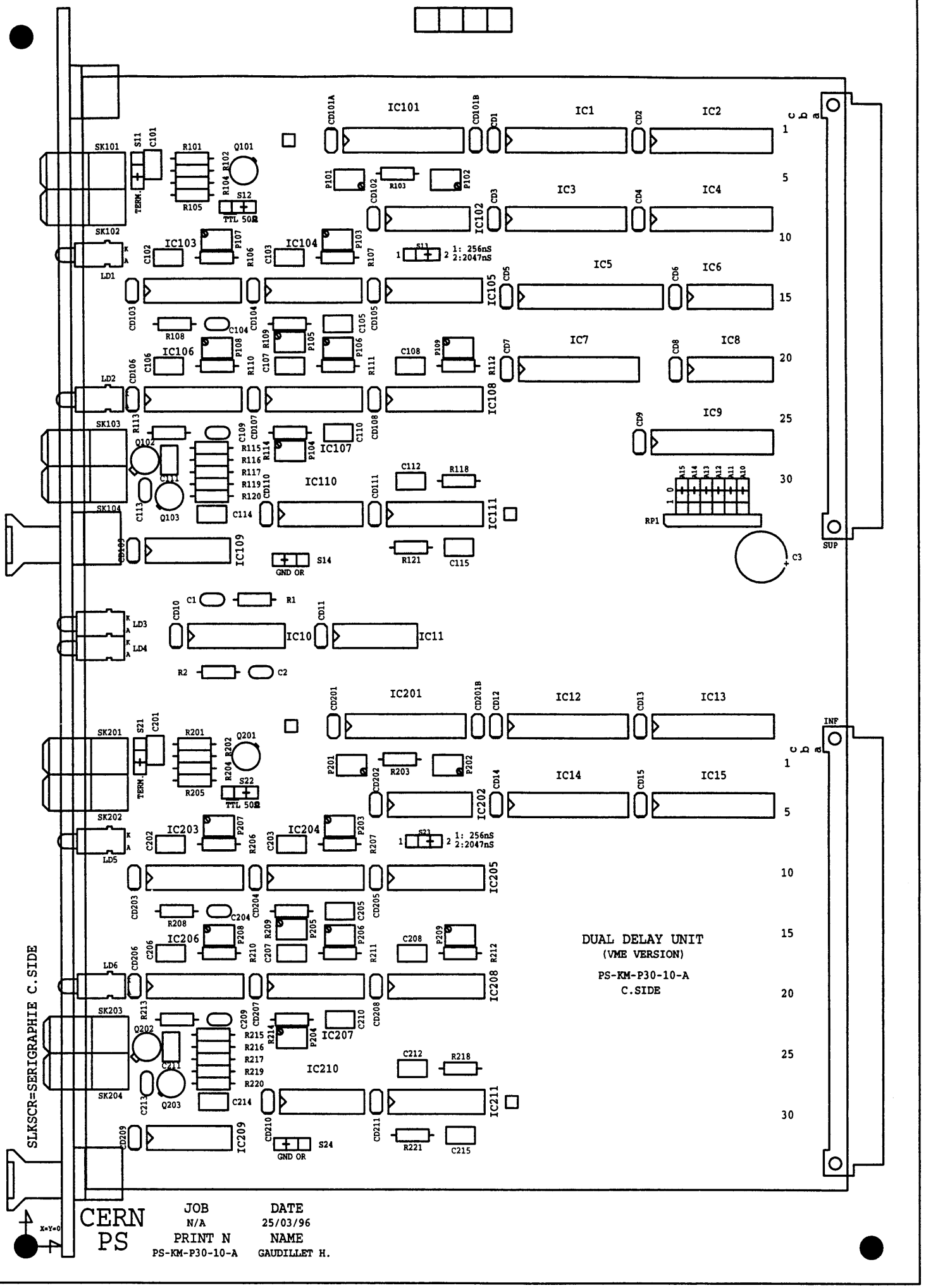

CERN-PS
PS-KM-E10-10
DUAL DELAY UNIT
VME VERSION
RESP:
DRAW:H. GAUDILLAT
JOB:
MODA
MODB
FILE:030810H.SCH
00-00-00
82-44 24-03-96
00-00 00-00-00
00-00-00
2 A

Fig. 2


IC101
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
IC11
IC12
IC13
IC14
IC15
IC103
IC104
IC106
IC107
IC109
IC110
IC111
IC201
IC203
IC204
IC206
IC207
IC209
IC210
IC211
SK101
SK102
SK103
SK104
SK201
SK202
SK203
SK204
LD1
LD2
LD3
LD4
LD5
LD6
Q101
Q102
Q103
Q201
Q202
Q203
S11
S12
S14
S21
S22
S23
S24
GND OR
TTL 50Ω
TERM.
1: 256nS
2:2047nS
RP1
SUP
INF
DUAL DELAY UNIT
(VME VERSION)
PS-KM-P30-10-A
C.SIDE
SLKSCR=SERIGRAPHIE C.SIDE
CERN
PS
JOB
N/A
PRINT N
PS-KM-P30-10-A
DATE
25/03/96
NAME
GAUDILLET H.