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GENERAL DESCRIPTION OF THE FAST EJECTION KICKER CONTROL AND ACQUISITION SYSTEM (KSU - KICK STRENGTH UNIT.)

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The CERN PS control system is being completely rejuvenated. The existing system, whose design options were frozen in 1978, uses 16 bit minicomputers for process computers and for conventional consoles and services.
These are being replaced by the agreed CERN Standard Architecture, using UNIX workstations as operator interface and VME based processors, under RT-UNIX.
This note describes the hardware and software implementations for the KFA 71/79 kicker system.

Geneva, Switzerland
20 May 1996

1. INTRODUCTION

This note describes the conversion of the KFA 71/79 control and acquisition system, for the fast PS ejection kickers, to allow adaptation to the control system changes mentioned in the abstract. The kicker system allows multi-user operations i.e., independently controllable parameters for the various ejection processes.
A user being a label for a set of parameters for a specific cycle.

The present system, controlled by CAMAC is limited in its input of users.
Furthermore it also has to be considered that all CAMAC will eventually become obsolete.
These considerations, plus the availability and variety of "off the shelf" Industrial components made us decide to update the system to the versatile VME-bus based model.

2. OVERVIEW OF THE CPS CONTROL SYSTEM

The standard model used in the CPS complex is the image of the common architecture of the CERN accelerator control system (fig.1); it consists mainly of three different layers;

- Control room (MCR) layer with workstations and central servers; the connection to this layer is done only through Ethernet cable

- Front end computing layer distributed around the machines, based on Device Stub Controllers, DSC-KSU for the kicker system.

- Equipment control layer, the kicker hardware controlled by the DSC-KSU.

Information on the first mentioned layer can be found in the various reports written by the controls group.

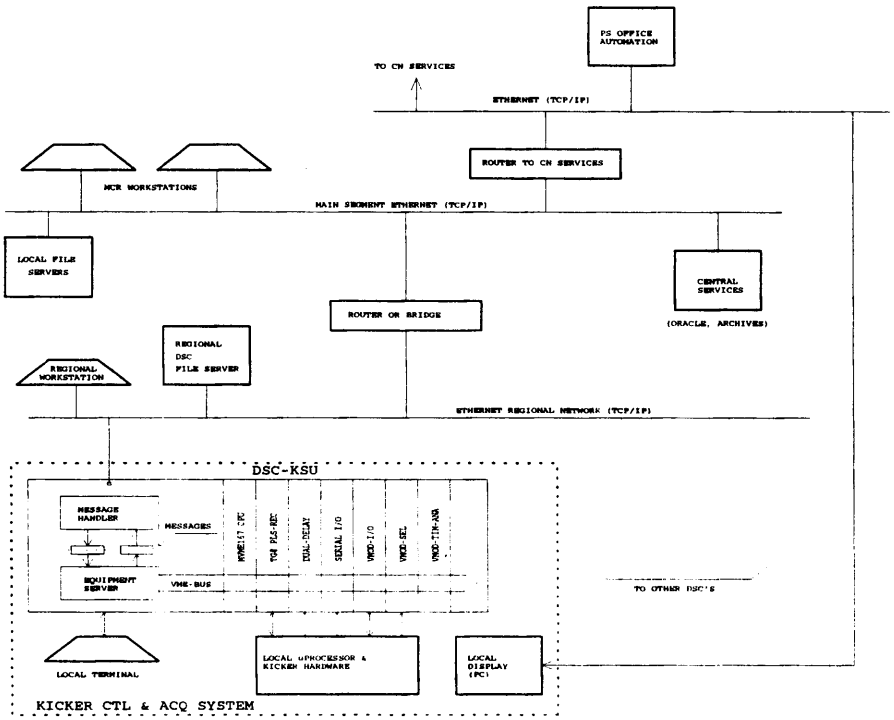

Fig.1

3. THE FRONT-END COMPUTING LAYER (DSC-KSU)

The DSC-KSU interface represents the front end computing layer in the new control system. It can be found in the local area, i.e. near the kicker hardware, connected to the MCR workstations via a LAN, and to the kicker hardware via VME hardware modules.
The main functions of the DSC are:

- To provide a uniform interface to the equipment as seen from the MCR workstations.
- To provide direct control and acquisition of the kicker hardware, interfaced directly to the DSC.
- To act as a master and data concentrator for all the Local Processor Units (installed on every kicker module), interfaced via RS232 serial I/O links.

The DSC comprises a real-time UNIX compatible Operating System, LynxOS, it allows to run several tasks concurrently. The DSC is diskless meaning that a DSC file server is required to provide storage space for the operating system, system startup files, application programs, the real-time task and their data files.
The DSC provides a fast and deterministic response to external events which is necessary when operating in PPM mode (pulse to pulse modulation.)

PPM - operations whereby a system performs a function upon the arrival of a particular event sent by the PLS and performs the same function upon every subsequent similar event without re-programming.

PLS - program line sequencer, timing system consisting of a bit stream, containing information such as user, cycle and particle type.

4. COMMUNICATION BETWEEN FRONT-END AND CONTROL ROOM

Someone wishing to change the control parameters for the KFA kicker system would access it by means of an application program running on a workstation in the MCR. This program allows the user to enter commands and view the results.

The application program does not communicate with the real-time task directly however, but via a message handler and equipment server (fig1), the so called equipment module, which is running on the same DSC as the real-time task. It is the duty of the equipment module to verify the validity of the request from the user before sending it to the real-time task, as well as receiving resultant messages.

An option included in the real-time program is to control and display status and acquisition data of the whole KFA71-79 complex via the tty1 terminal in/output of the DSC-KSU.

5. LOCAL ACCESS FACILITIES

- Local display, showing the status and acquisition of the kicker complex for synoptic use.
- Local terminal, connected to the CPU via tty1 terminal in/output, for local control of the ksu71-79 real-time task.
- Regional workstation, not for specific applications, can be seen as duplication of some services in the MCR.

6. KFA 71/79 SYSTEM

The KFA system consists of 12 kicker modules each one having its own Local Processor Unit.
To allow multi-users operations, the different 'kicks' have to be modulated in pulse amplitude and width, to obtain the desired beam deflection.

The functionality of the KFA system is based on the standard PFN(cable) principle, see fig.2.

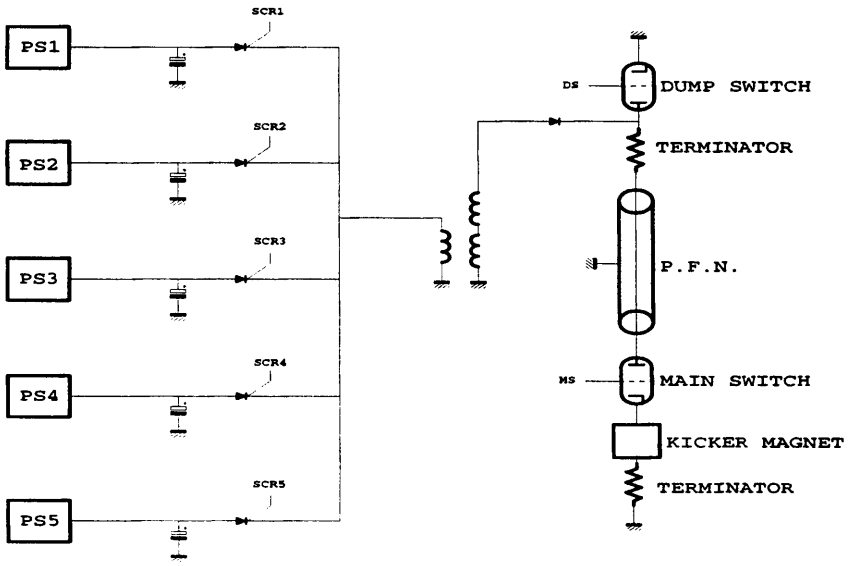

Fig.2

Note that in this diagram four extra capacitor banks have been added, so that the PFN can be charged to different voltage levels from cycle to cycle by triggering the different SCR's (Warning signals.)
Due to hardware limitations the programmable supplies (PS1-PS5) charging the capacitor banks, should once set, remain at the same potential on all cycles (not absolutely necessary but recommended for stability performance reasons.)

A new charge control unit is in the design stage, it will not have these limitations, but can charge or discharge to the desired value from cycle to cycle.
This will simplify the multi-user operations to two capacitor banks, one for batch A and one for batch B, however the design of the new KSU has to include the functionality of the old charge control unit, for at least until the start-up in 1997.

The power supplies defining the pulse amplitudes are set by DAC's in the Local Processor Unit, and the pulse width is controlled by the MS & DS timing signals (START & END signals.)
By combining the different kicker modules the required beam deflection will be obtained.

7. DSC-KSU CONTROL AND ACQUISITION

7.1 Block diagram KFA71-79 control and acquisition system

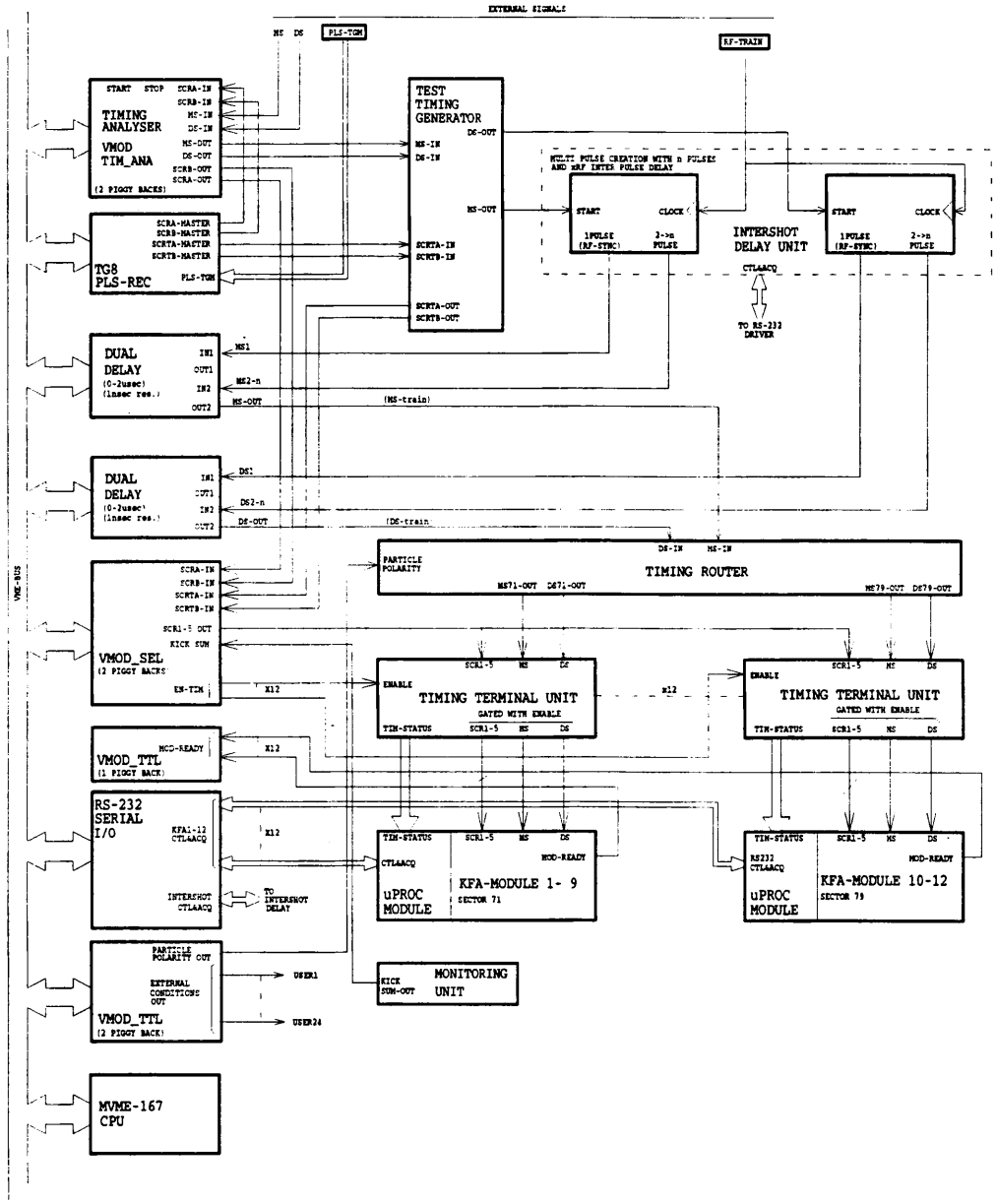

Fig.3

The block diagram above shows the lay-out of the KFA control and acquisition system, in the following paragraphs the global functions of the system will be discussed.
Furthermore a short description will be given of the modules that form the interface between kicker equipment and MCR workstations. (i.e. the VME-modules).

7.2 Global functions

The KFA71-79 can produce an ensemble of kick pulses, as can be seen in the figure below, to obtain the desired ejection of the particle beam.

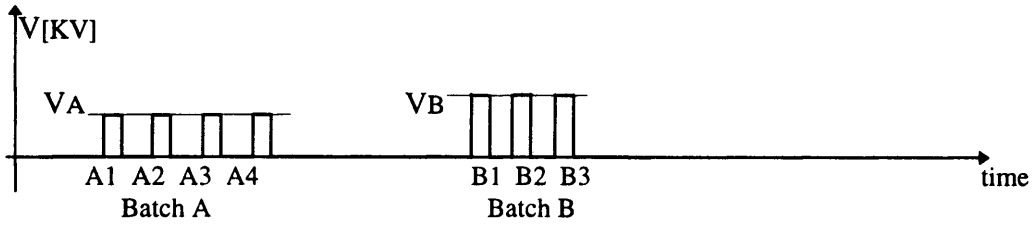

fig.4

Kick: A voltage pulse causing a deflection of the particle beam.
Batch: Group of several 'kicks' of the same amplitude.

In a given cycle there can be a maximum of two batches (Batch A and Batch B), the order of activation is transparent to the KSU, i.e. batch B can start before batch A.

In the example batch A has 4 pulses A1-A4 with amplitude VA and batch B has three pulses B1-B3 with amplitude VB, the parameters for batch A and batch B are independently controllable and have been selected to obtain a flexible control system from the operators environment.

Note The following equation has to be met when setting up a batch :

Nk / Np > = Vbatch / Vmax-mod

Np = number of pulses per batch
Nk = number of kicker modules (12 modules)
Vmax-mod = maximum kick amplitude per module (83kV)
Vbatch = requested kick amplitude (minimum = 30kV)

The PPM control parameters for batch A are:

- Kick on/off (batch A)
- Pulse amplitude (VA)
- MS 1 fine delay (delays start of first pulse on batch A)
- DS 1 fine delay (delays stop of first pulse on batch A)
- Pulse number (Pulses to be generated for batch A)
- Intershot delay (delay between two pulses in batch A, based on the RF pulse train)
- MS 2-n fine delay (delays start of second to last pulse on batch A)
- DS 2-n fine delay (delays stop of second to last pulse on batch A)

The non-PPM control parameters are:

- Deselect modules, this control input gives the option to deselect (a) module(s), i.e. the de-selected modules can not be used for any of the 24 USER's.
- Set-up, activating this variable resets all kickers and reassigns the kicker modules to the USER's.

The control parameters for batch B are identical to the ones for batch A.
The timing and (MS, DS and Intershot) delay parameters will be discussed in the next chapter.

The module assignment to the different users is calculated inside the DSC along a given algorithm, deciding which KFA module is pulsing at what operation, taking into account the hardware limitation of the charge control unit.

The kick strength data, when calculated for each module, is then stored in memory and transmitted to the Local Processor Units, via the RS232 interface card.
This data sets the DAC's that are controlling the programmable power supplies, feeding the capacitor banks.

7.3 Timing

RF- and fine delays

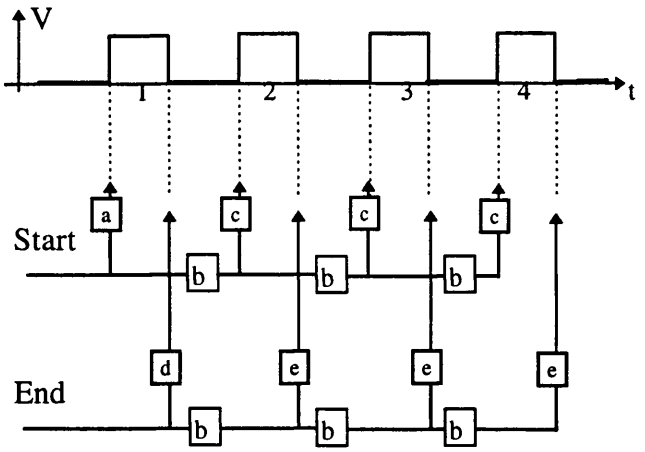

fig.5

Every batch is composed out of three major timing signals which are externally generated :

- SCR (warning), for charging the PFN.
- MS (start), controlling the rising edge of the kick pulse.
- The DS signal (end), controlling the falling edge of the pulse.

In the example of fig.5 there are four pulses in a batch, implying that there must be three more 'start' and 'end' pulses, this is correct but they are generated locally by means of the Intershot Delay Unit (IDU).
The IDU has a RS232 link with the DSC-KSU who informs the IDU after an SCR pulse has arrived how many pulses are desired and the RF-delay (b in fig.5) between the pulses on this batch.
With this information the IDU generates the required burst of start and end pulses.

The IDU also makes a separation between the first MS (MS 1) and the following burst (MS 2-n), the same is done for the DS pulses. (DS 1 and DS 2-n)
This makes it possible to delay the first pulse independently from the following burst of pulses.

The delays are set up with the DUAL-DELAY VME-module (0-2μsec, 1nsec resolution.) (ref.7), developed in the PS kicker section.

Summary of independently controllable delays per batch :

a. MS 1 fine delay (0-2µsec, 1nsec resolution)	PX.SKFA71AF
b. RF-intershot delay (delay in RF-periods)	
c. MS 2-n fine delay (0-2µsec, 1nsec resolution)	PX.EKFA71AF
d. DS 1 fine delay (0-2µsec, 1nsec resolution)	PX.SDKFA71AF
e. DS 2-n fine delay (0-2µsec, 1nsec resolution)	PX.EDKFA71AF

The second column describes the equipment names used in the PTIMD equipment module, for batch B the AF should be replaced by BF.
In chapter 8 is described how to access the listing of these properties.

7.4 SCR-generation

The different SCR signals are generated quasi external, that is to say they are generated inside the DSC-KSU, by a so called TG8 module, but their programmation is performed by the controls group.
The TG8 is a multi purpose VME timing module, which receives messages distributed over a timing network (PLS-telegram.)
These messages include timing information, clock plus calendar and telegrams instructing the accelerator on the characteristics of the next beam to be produced.
The TG8 supplies the KSU with the active user and particle type at the start of a cycle, furthermore it supplies the following timing signals :

• ELFT	(PX.ELFT_PK71)	end of last flat top
• SCR A	(PX.WKFA1)	warning batch a
• SCR B	(PX.WKFA2)	warning batch b
• SCR TA	(PX.WTKFA1)	warning batch a test (@ C100)
• SCR TB	(PX.WTKFA2)	warning batch b test (@ C130)

These signals will provoke an interrupt signal for the real time task.

Furthermore a check will be performed on the timing sequence, (SCR, MS and DS) and a timing fault status will be returned. (see ANNEX 1)
This is realised with the **VMOD_TIM_ANA** card, a VMOD-IO piggy back VME card.(ref. 8)

The timing signals supplied to the modules selected for a specific operation are enabled with the **VMOD_SEL** card (VMOD-IO piggy back board see ref.9), by sending a gate signal to the module Timing Terminal Unit (TTU), the modules will be deselected after they have sent a kick return signal, indicating that they have pulsed.
The modules can now be prepared for the next selection.
If a timing error is detected, the KSU has to generate a 'DS SAFETY' signal to discharge the PFN cable, this is done inside the VMOD_TIM_ANA card.

A table of selected modules and HV kick strength and other relevant status and acquisition information, "KFA 71/79 General Status" display, will be available on local as well as on control room level.

7.5 Modules Ready, External Conditions and Particle Type Detection

In order for the KSU to select kicker modules which are in the ready state, i.e. kickers that are ready to pulse, there has to be a direct feedback from all the kicker modules indicating this status. These signals are received by the DSC by means of the so called **VMOD-TTL** I/O board, a VMOD-IO piggy back board, internally set to receive data. (ref.11)

Furthermore if an equipment error occurs, implying that there are not enough modules to perform the required operation, a signal has to be returned on the USER in question.
There are 24 USER's therefore there are 24 so called 'EXTERNAL CONDITIONS' signals.
This signal will then be treated externally, so that further beam injection into the PS can be blocked on this USER.
This action is performed by another two VME VMOD-TTL I/O boards set to send data.

Further use is made of the VMOD-TTL I/O to signal to a timing distribution unit the polarity of the particles.
This unit will delay the MS (start)- and DS (end) signals depending on the polarity of the particles being accelerated, i.e. taking into account the particle flight time between KFA79 and KFA71.

7.6 Local Processor Unit

Communication from DSC-KSU to the kicker modules is obtained via a local processor, which is positioned in every kicker module.
Connections from and to the processor are based on the RS232 serial I/O principle, with the communication speed set at 9600 baud.
The VME module performing this task in the DSC are two **IP-Octal 232** (ref. 13)piggy back boards installed on the **VIPC610** (ref.12) mother board. (Greenspring computers)
The VIPC610 conforms to the IndustryPack Logic Interface Specification.

The local processor receives its instructions from the DSC, passes it on to the KFA module, and returns a set of status parameters after cycle end.

The control parameters are:
- On/off, standby and reset commands.
- Pulse amplitude.

The acquisition parameters returned from the local processor to the DSC are:
- Interlock status.
- Status of KFA module (on/off, standby etc.)
- H.V. kick strength (pulse amplitude in kV.)

8. EQUIPMENT MODULE ACCESS

The properties with their description for the ksu71-79 can be found on the PS network in the file :
- /ps/doc/postscript/eqm_056_ksu.ps

Equipment names:
1. PR.KFA71A for batch A
2. PR.KFA71B for batch B

The VME dual delay, fine delay properties for the ksu71-79 can be found in the file:
- /ps/doc/postscript/eqm_250_ptimd.ps

Equipment names:
1. PX.SKFA71AF (MS1 fine delay batch A)
2. PX.EKFA71AF (DS1 fine delay batch A)
3. PX.SDKFA71AF (MS2-n fine delay batch A)
4. PX.EDKFA71AF (DS2-n fine delay batch A)
5. PX.SKFA71BF (MS1 fine delay batch B)
6. PX.EKFA71BF (DS1 fine delay batch B)
7. PX.SDKFA71BF (MS2-n fine delay batch B)
8. PX.EDKFA71BF (DS2-n fine delay batch B)

Or via **NETSCAPE** connect to http://psas01/
PS Accelerator Control System
Select **control modules**
and enter **ksu or ptimd.**

For **detailed** property information of the KFA71-79 system see **ANNEX 1**

This summarizes the hardware implementations for the KFA71/79 control and acquisition system. On the following pages the software part i.e. the real-time program will be described.

9. REAL-TIME PROGRAM FOR THE KFA 71/79 FAST EJECTION KICKER SYSTEM

Description of the real-time multi-threaded program under LynxOS for the KFA 71/79 fast ejection system.
A multi-threaded process can be thought of as a process with many paths or "threads" of execution which can all be executed at the same time.

9.1 INITIALISATION PHASE

Sequence of actions taken after start of **main()**.

- Attach to the PLS telegram received by the TG8
- Connect to the interrupts generated by the TG8
- Initialise hardware
- Set kickers on
- Wait till minimum amount of modules are ready
- Set all banks of all modules to initialisation voltage of 40kV
- Create threads - **pls()** - **action()**

9.2 THREADS CREATED

main() can also be seen as a thread, **main()** has the lowest priority and runs a local data control program (ksudat) after the initialisation phase, allowing total control of the KFA71-79 kicker complex including the Test Operation (see chapter 9.3).
The threads **pls()** and **action()** are set at the same priority, but a higher priority than **main()** and perform the real-time task for the ksu71-79 .

pls() ; actions followed by the arrival of a CPS telegram, received by the TG8.

Action taken upon arrival:
- read user number and particle type.
- if control data has changed perform the following actions :

1. Perform control action(s) if requested. (on, off, standby, reset, deselect)
2. (Re)-calculate modules required per operation and voltage per module.
3. Assign module numbers and capa-banks to the physics operations.

If an ejection has to be performed, i.e. if kick is on :

4. Program VMOD-SEL (for enabling the timing on the required modules)
5. Sleep till arrival of a new CPS telegram

action() ; thread which waits for one of the following interrupt from the TG8 module:

1. ELFT end of last flat top
2. SCR A warning batch a
3. SCR B warning batch b
4. SCR TA warning batch a test
5. SCR TB warning batch b test

On arrival of an ELFT signal perform the following actions :

- Read acquisition results from the Local Processor Units via the RS232 link
  1. Interlock status
  2. HV kick strength
  3. Status of the module

- Calculate ΣHV kick strength
- Write acquisition and status results into memory
- Sleep till new interrupt signal ELFT arrives

On arrival of one of the SCR (warning) signals perform the following actions (if kick is on) :

1. Program dual delay cards for MS (start) and DS (stop) fine delays.
2. Program Intershot delay unit with required RF delay, if multipulsing.

main() , is a thread with the lowest priority and sleeps most of the time.
It allows local data input, by means of a function called ksudat.c.
With this function all the ksu71-79 control functions can be executed locally.

9.3 USER-TEST FOR SPECIALISTS

A special test operation has been included which can be seen as an extra USER (USER25) .
With this user ejections can be simulated, without interfering with the particle beam.
Its use is intended for kicker specialists only and it can perform double batch multi-shot operations.

The warning signals are generated by the TG8 module and are activated on every USER .
SCR TA, warning batch A is active @ C100.
SCR TB, warning batch B is active @ C130.

These signals are fed to the timing simulator unit which generates the start and stop pulses, further functions are identical to the ones under normal operation.

The start (MS) and end (DS) signals can be fine delayed as for the normal operations mentioned in chapter 7.2 **(see also ANNEX 1)** the equipment names used in the PTIMD equipment module are the following :

- MS 1 fine delay (TEST) PX.STKFA71AF
- MS 2-n fine delay (TEST) PX.ETKFA71AF
- DS 1 fine delay (TEST) PX.SDTKFA71AF
- DS 2-n fine delay (TEST) PX.EDTKFA71AF

(for batch b replace AF by BF)

If however the test operation uses too many modules to allow a proper functioning of the standard ejection operations, the modules assigned to the test operation will be overridden and used for the standard operations.

10. CONCLUSION

The described system with one central control system the DSC-KSU via which all external communication is routed and with every kicker individually controllable via the Local Processor Unit, allows a very flexible system.

The flexibility obtained with this set-up allows compatibility for the installation of future kicker control and acquisition systems.

The real-time program for the ksu71-79 can be found on the PS network in the directory
/ps/local/home/schipper/ksu and
/ps/local/home/schipper/ksu/include

The programs forming the real-time task (ksu71-79) are :

- ksu71main.c
- ini_all.c
- ksu_calc.c
- pls.c
- ksudat.c
- ksu.h

This concludes the general description of the hard- and software control and acquisition system for the KFA 71/79 fast ejection kickers.
In **ANNEX1** a detailed listing of the properties for the KFA71-79 system can be found.

11. REFERENCES

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8. USER MANUAL FOR THE VMOD-TIM-ANA PLUG-IN CARD
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   PS/PA/Note 96-21

9. USER MANUAL FOR THE VMOD-SEL PLUG-IN CARD
   J. Schipper
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    JANZ Computer AG, Germany

11. VMOD-TTL Version 1.0 Data sheet (November 1990)
    VME MODULbus 20 channel TTL-I/O
    JANZ Computer AG, Germany

12. VIPC610 User Manual
    Quad IndustryPack Carrier for 6U VMEbus Systems
    GREENSPRING Computers

13. IP-Octal 232 User Manual
    IndustryPack 8 channel RS232 piggy back
    GREENSPRING Computers

14. LynxOS Device Driver for IP-Octal Serial
    Software Installation Manual
    SYSGO Mainz, Germany

ANNEX 1

DETAILED PROPERTY INFORMATION FOR THE KFA71-79 KICKER SYSTEM (KSU)

The 'KSU' equipment module has two members and are defined as follows :

Memberno	Equipment name	DSC	Description
6001	PR.KFA71A	dcpsk71	KFA71-79 batch A
6002	PR.KFA71B	dcpsk71	KFA71-79 batch B

NOTE
All properties mentioned in this note are of the variable type EQM_TYP_INT, except CCV the kick amplitude which is of the variable type EQM_TYP_REAL.

CONTROL PARAMETERS (ppm)	Property name
1. Actuation batch (Kick on)	CCSACT
2. Kick strength (Pulse amplitude)	CCV
3. Number of pulses	NUMBER
4. Intershot delay in RF periods	DELAY

ad.1 Kick on
bit 0 = 1 => ON

ad.2 Amplitude in kV
Vmin = 32kV
Vmax = 996kV

GLOBAL CONTROLS (non-ppm)	Property name
• De-select module(s) (Select = 0, De-select = 1) bit 0 = Module 1 : : bit 11 = Module 12	SELECT
• Reset (SET-UP) - (bit 0 = 1 => reset) Reset modules and / or recalculate kicker table (RT-task will reset bit 0)	RSET
• Module control operations (x = module number) definition : bit 0 = 1 => MODULE OFF bit 1 = 1 => MODULE ON bit 2 = 1 => STANDBY bit 3 = 1 => RESET only one bit should be active, reset of ONOFx will be done by RT-task	ONOFx

STATUS (ppm)

Property name - STAQ

STAQ is a three dimensional array containing the following information :

- STAQ[0] - Global Status

  Global status has the following structure :
  (active high)
  bit 0 = KICK ON
  bit 1 = INTERLOCK
  bit 2 = TIMING ERROR
  bit 3 = Too many Users / too many modules not ready
  bit 4 = Requested operation not compatible with equipment (outside limits)
  bit 5 = NO DATA TRANSMISSION (no communication Local Processor Unit => KSU)

- STAQ[1] - Timing Error

  1 byte of timing error information defined as following :
  (active high)
  bit 0 = HARDWARE ERROR
  bit 1 = EARLY
  bit 2 = LATE
  bit 3 = MISSING
  bit 4 = STOP (DS)
  bit 5 = START (MS)
  bit 6 = SCR

  bit 6, 2, 1 SCR MULTI-PULSING
  bit 5, 4, 2, 1 PULSE TOO LONG

- STAQ[2] - Selected modules and capacitor banks on last operation

(bit 0 - bit 11 modules selected, bit 0 module 1 selected, bit 1 module 2 selected etc. active high)

selected capa-bank definition :

bit 14	bit 13	bit 12	
0	0	0	no selection
0	0	1	bank 1 selected
0	1	0	bank 2 selected
0	1	1	bank 3 selected
1	0	0	bank 4 selected
1	0	1	bank 5 selected
	rest		error

ACQUISITION (ppm)

Property name - AQN

AQN is a four dimensional array containing the following acquisition information :

- AQN[0] - Kick strength - sum of kick strength of selected modules in kV
- AQN[1] - Pulse width - pulse width of first pulse in batch, kick sum return
- AQN[2] - Pulse width - pulse width of first pulse in batch, theoretical
- AQN[3] - Pulse width - pulse width of second pulse in batch, kick sum return

At the moment of writing this report the pulse width measurements were not available yet

ACQUISITION PER MODULE (non-ppm)

Property name - SELECTx (x indicating the module number)

SELECTx is a five dimensional array containing the following information :

- SELECTx[0] - Status of module x

  definition :

  (set **high** = true)
  bit 0 - WARNING (errors occurred without immediate interlock fault)
  bit 1 - POWER ON (presence of 3-phase)
  bit 2 - OIL INTERLOCK
  bit 3 - HT INTERLOCK
  bit 4 - NO DATA TRANSMISSION (KSU - KICKER)
  bit 5,6,7 - not used

- SELECTx[1] - Status of module x

  definition :

  (set **low** = true)
  bit 0 - OFF
  bit 1 - GO STANDBY
  bit 2 - STANDBY
  bit 3 - GO ON
  bit 4 - ON
  bit 5 - MODULE CAN BE RESET
  bit 6 - LOCAL
  bit 7 - LOCAL/REMOTE SWITCH (causes interlock when switched)

- SELECTx[2] - Interlock of module x

  definition :

  (set **high** = true)
  bit 0 - PLC
  bit 1 - DS FAULTY SHOT
  bit 2 - MS FAULTY SHOT
  bit 3 - DS G1
  bit 4 - MS G1
  bit 5 - DS OILFLOW
  bit 6 - MS OIL FLOW
  bit 7 - RESISTOR OILFLOW

- SELECTx[3] - Interlock of module x

  definition :

  (set **high** = true)
  bit 0 - HT SWITCH
  bit 1 - EMERGENCY STOP RING
  bit 2 - EMERGENCY STOP CB
  bit 3 - RING VACUUM
  bit 4 - SF6 PFN
  bit 5 - SF6 TRANSMISSION CABLE
  bit 6 - OVER VOLTAGE
  bit 7 - IP PROTECTION

- SELECTx[4] - Interlock of module x
  (not-used)

STATUS INDICATOR OF MODULES CAUSING INTERLOCK (non-ppm)

Property name - INTLK

definition :
active high = > interlock
bit 0 - mod1,
: :
bit 11 - mod12

TEST OPERATION PARAMETERS

Control parameters for operation test
Property name - TEST1

TEST1 is a six dimensional array containing the following control values :

- TEST1[0] - Kick on/off (bit 0 = 1 => ON)
- TEST1[1] - Pulse amplitude in **0.1kV** steps
- TEST1[2] - Intershot delay in RF-periods
- TEST1[3] - Pulse number
- TEST1[4] - Modules selected (bit 0 = mod 1, bit 11 = mod 12)
- TEST1[5] - Capa-banks selected (1 to 5)

ACQUISITION AND STATUS FOR OPERATION TEST

The acquisition and status parameters for the operation test have the same format as the ones for normal operations
Property name - TESTAQ (equivalent to AQN)
Property name - TESTAT (equivalent to STAQ)

VME DUAL DELAY - fine delays (ppm)

The fine delay parameters are seen as a part of the timing system and are therefore organised in a different equipment module nl. PTIMD
The 'PTIMD' equipment module has 16 members and are defined as follows :

Memberno	Equipment name	DSC	Description
6601	PX.SKFA71AF	dcpsk71	MS1 fine delay batch A
6602	PX.EKFA71AF	dcpsk71	DS1 fine delay batch A
6603	PX.SDKFA71AF	dcpsk71	MS2-n fine delay batch A
6604	PX.EDKFA71AF	dcpsk71	DS2-n fine delay batch A
6605	PX.SKFA71BF	dcpsk71	MS1 fine delay batch B
6606	PX.EKFA71BF	dcpsk71	DS1 fine delay batch B
6607	PX.SDKFA71BF	dcpsk71	MS2-n fine delay batch B
6608	PX.EDKFA71BF	dcpsk71	DS2-n fine delay batch B
6609	PX.STKFA71AF	dcpsk71	MS1 fine delay test batch A
6610	PX.ETKFA71AF	dcpsk71	DS1 fine delay test batch A
6611	PX.SDTKFA71AF	dcpsk71	MS2-n fine delay test batch A
6612	PX.EDTKFA71AF	dcpsk71	DS2-n fine delay test batch A
6613	PX.STKFA71BF	dcpsk71	MS1 fine delay test batch B
6614	PX.ETKFA71AF	dcpsk71	DS1 fine delay test batch B
6615	PX.EDTKFA71AF	dcpsk71	MS2-n fine delay test batch B
6616	PX.EDTKFA71BF	dcpsk71	DS2-n fine delay test batch B

Property name - CCV

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